LIN Transceiver for Automotive

BD41030FJ-C

General Description

BD41030FJ-C is the best transceiver for BUS system which need LIN (Local Interconnect Network) master and slave protocol.
BD41030FJ-C is available in small SOP package and low standby electricity consumption in sleep mode.

Features

- AEC-Q100 Qualified(Note 1)
- Absolute maximum ratings of LIN pin is -27V to+40V
- Max transmission rate 20kbps
- Low Electro Magnetic Emission (EME)
- High Electro Magnetic Immunity (EMI)
- High impedance at power off for bus
- Interface (RXD/TXD) with protocol layer corresponds to 3.3V/5.0V logic.
- Built-in terminator for LIN slave
- Standby power consumption in sleep mode
- Transmit data(TXD) dominant time-out function
- Resistant to LIN-BAT/GND short-circuit
- Built-in Thermal Shut Down(TSD)

(Note1:Grade1)

Applications

- LIN communication for Automotive networks.

Key Specifications

Supply Voltage:	5V to 27V
Supply Current (Sleep mode):	1µA to 8µA
Supply Current: (Standby mode; Recessive)	100µA to 1000µA
Supply Current: (Normal mode; Recessive)	100µA to 1000µA
Supply Current: (Normal mode; Dominant)	200µA to 2000µA

Package(s)

Package(s)	W(Typ) x D(Typ) x H(Max)
SOP-J8	4.90mm x 6.00mm x 1.65mm

SOP-J8

Typical Application Circuit(s)

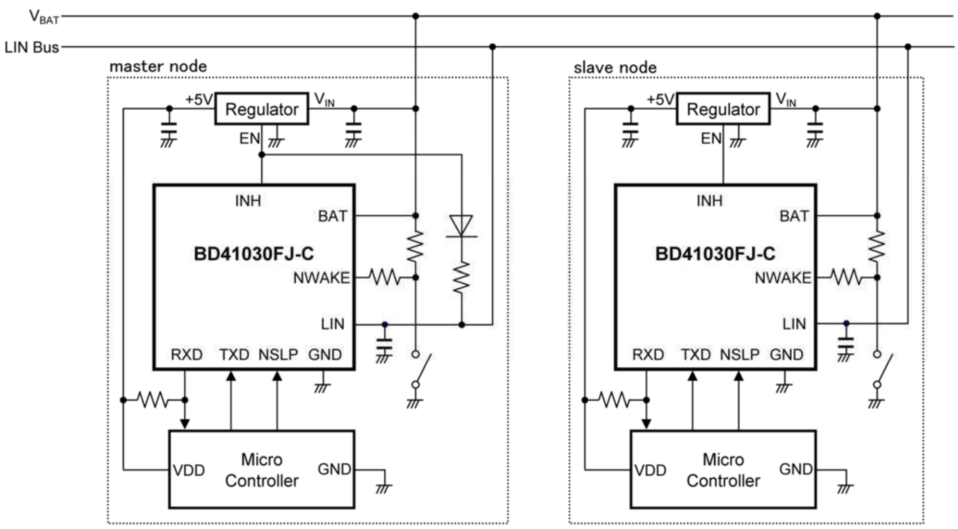


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration(s)

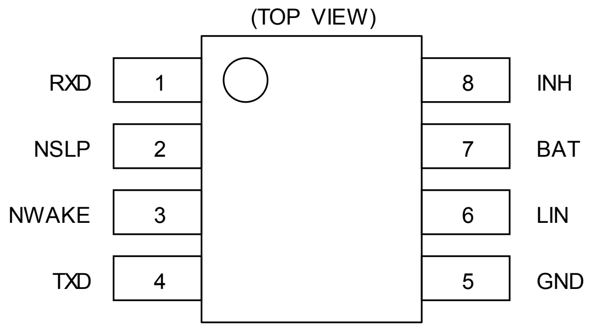


Figure 2. Pin Configuration

Pin Description(s)

Table 1. Pin Description

Pin No.	Pin Name	Function
1	RXD	Received data output pin (Open Drain). "L" is output at standby mode.
2	NSLP	Sleep control input pin ("L" Active mode). Shift to sleep mode by "L" input in normal mode.
3	NWAKE	Local wake-up input pin ("L" Active mode). Active at leading edge.
4	TXD	Transmission data input pin("L" Active mode)
5	GND	Ground
6	LIN	LIN bus input and output pin.
7	BAT	Power supply pin.
8	INH	Sleep status indicator. "Hi-z" at sleep mode and "H" in the other modes.

Block Diagram(s)

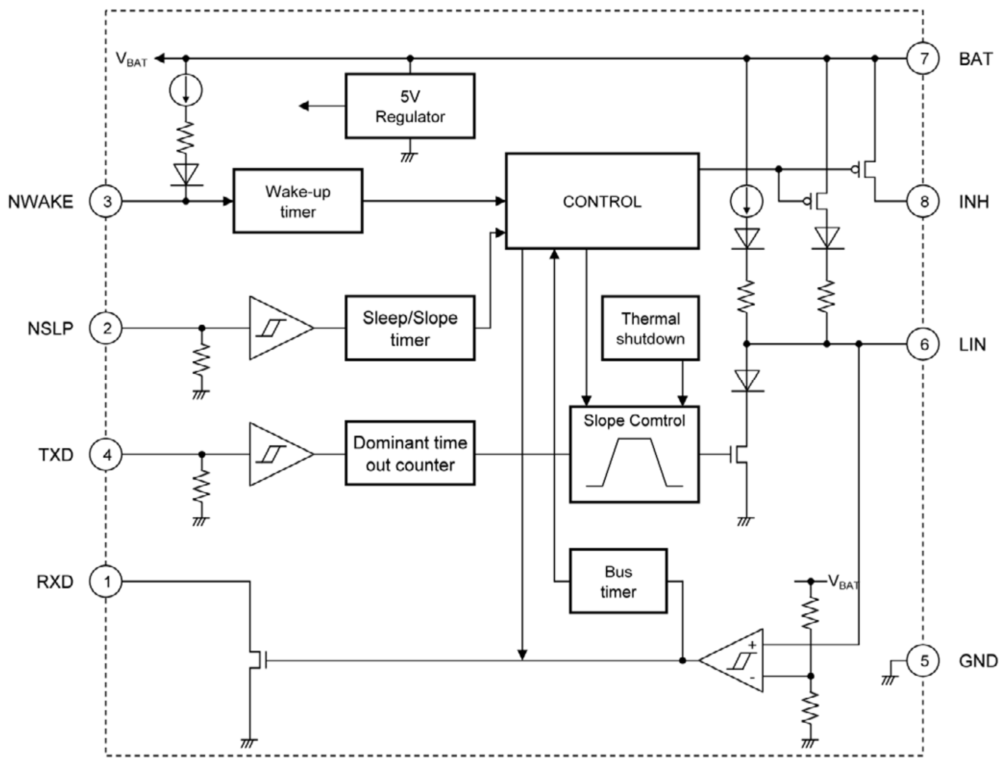


Figure 3. Block diagram

Description of Block(s)

1. Sleep mode

In sleep mode, the transmit/receive function is not available and BD41030FJ-C is under the condition of low power consumption mode. In this mode BD41030FJ-C shifts to sleep mode at startup of power supply (V_{BAT}) when NSLP is “L” or in normal mode also when pin NSLP is “L”.
During sleep mode, one of the following wake-up events triggers a shift of state:

・Pin NWAKE “H” → “L” (Shift to standby mode)
・Pin LIN “H” → “L” → “H” (Shift to standby mode)
・Pin NSLP “L” → “H” (Shift to normal mode)

The above-mentioned wake-up events shift the mode when a state remains for a given period of time (t_{NWAKE}, t_{BUS}, $t_{gotonorm}$). Hereinafter, a wake-up event on pin NWAKE is defined as Local wake-up, and a wake-up event on pin LIN is defined as Remote wake-up.

2. Standby mode

When a wake-up event occurs on pin NWAKE or pin LIN in sleep mode, BD41030FJ-C shifts to standby mode.
In standby mode, pins become the following state:

・Pin INH “H” (≒V_{BAT} voltage)
・Pin RXD “L” (Informs the microcontroller of being in standby mode.)
・Pin LIN Slave resistor ON

BD41030FJ-C shifts from standby mode to normal mode when pin NSLP input switches to “H”.

3. Normal mode

BD41030FJ-C shifts to normal mode when pin NSLP switches to “H” in sleep mode or standby mode. In normal mode, data can be transmitted or received through the bus line. When receiving data, the transceiver informs a LIN bus input from pin RXD to the microcontroller. When transmitting data, the transceiver converts a TXD input signal to a slew-rate-controlled LIN bus signal and informs the bus line of the converted signal. The maximum operating frequency in this mode is 10 kHz.
From this mode, BD41030FJ-C shifts to sleep mode when pin NSLP input switches to “L” and this state remains for a given period of time ($t_{gotosleep}$).

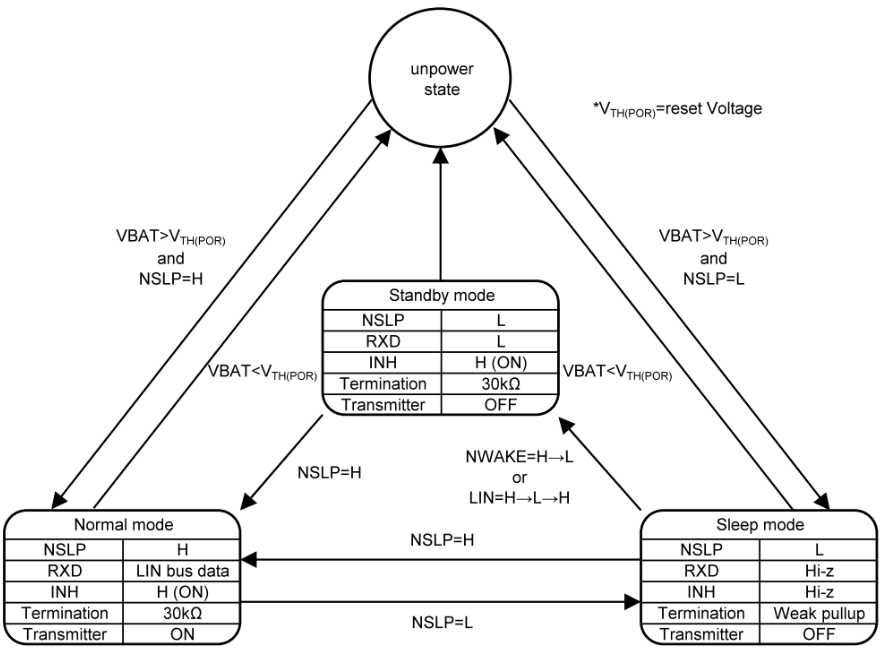


Figure 4. State Transition Chart

Table 2. The state of the pin in each mode

MODE	NSLP	TXD	RXD	INH	TRANSMITTER
Sleep mode	L	pull-down	Hi-z	Hi-z	OFF
Standby mode	L	pull-down	L	H	OFF
Normal mode	H	pull-down	H : recessive state L : dominant state	H	ON

4. TXD dominant time-out counters Fail-safe function

A TXD dominant time-out counter prevents the bus line from being driven to a permanent dominant state (blocking all network communication) in case pin TXD input is forced permanently low by a hardware and/or software application failure. The timer is trigged by a negative edge on pin TXD and in case the value exceeds the internal timer value (t_{dom}), the transmitter becomes disabled and drives the bus line into a recessive state. The timer is reset by a positive edge on pin TXD input.

5. Fail-safe function

・Pin TXD provides a pull-down to GND in order to force a predefined level on input pin TXD in case the pin TXD is not connected.
・Pin NSLP provides a pull-down to GND in order to force the transceiver into sleep mode in case the pin NSLP is not connected.
・Pin RXD is “Hi-z” in case of lost power supply on pin V_{BAT}.
・The output driver at pin LIN will be off when junction temperature exceeds T_J activating the TSD circuit without relation to input signal at pin TXD. However, when junction temperature drops below T_J the output driver at pin LIN will depend again on the input signal at pin TXD.

Absolute Maximum Ratings (Ta = 25°C)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage on pin BAT(Note 1)	V_{BAT}	-0.3 to +40.0	V
DC voltage on pin TXD, RXD, NSLP	V_{TXD}, V_{RXD}, V_{NSLP}	-0.3 to +7.0	V
DC voltage on pin LIN	V_{LIN}	-27 to +40	V
DC voltage on pin NWAKE	V_{NWAKE}	-1 to +40	V
Current on pin NWAKE(Note 2)	I_{NWAKE}	-15	mA
DC voltage on pin INH	V_{INH}	-0.3 to V_{BAT} + 0.3	V
Output current at pin INH	I_{INH}	-50 to +15	mA
Power dissipation(Note 3)	Pd	674	mW
Storage temperature range	T_{stg}	-55 to +150	°C
Junction Max temperature	T_{jmax}	+150	°C
Electro static discharge（HBM）(Note 4)	V_{ESD}	4000	V

(Note 1) Pd, ASO should not be exceeded.
(Note 2) Available only when $V_{NWAKE} < V_{GND}$-0.3V. Current flow to pin GND.
(Note 3) Regarding above Ta=25°C, Pd decreased at 5.40mW/°C for temperatures when mounted on 70x70x1.6mm Glass-epoxy PCB.
(Note 4) JEDEC qualified.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Range	Unit
Supply voltage	V_{BAT}	5.0 to 27.0	V
Operating temperature range	T_{opr}	-40 to +125	°C

Electrical Characteristics (Ta= -40 to +125°C; V_{BAT} =5 to 27V; $R_{L(LIN-BAT)}$ =500Ω; typical values are given at Ta=25°C; V_{BAT} =12V; unless otherwise specified)

Table 5. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BAT						
Supply current 1 on pin BAT (Sleep mode)	I_{BAT1}	1	3	8	μA	Sleep mode. V_{LIN} = V_{BAT} V_{NWAKE} = V_{BAT} V_{TXD} = 0V V_{NSLP} = 0V
Supply current 2 on pin BAT (Standby mode, Recessive)	I_{BAT2}	100	400	1000	μA	Standby mode. V_{LIN} = V_{BAT} (bus: Recessive) V_{INH} = V_{BAT} V_{NWAKE} = V_{BAT} V_{TXD} = 0V V_{NSLP} = 0V
Supply current 3 on pin BAT (Note 1) (Standby mode, Dominant)	I_{BAT3}	300	900	2000	μA	Standby mode. V_{BAT} = 12V V_{LIN} = 0V (bus: Dominant) V_{INH} = V_{BAT} V_{NWAKE} = V_{BAT} V_{TXD} = 0V V_{NSLP} = 0V
Supply current 4 on pin BAT (Normal mode, Recessive)	I_{BAT4}	100	400	1000	μA	Normal mode. V_{LIN} = V_{BAT} (bus: Recessive) V_{INH} = V_{BAT} V_{NWAKE} = V_{BAT} V_{TXD} = 5V V_{NSLP} = 5V
Supply current 5 on pin BAT (Note 1) (Normal mode, Dominant)	I_{BAT5}	200	1000	2000	μA	Normal mode. V_{BAT} = 12V (bus: Dominant) V_{INH} = V_{BAT} V_{NWAKE} = V_{BAT} V_{TXD} = 0V V_{NSLP} = 5V
TXD						
High level input voltage	V_{IH}	2.0	-	7.0	V	
Low level input voltage	V_{IL}	-0.3	-	+0.8	V	
Hysteresis voltage	V_{hys}	0.03	-	0.50	V	
Pull-down resistor	R_{TXD}	125	350	800	kΩ	V_{TXD} = 5V
Low level input current	I_{IL}	-5.0	0.0	+5.0	μA	V_{TXD} = 0V
NSLP						
High level input voltage	V_{IH}	2.0	-	7.0	V	
Low level input voltage	V_{IL}	-0.3	-	+0.8	V	
Hysteresis voltage	V_{hys}	0.03	-	0.50	V	
Pull-down resistor	R_{NSLP}	125	350	800	kΩ	V_{NSLP} = 5V
Low level input current	I_{IL}	-5.0	0.0	+5.0	μA	V_{NSLP} = 0V
RXD (open-drain)						
Low level output current	I_{OL}	1.3	3.5	-	mA	Normal mode. V_{LIN} = 0V V_{RXD} = 0.4V
High level leakage current	I_{OZH}	-5.0	0.0	+5.0	μA	Normal mode. V_{LIN} = V_{BAT} V_{RXD} = 5V

(Note 1) When V_{BAT} is 12V or more, add to the circuit current the value calculated by the following expression because I_{BAT} depends on pull-up resistor inside LIN terminal.

$$I_{BAT(increase)} = \frac{V_{BAT} - 12V}{20k\Omega}$$

(20kΩ is the minimum value of pull-up resistor inside LIN terminal)

Electrical Characteristics (Ta= -40 to +125°C; V_{BAT} =5 to 27V; $R_{L(LIN-BAT)}$ =500Ω; typical values are given at Ta=25°C; V_{BAT} =12V; unless otherwise specified)

Table 6. Electrical Characteristics

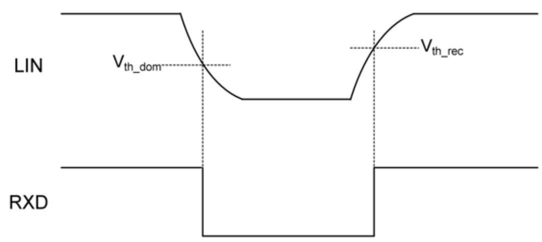
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
NWAKE						
High level input voltage	V_{IH}	V_{BAT} - 1.0	-	V_{BAT} + 0.3	V	
Low level input voltage	V_{IL}	-0.3	-	V_{BAT} - 3.3	V	
High level leakage current	I_{IH}	-5.0	0.0	+5.0	μA	V_{NWAKE} = 27V V_{BAT} = 27V
Pull-up current	I_{IL}	-30	-10	-3	μA	V_{NWAKE} = 0V
INH						
Switch-on resistance between pins BAT and INH	R_{INH}	-	30	50	Ω	Standby mode, Normal mode. I_{INH} = -15mA, V_{BAT} = 12V
High level leakage current	I_{OZH}	-5.0	0.0	+5.0	μA	Sleep mode. V_{INH} = V_{BAT} = 27V
LIN						
LIN recessive output voltage	V_{O_rec}	V_{BAT} x 0.9	-	V_{BAT}	V	V_{TXD} = 5V, I_{LIN} = 0mA
LIN dominant output voltage	V_{O_dom1}	-	-	1.2	V	V_{TXD} = 0V, V_{BAT} = 7.3V
	V_{O_dom2}	0.6	-	-	V	V_{TXD} = 0V, V_{BAT} = 7.3V $R_{L(LIN-BAT)}$ = 1kΩ
	V_{O_dom3}	-	-	2.0	V	V_{TXD} = 0V, V_{BAT} = 18V
	V_{O_dom4}	0.8	-	-	V	V_{TXD} = 0V, V_{BAT} = 18V $R_{L(LIN-BAT)}$ = 1kΩ
High level leakage current	I_{IH}	-5.0	0.0	+5.0	μA	V_{LIN} = V_{BAT}
LIN pull-up current	I_{IL}	-10.0	-5.0	-2.0	μA	Sleep mode. V_{LIN} = V_{NSLP} = 0V
Pull-up resistance (Slave termination resistance to pin BAT)	R_{SLAVE}	20	30	47	kΩ	Standby mode, Normal mode. V_{LIN} = 0V, V_{BAT} = 12V
Capacitance of pin LIN	C_{LIN}	-	-	250	pF	
Short-circuit output current	I_{O_SC0}	40	-	200	mA	V_{LIN} = V_{BAT} = 18V, V_{TXD} = 0V t < t_{dom}
Input leakage current at the receiver operating (included pull-up resistor)	$I_{BUS\_PAS\_dom}$	-1	-	-	mA	V_{LIN} = 0V V_{BAT} = 12V V_{TXD} = 5V
Input leakage current at the receiver operating	$I_{BUS\_PAS\_rec}$	-	-	20	μA	V_{LIN} = 18V V_{BAT} = 8V V_{TXD} = 5V
Loss of ground leakage current	$I_{BUS\_NO\_GND}$	-1	-	1	mA	V_{BAT} = V_{GND} = 12V V_{LIN} = 0V to 18V
Loss of battery leakage current	$I_{BUS\_NO\_BAT}$	-	-	100	μA	V_{BAT} = 0V V_{LIN} = 18V
Receiver threshold voltage	V_{th_rx}	V_{BAT} x 0.4	-	V_{BAT} x 0.6	V	V_{BAT} = 7.3V to 27.0V
Receiver center voltage (Note 2)	V_{cn_rx}	V_{BAT} x 0.475	V_{BAT} x 0.500	V_{BAT} x 0.525	V	V_{BAT} = 7.3V to 27.0V V_{cn_rx} = (V_{th_dom} + V_{th_rec})/2
Receiver threshold hysteresis voltage (Note 2)	V_{th_hys}	V_{BAT} x 0.100	V_{BAT} x 0.140	V_{BAT} x 0.175	V	V_{BAT} = 7.3V to 27.0V V_{th_hys} = V_{th_rec} - V_{th_dom}

Electrical Characteristics (Ta= -40 to +125°C; V_{BAT} =5 to 27V; $R_{L(LIN-BAT)}$ =500Ω; typical values are given at Ta=25°C; V_{BAT} =12V; unless otherwise specified)

Table 7. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AC characteristics (Note 6)						
RXD propagation delay	$t_{PropRxDom}$	-	-	6.0	μs	Normal mode $C_{L(LIN-GND)}$ = 0nF $R_{L(LIN-BAT)}$ = ∞ Voltage on LIN externally forced. LIN t_f, t_r < 20ns C_{RXD} = 20pF R_{RXD} = 2.4kΩ $\Delta t_{d\_(BUS-RXD)}$= $t_{PropRxDom}$-$t_{PropRxRec}$
	$t_{PropRxRec}$	-	-	6.0	μs	
RXD propagation delay failure	$\Delta t_{d\_(BUS-RXD)}$	-2.0	0.0	+2.0	μs	
Duty cycle 1 (Note 3, Note 4)	D1	0.396	-	-		Normal mode $TH_{Rec(max)}$ = 0.744 x V_{BAT} $TH_{Dom(max)}$ = 0.581 x V_{BAT} V_{BAT}=7.0 to 18.0V t_{Bit}=50μs
Duty cycle 2 (Note 3, Note 5)	D2	-	-	0.581		Normal mode $TH_{Rec(min)}$ = 0.422 x V_{BAT} $TH_{Dom(min)}$ = 0.284 x V_{BAT} V_{BAT}=7.6 to 18.0V t_{Bit}=50μs
Duty cycle 3 (Note 3, Note 4)	D3	0.417	-	-		Normal mode $TH_{Rec(max)}$ = 0.778 x V_{BAT} $TH_{Dom(max)}$ = 0.616 x V_{BAT} V_{BAT}=7.0 to 18.0V t_{Bit}=96μs
Duty cycle 4 (Note 3, Note 5)	D4	-	-	0.590		Normal mode $TH_{Rec(min)}$ = 0.389 x V_{BAT} $TH_{Dom(min)}$ = 0.251 x V_{BAT} V_{BAT}=7.6 to 18.0V t_{Bit}=96μs
Dominant time for wake-up via bus	t_{BUS}	30	70	150	μs	Sleep mode (Remote wake-up)
Dominant time for wake-up via pin NWAKE	t_{NWAKE}	7	20	50	μs	Sleep mode (Local wake-up)
Time period for mode change from sleep or standby mode into normal mode	$t_{gotonorm}$	2	5	10	μs	Shift from Sleep/Standby mode to Normal mode
Time period for mode change from normal mode into sleep mode	$t_{gotosleep}$	2	5	10	μs	Shift from Normal mode to Sleep mode
TXD dominant time out	t_{dom}	6	12	20	ms	V_{TXD} = 0V

(Note 2)



(Note 3) Load condition at bus ($C_{L(LIN-GND)}$;$R_{L(LIN-BAT)}$) : 1nF;1kΩ / 6.8nF;660Ω / 10nF;500Ω

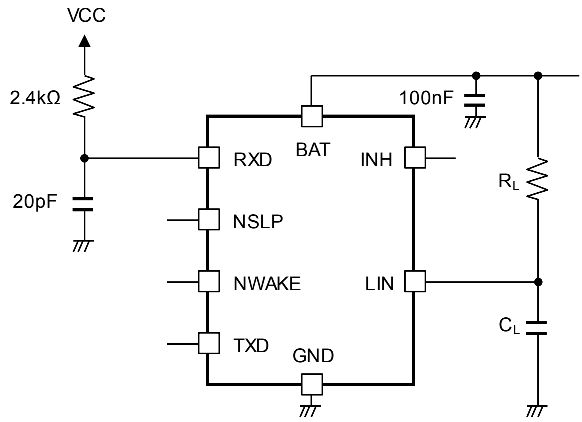
(Note 4)

$$D1, D3 = \frac{t_{\mathrm{Bus\_rec\,(min)}}}{2x t_{\mathrm{Bit}}}$$

(Note 5)

$$D2, D4 = \frac{t_{\mathrm{Bus\_rec\,(max)}}}{2x t_{\mathrm{Bit}}}$$

(Note 6) AC characteristic evaluation circuit diagram



Typical Performance Curves

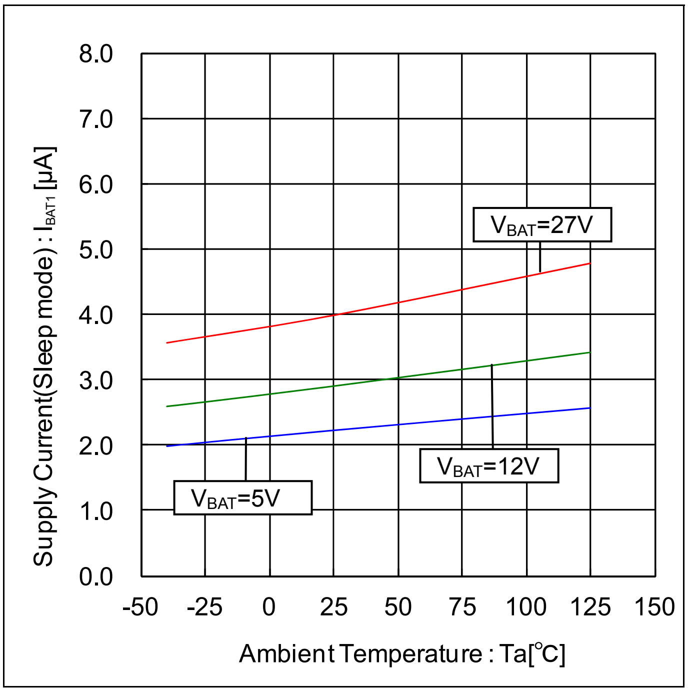


Figure 5. Supply Current(Sleep mode)- temperature characteristic

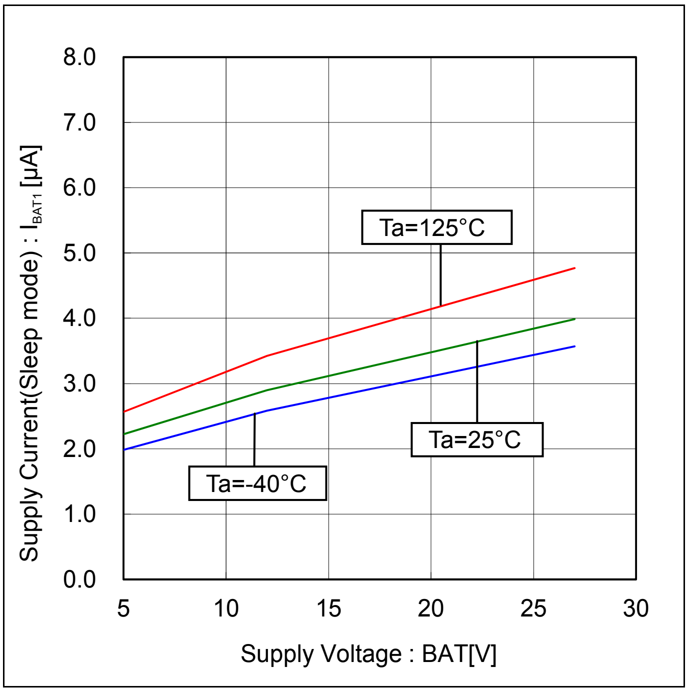


Figure 6. Supply Current(Sleep mode)- voltage characteristic

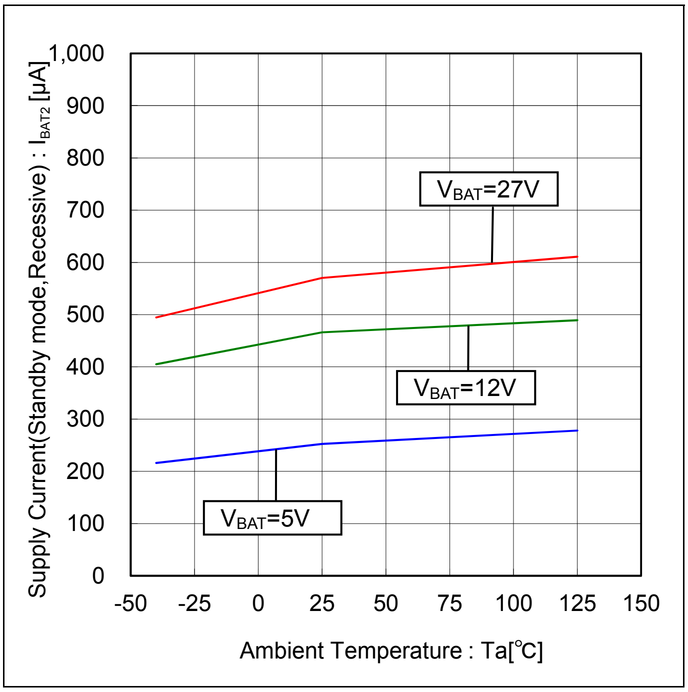


Figure 7. Supply Current(Standby mode, Recessive)- temperature characteristic

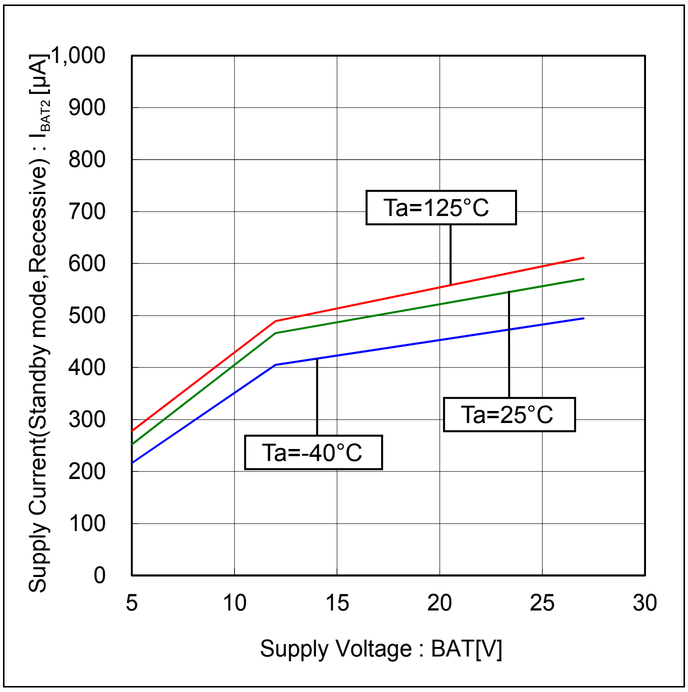


Figure 8. Supply Current(Standby mode, Recessive)- voltage characteristic

Typical Performance Curves - continued

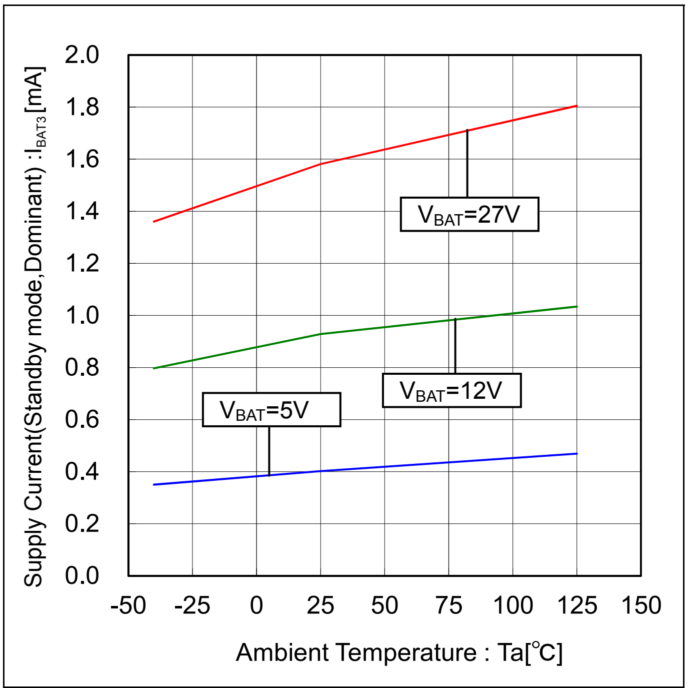


Figure 9. Supply Current(Standby mode, Dominant)- temperature characteristic

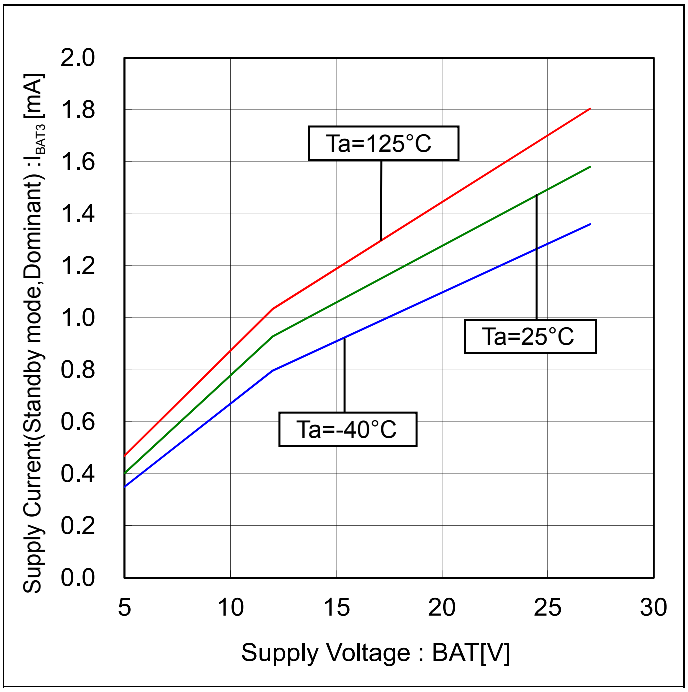


Figure 10. Supply Current(Standby mode, Dominant)- voltage characteristic

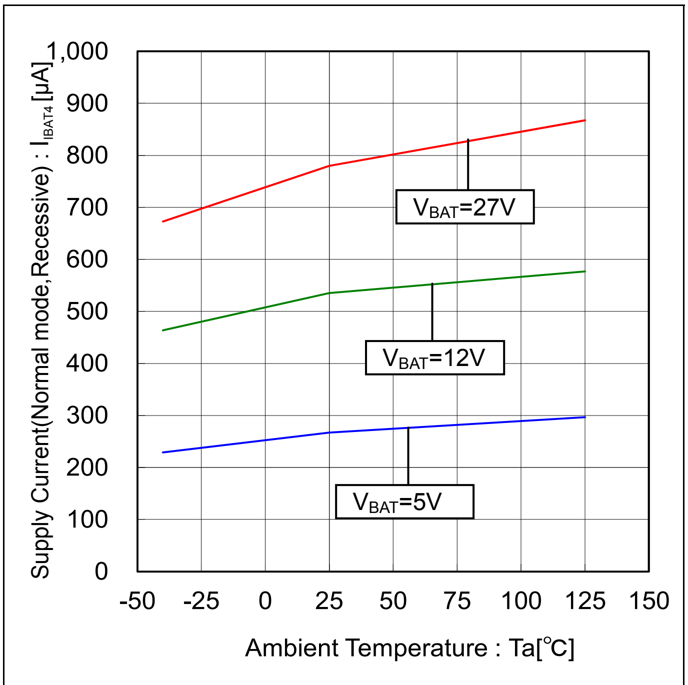


Figure 11. Supply Current(Normal mode, Recessive)- temperature characteristic

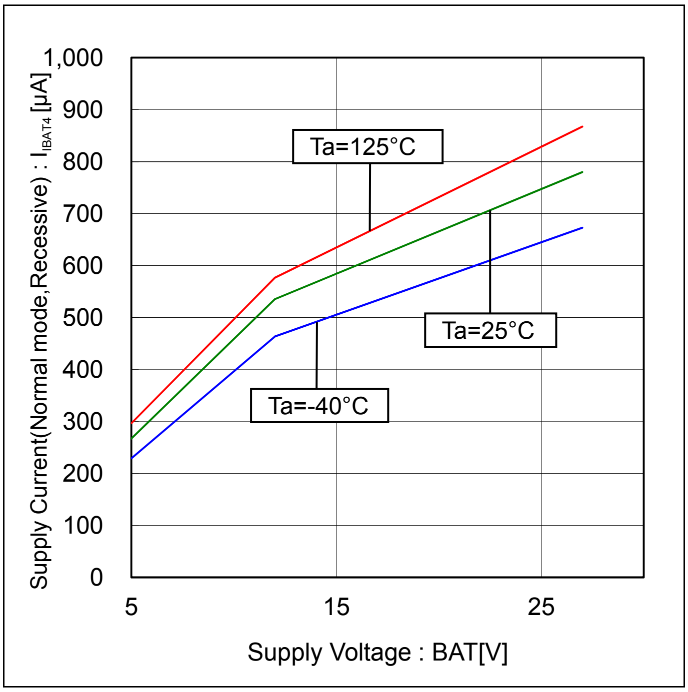


Figure 12. Supply Current(Normal mode, Recessive)- voltage characteristic

Typical Performance Curves - continued

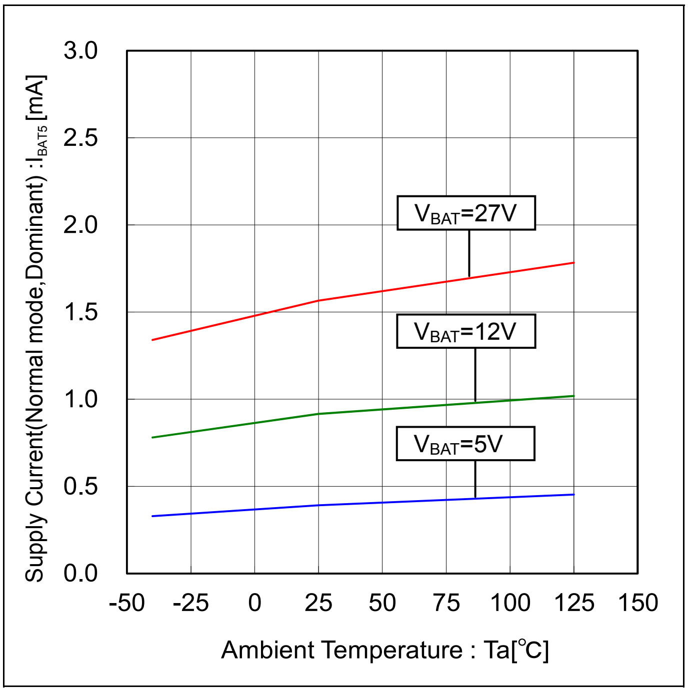


Figure 13. Supply Current(Normal mode, Dominant)- temperature characteristic

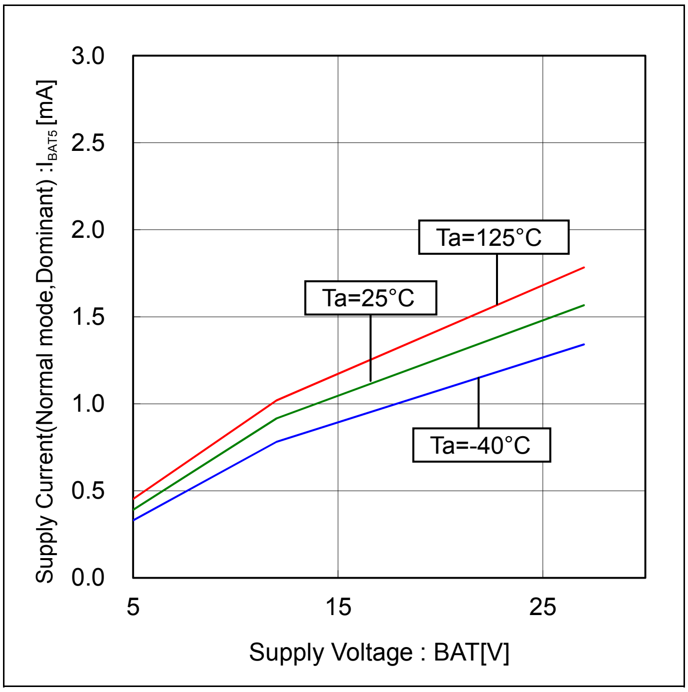


Figure 14. Supply Current(Normal mode, Dominant) - voltage characteristic

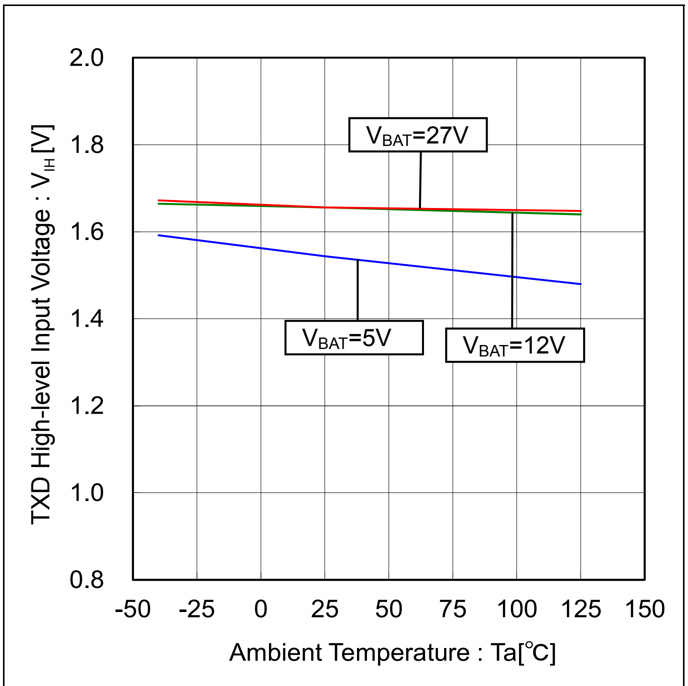


Figure 15. TXD High-level Input Voltage- temperature characteristic

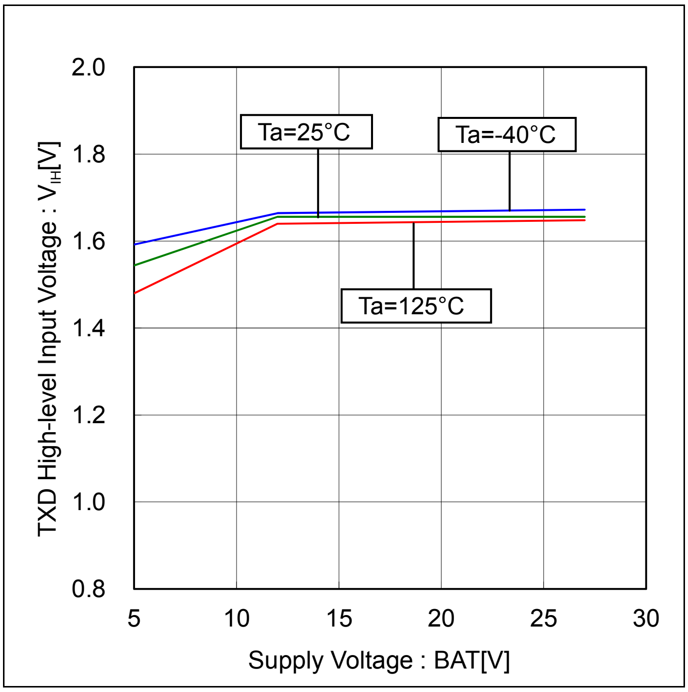


Figure 16. TXD High-level Input Voltage- voltage characteristic

Typical Performance Curves - continued

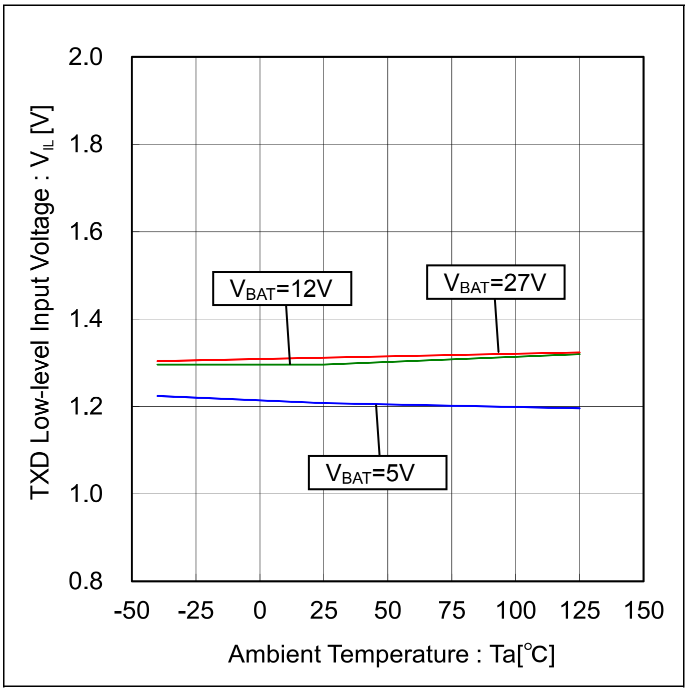


Figure 17. TXD Low-level Input Voltage- temperature characteristic

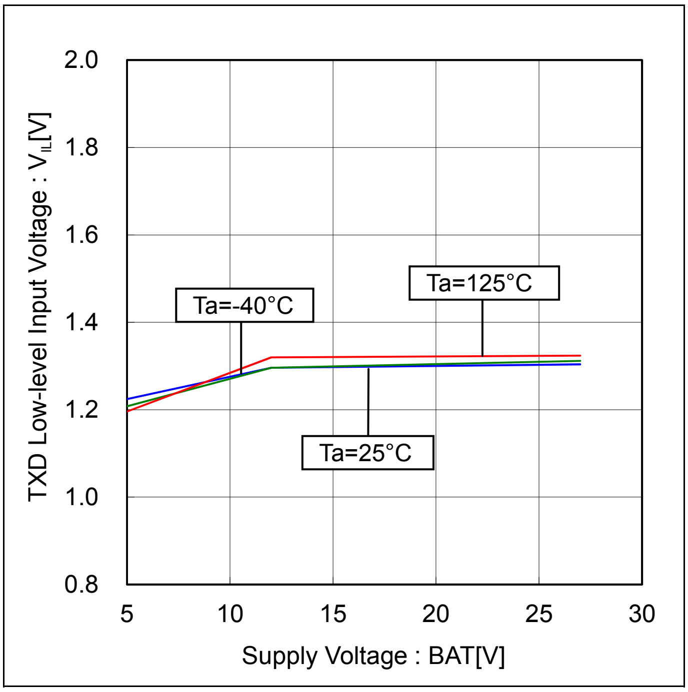


Figure 18. TXD Low-level Input Voltage- voltage characteristic

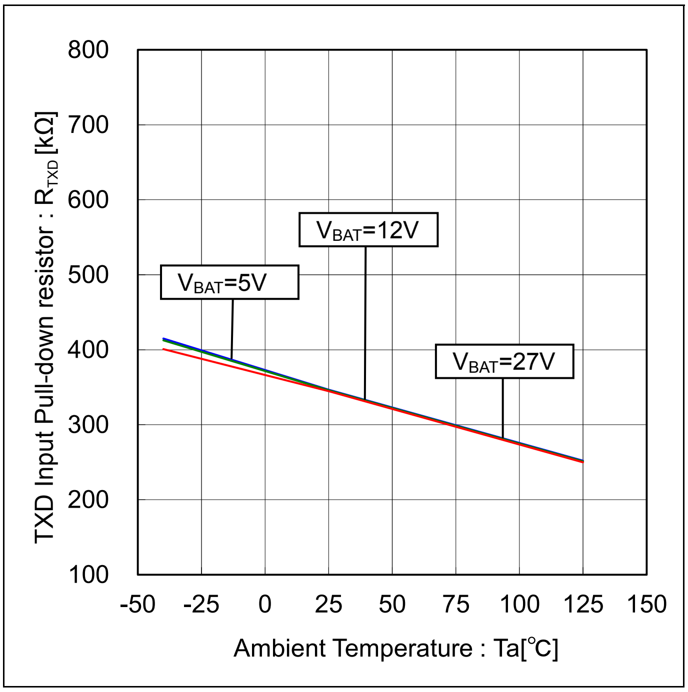


Figure 19. TXD Input Pull-down resistor- temperature characteristic

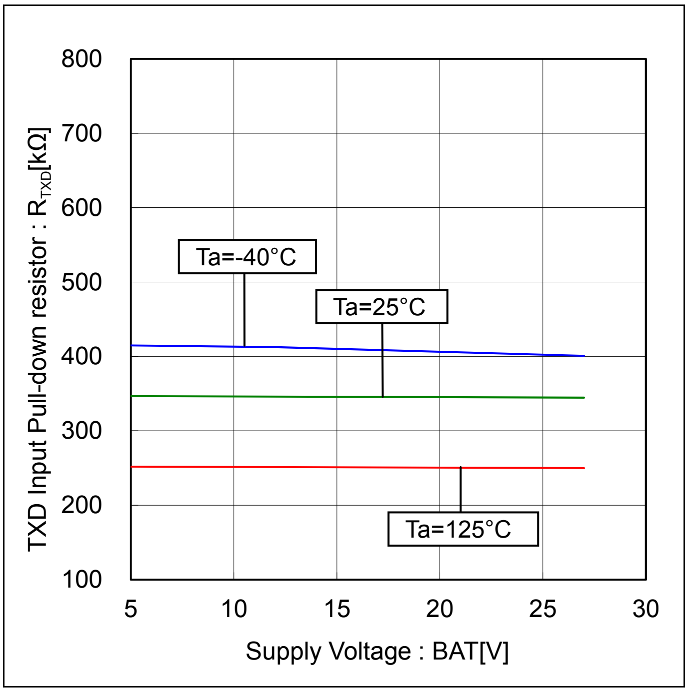


Figure 20. TXD Input Pull-down resistor- voltage characteristic

Typical Performance Curves - continued

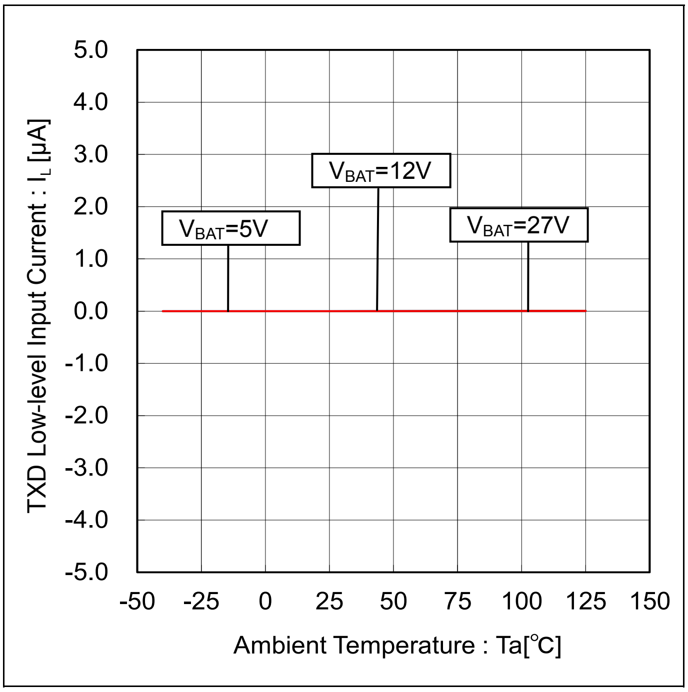


Figure 21. TXD Low-level Input Current- temperature characteristic

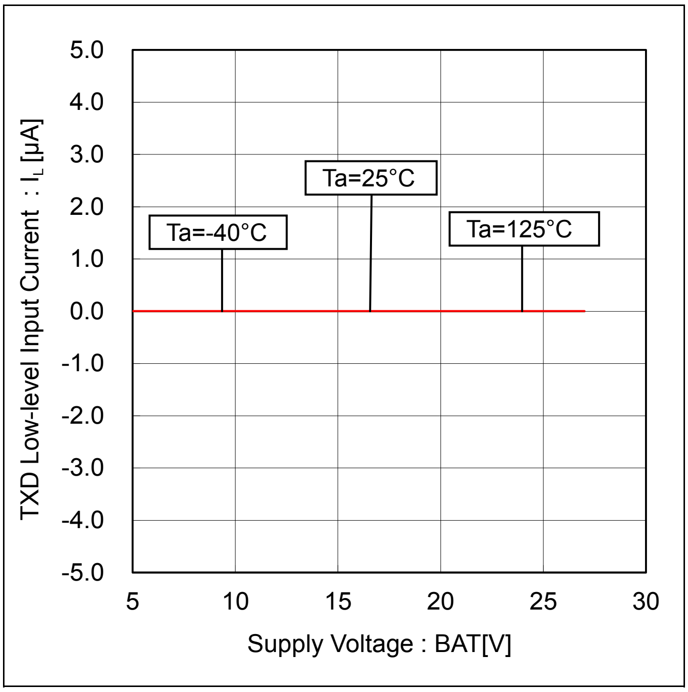


Figure 22. TXD Low-level Input Current- voltage characteristic

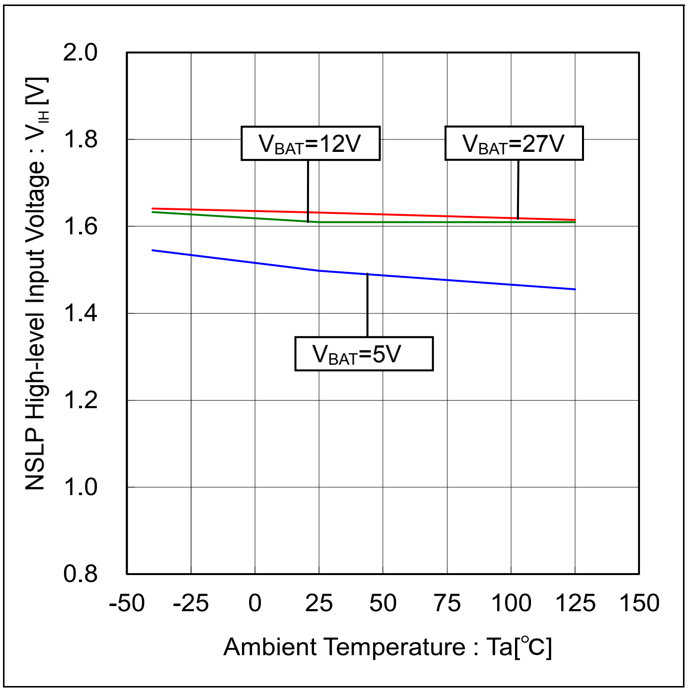


Figure 23. NSLP High-level Input Voltage- temperature characteristic

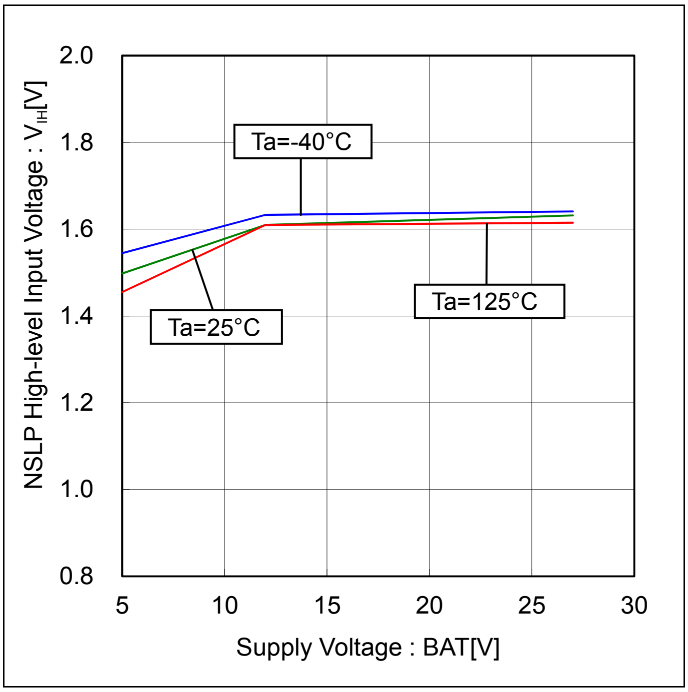


Figure 24. NSLP High-level Input Voltage- voltage characteristic

Typical Performance Curves - continued

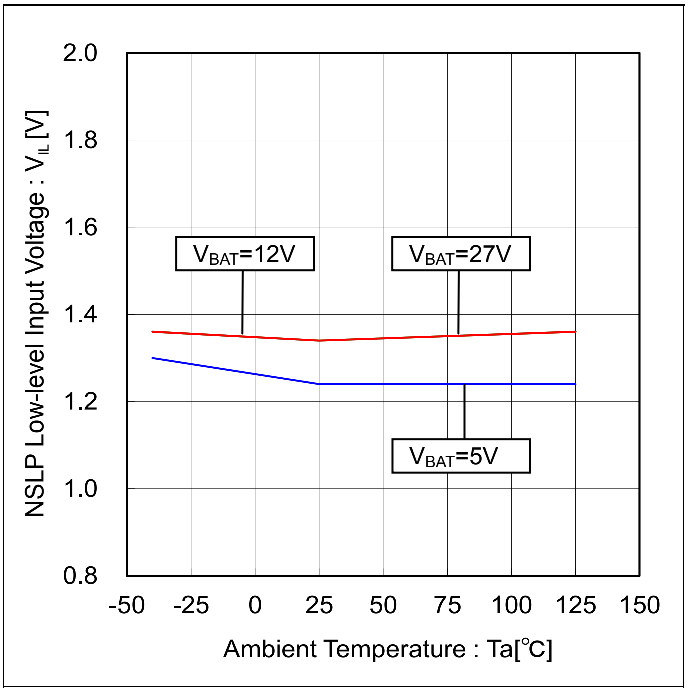


Figure 25. NSLP Low-level Input Voltage- temperature characteristic

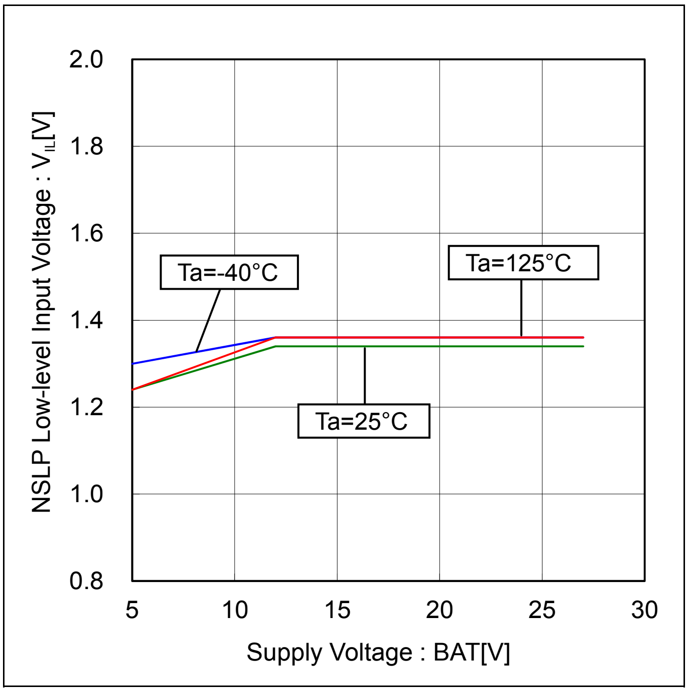


Figure 26. NSLP Low-level Input Voltage- voltage characteristic

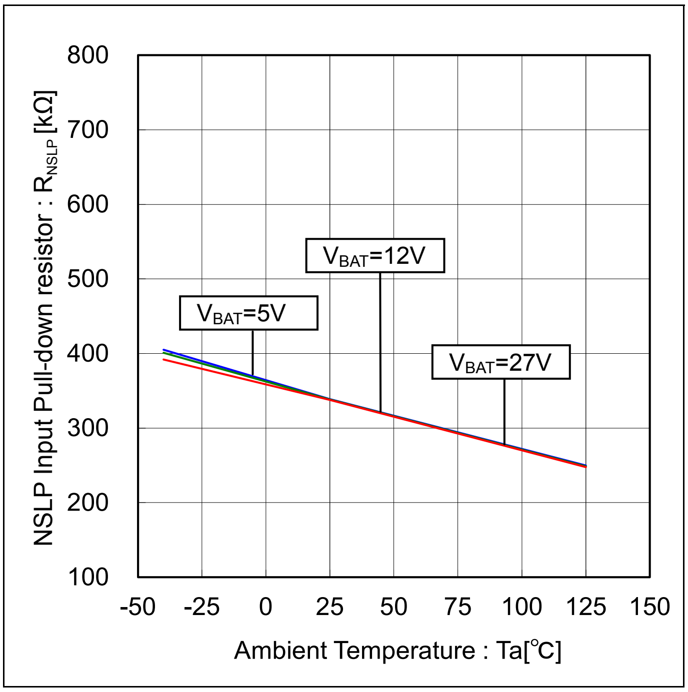


Figure 27. NSLP Input Pull-down resistor- temperature characteristic

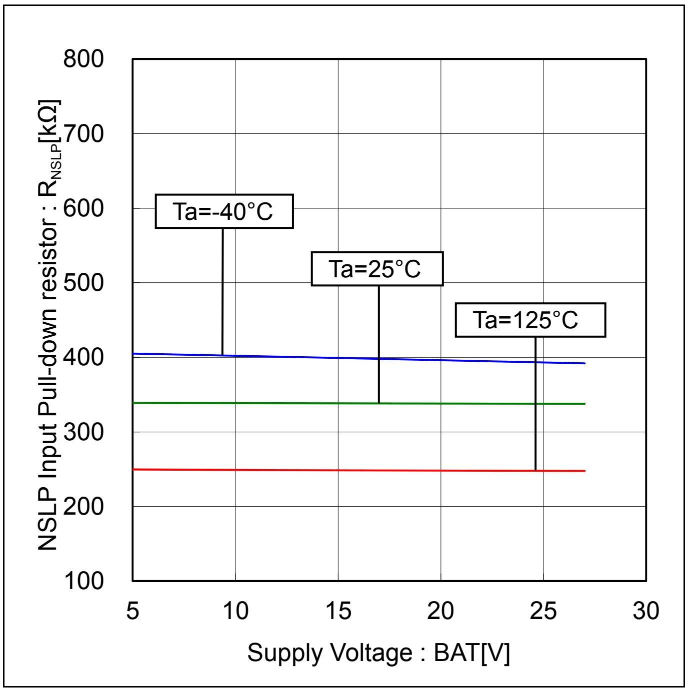


Figure 28. NSLP Input Pull-down resistor- voltage characteristic

Typical Performance Curves - continued

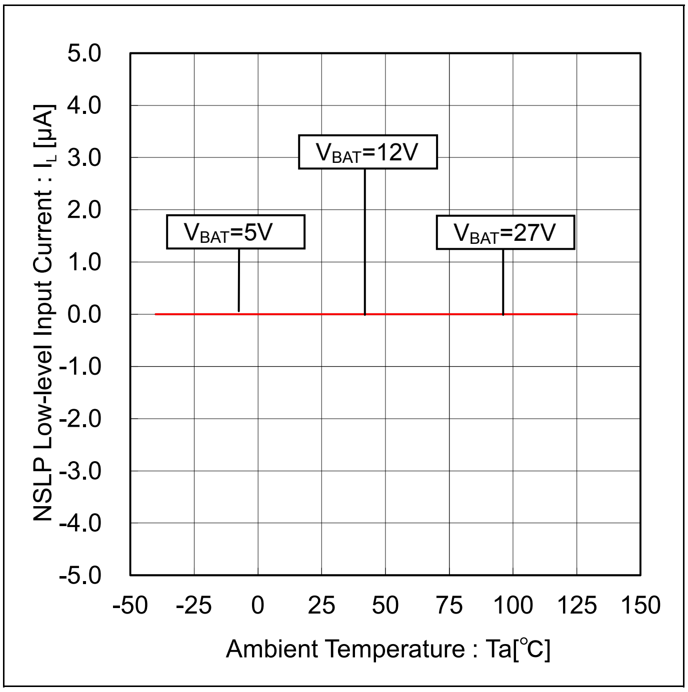


Figure 29. NSLP Low-level Input Current- temperature characteristic

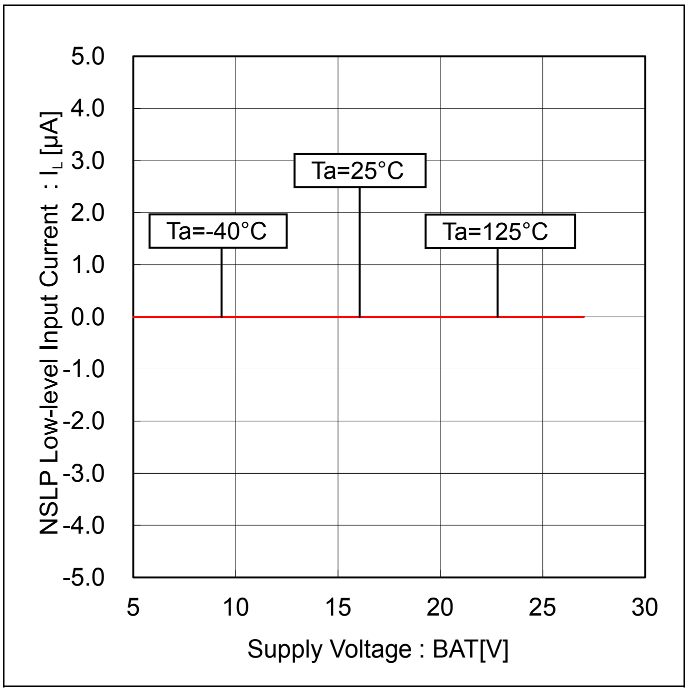


Figure 30. NSLP Low-level Input Current- voltage characteristic

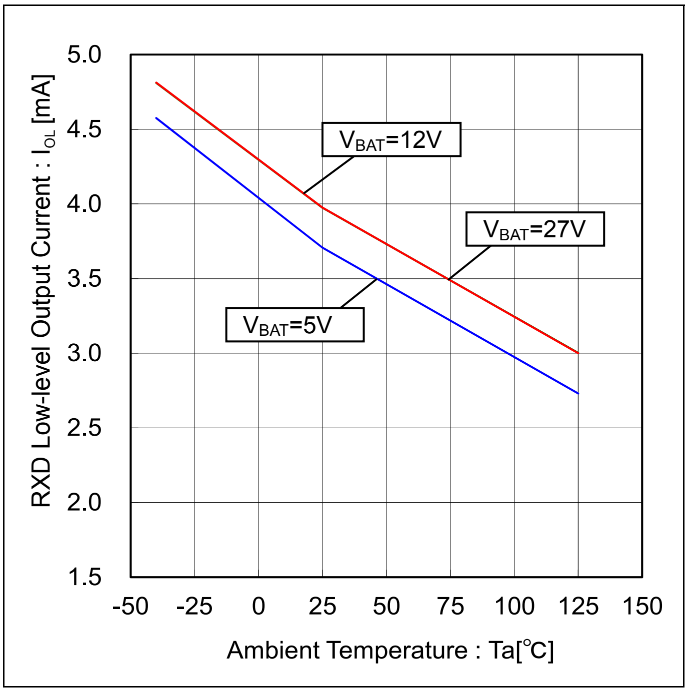


Figure 31. RXD Low-level Output Current- temperature characteristic

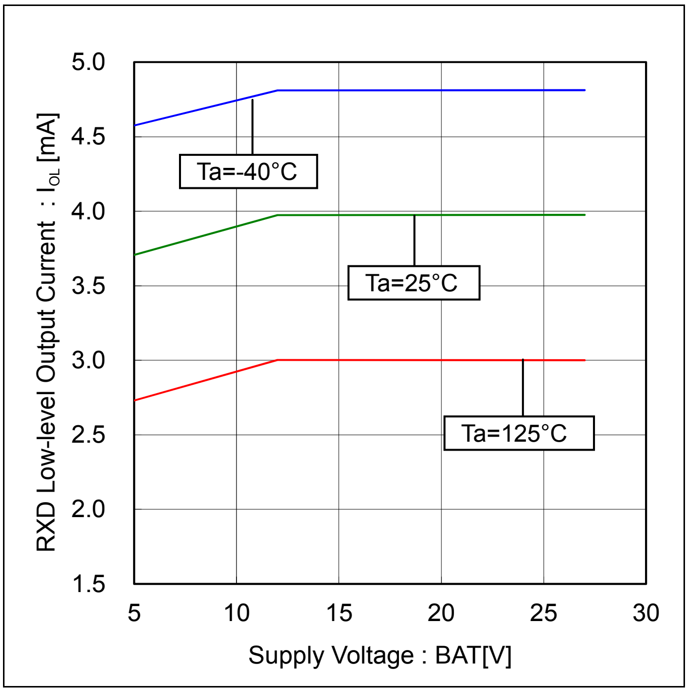


Figure 32. RXD Low-level Output Current- voltage characteristic

Typical Performance Curves - continued

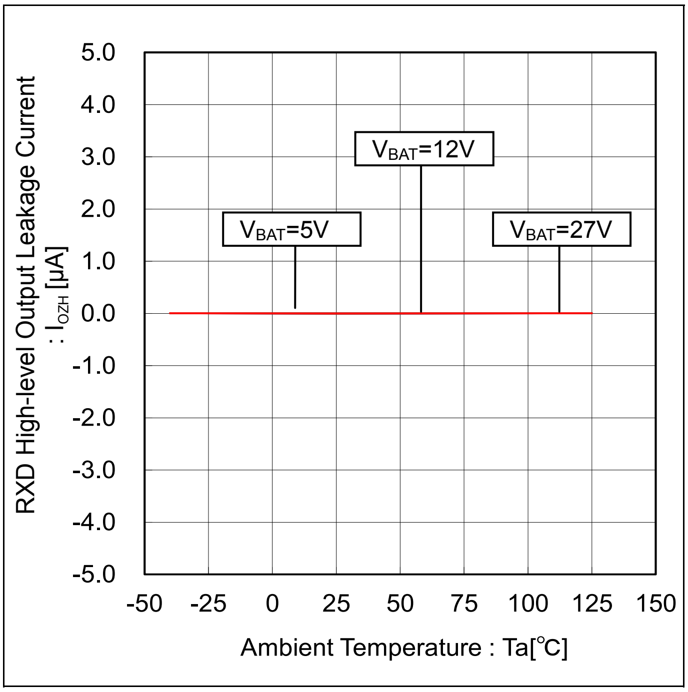


Figure 33. RXD High-level Output Leakage Current- temperature characteristic

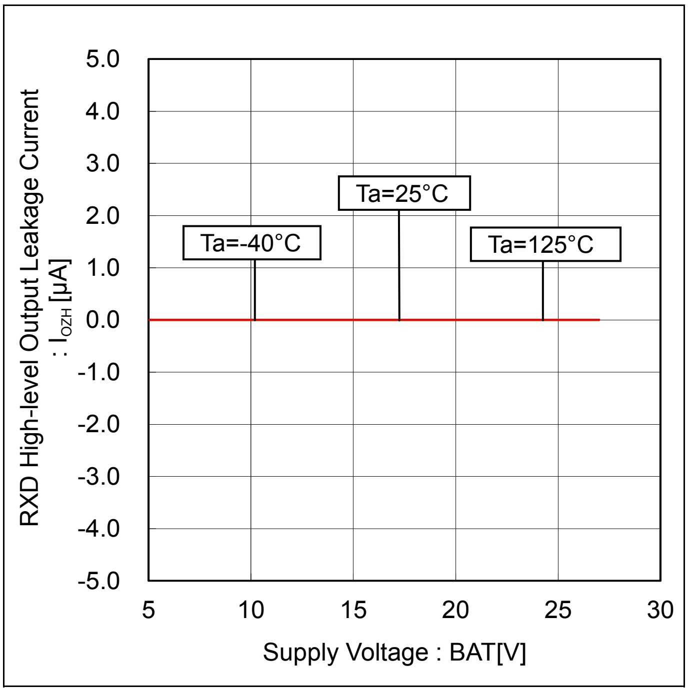


Figure 34. RXD High-level Output Leakage Current- voltage characteristic

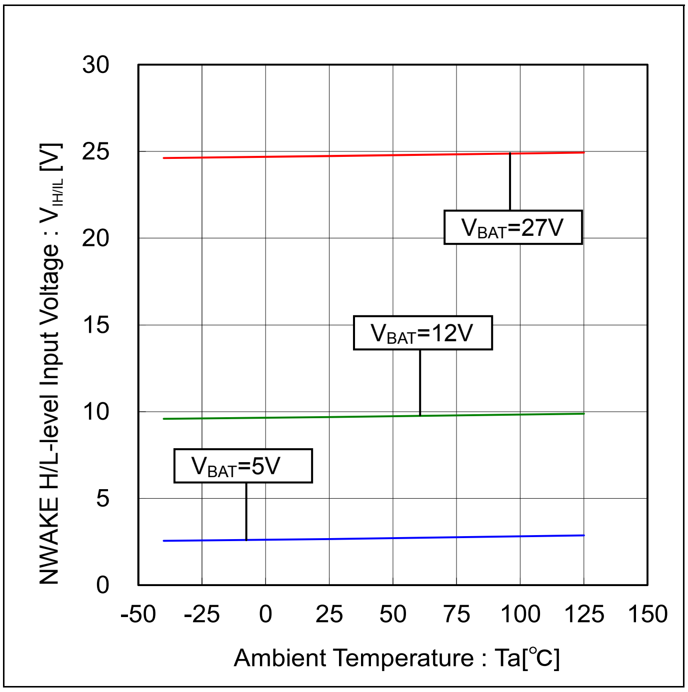


Figure 35. NWAKE H/L-level Input Voltage- temperature characteristic

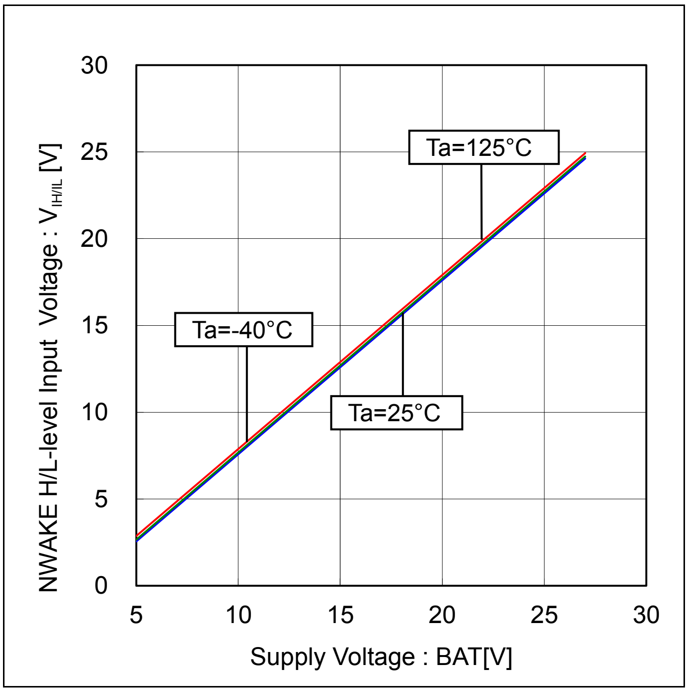


Figure 36. NWAKE H/L-level Input Voltage- voltage characteristic

Typical Performance Curves - continued

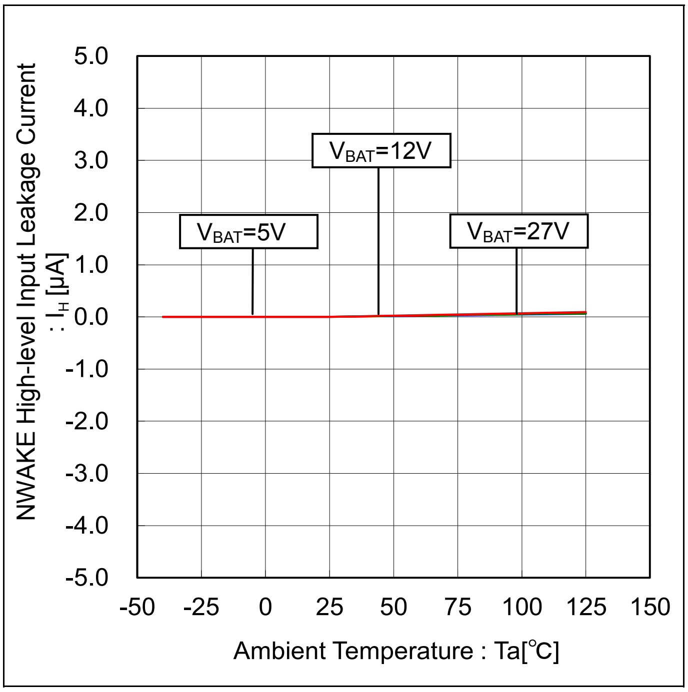


Figure 37. NWAKE High-level Input Leakage Current - temperature characteristic

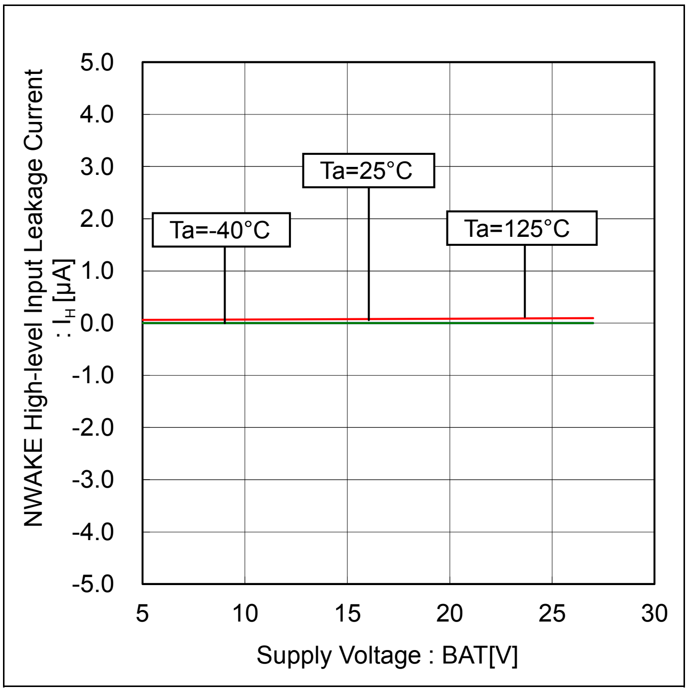


Figure 38. NWAKE High-level Input Leakage Current- voltage characteristic

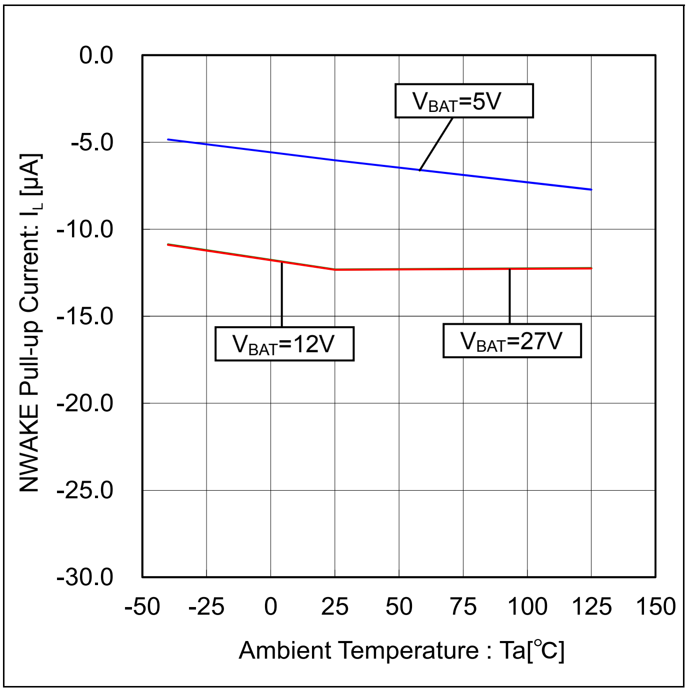


Figure 39. NWAKE Pull-up Current- temperature characteristic

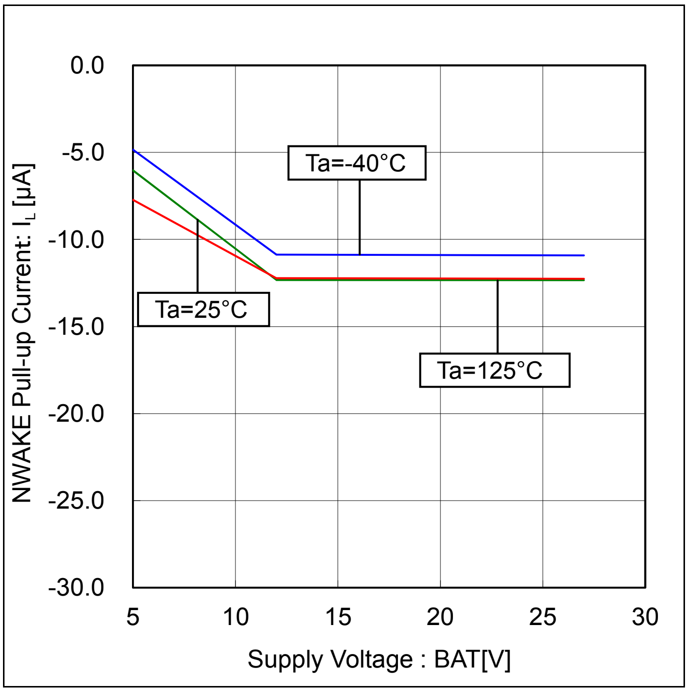


Figure 40. NWAKE Pull-up Current- voltage characteristic

Typical Performance Curves - continued

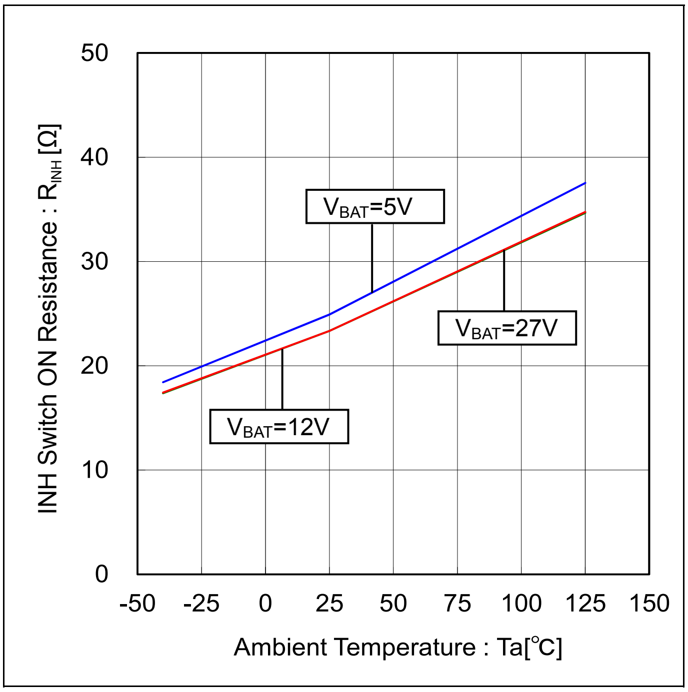


Figure 41. INH Switch ON Resistance- temperature characteristic

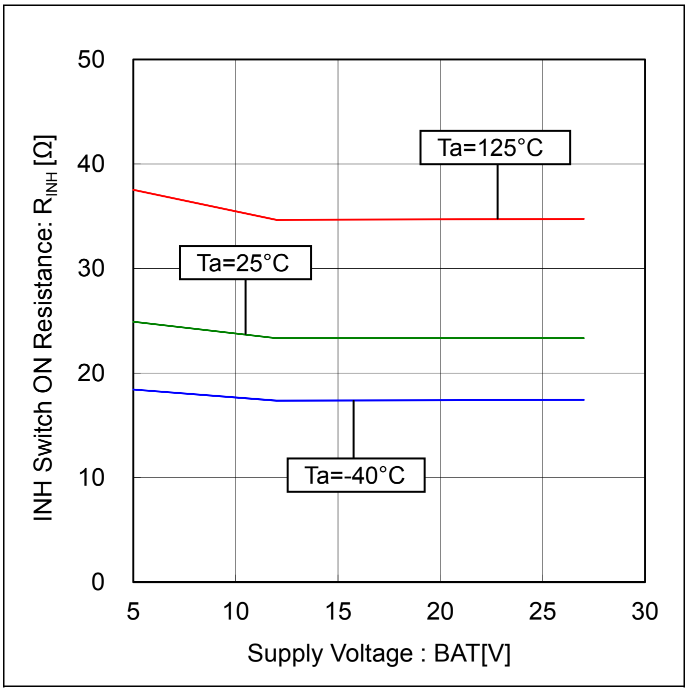


Figure 42. INH Switch ON Resistance- voltage characteristic

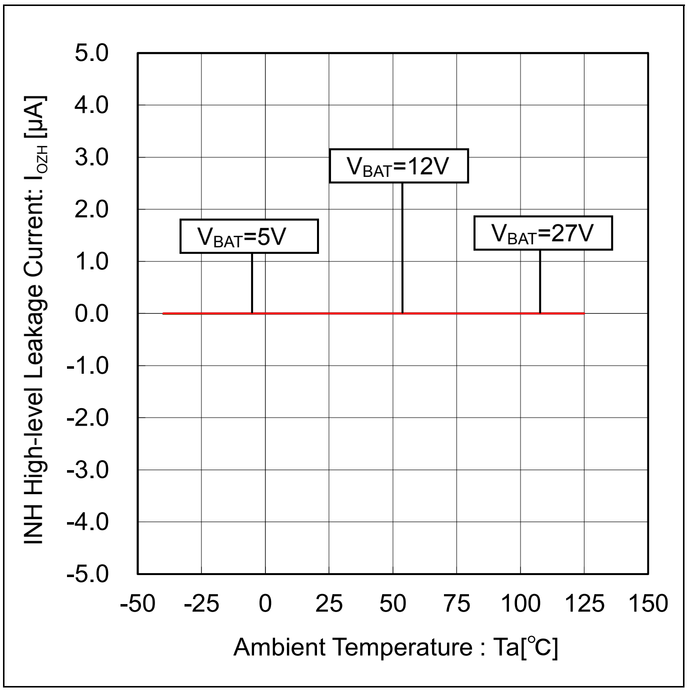


Figure 43. INH High-level Leakage Current- temperature characteristic

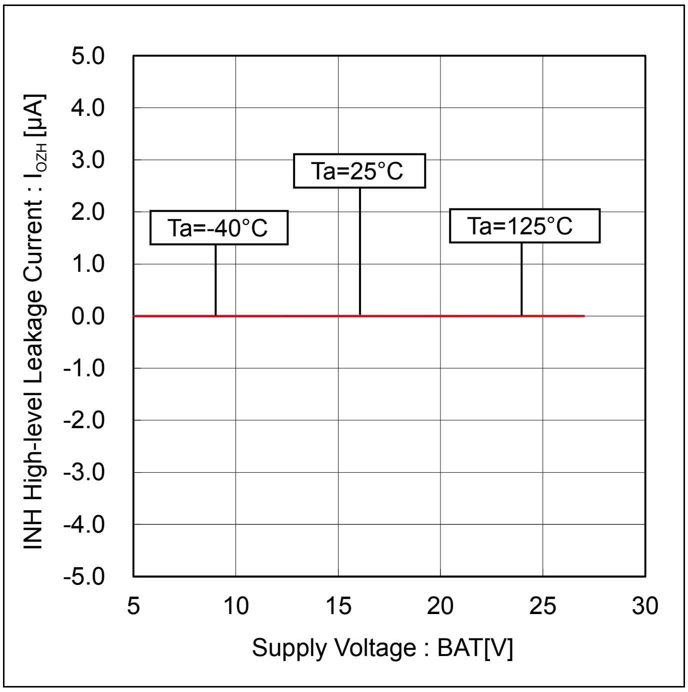


Figure 44. INH High-level Leakage Current- voltage characteristic

Typical Performance Curves - continued

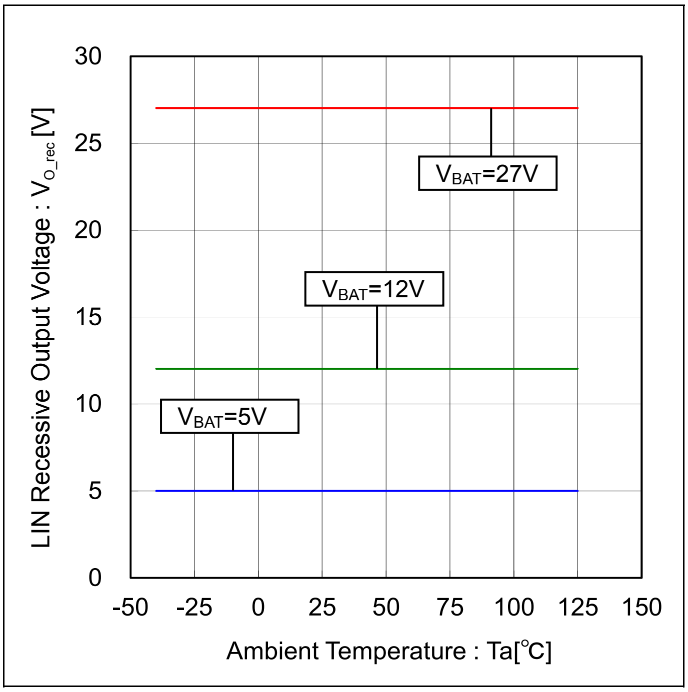


Figure 45. LIN Recessive Output Voltage- temperature characteristic

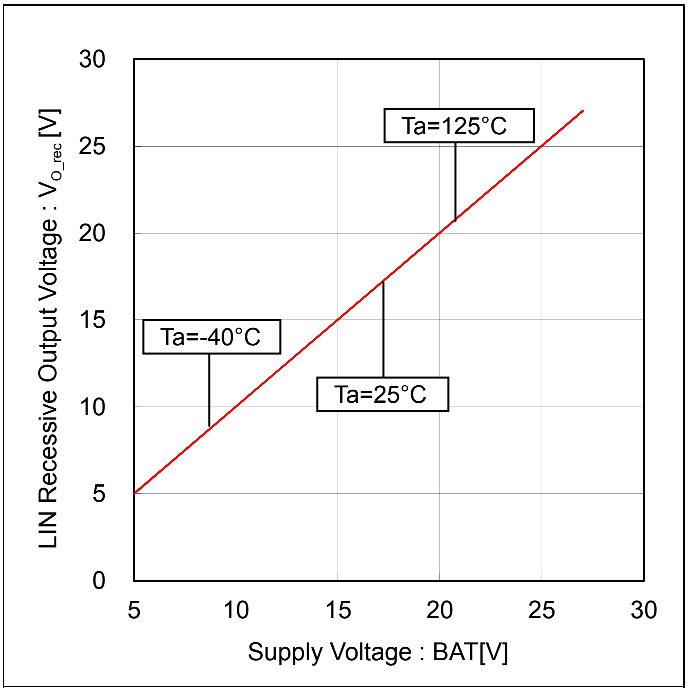


Figure 46. LIN Recessive Output Voltage- voltage characteristic

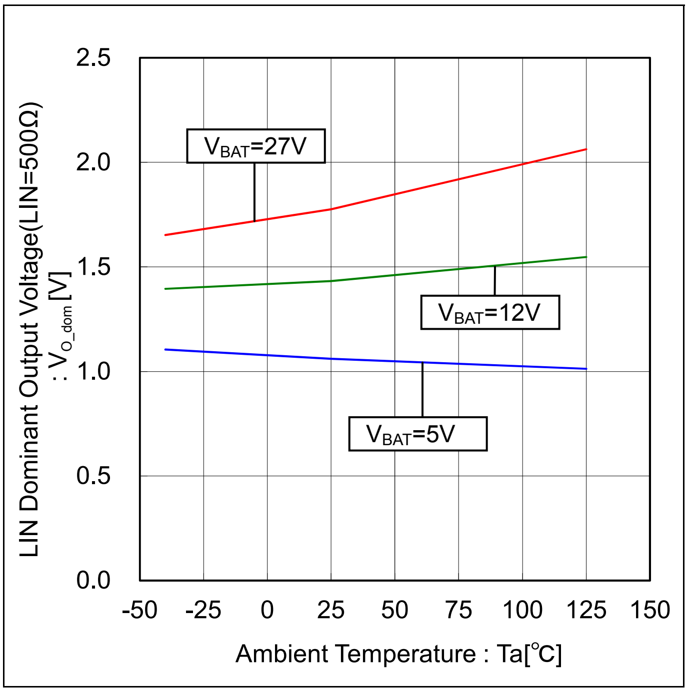


Figure 47. LIN Dominant Output Voltage(LIN=500Ω)- temperature characteristic

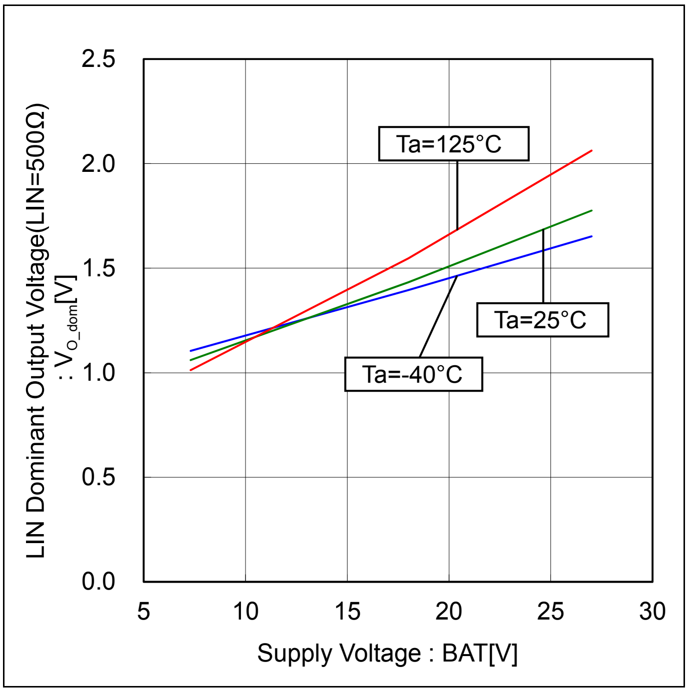


Figure 48. LIN Dominant Output Voltage(LIN=500Ω)- voltage characteristic

Typical Performance Curves - continued

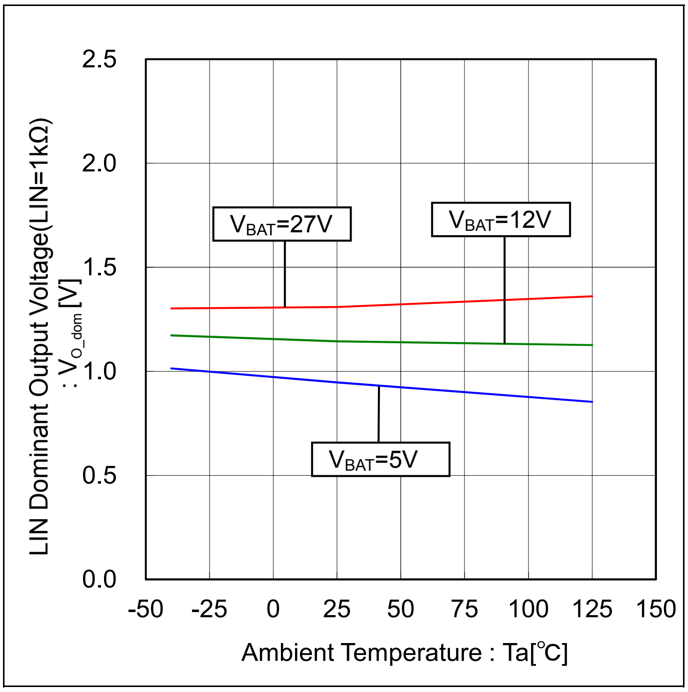


Figure 49. LIN Dominant Output Voltage(LIN=1kΩ) - temperature characteristic

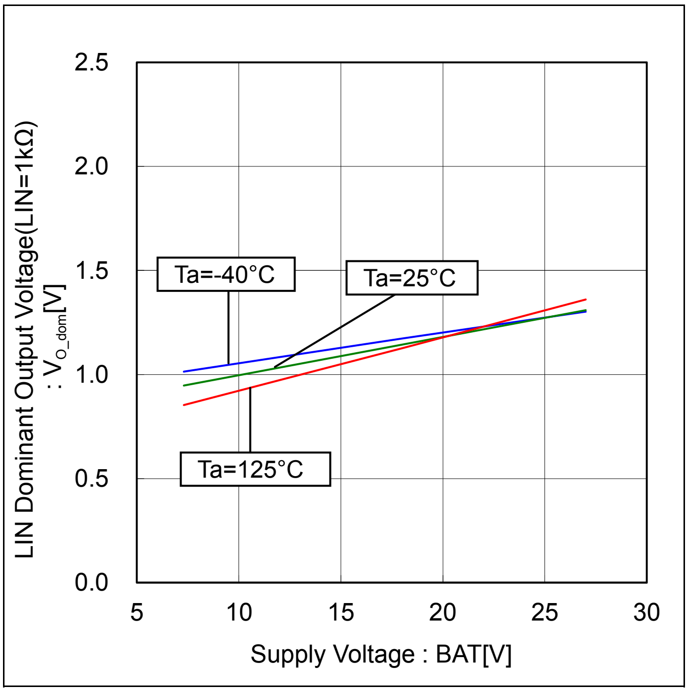


Figure 50. LIN Dominant Output Voltage(LIN=1kΩ) -voltage characteristic

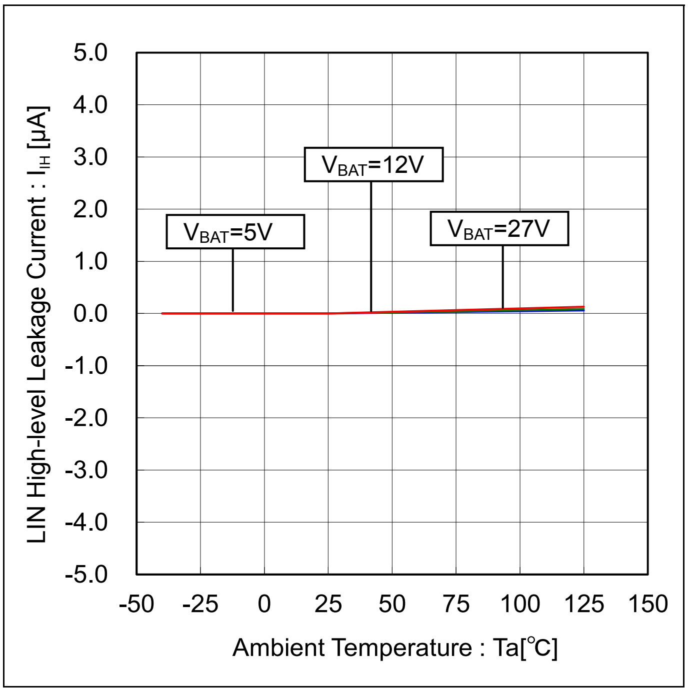


Figure 51. LIN High-level Leakage Current- temperature characteristic

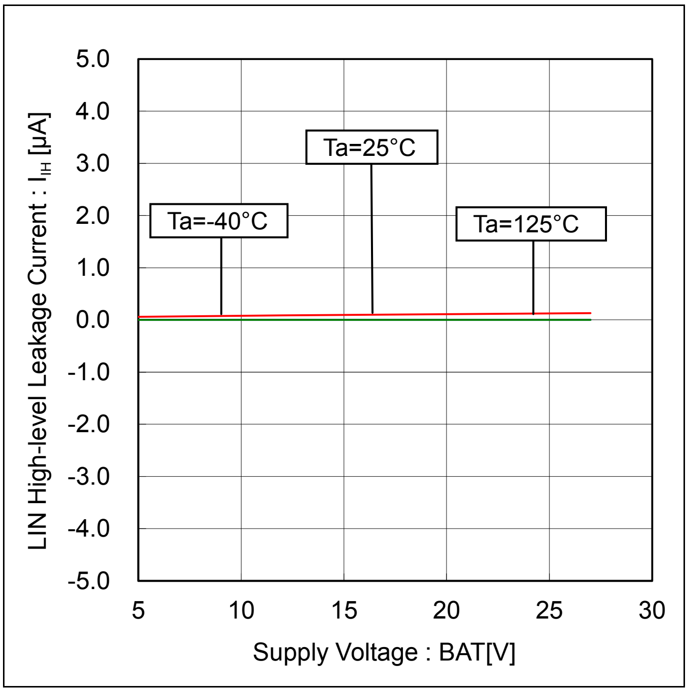


Figure 52. LIN High-level Leakage Current- voltage characteristic

Typical Performance Curves - continued

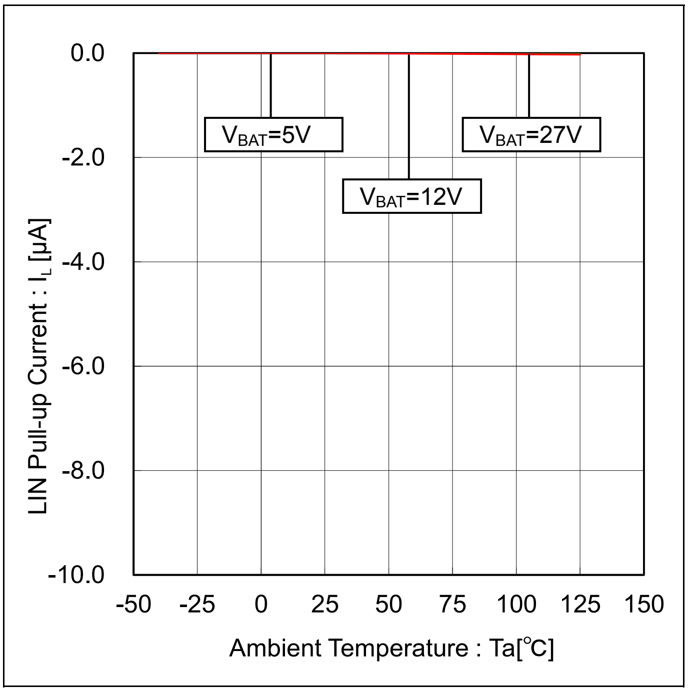


Figure 53. LIN Pull-up Current- temperature characteristic

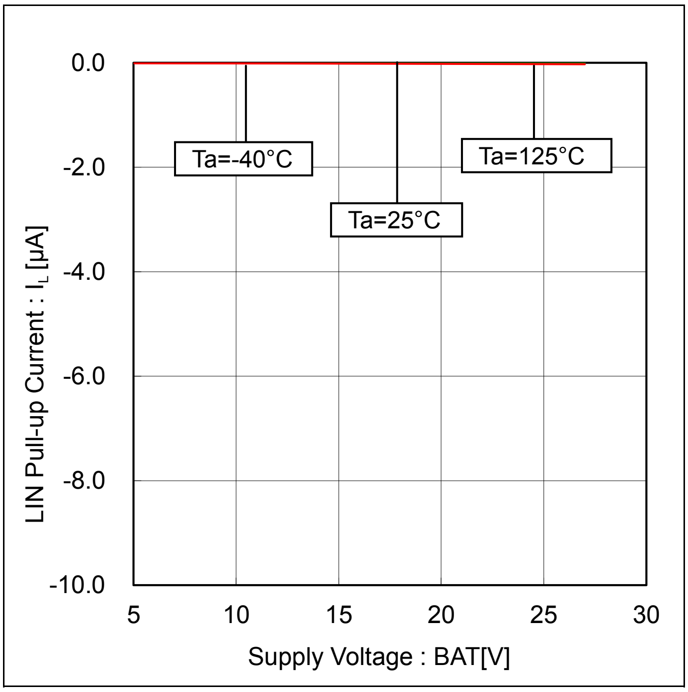


Figure 54. LIN Pull-up Current- voltage characteristic

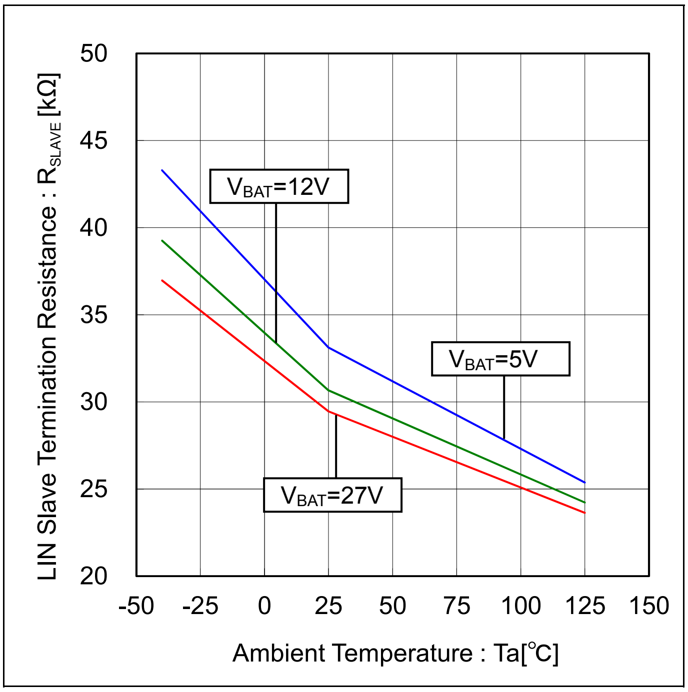


Figure 55. LIN Slave Termination Resistance- temperature characteristic

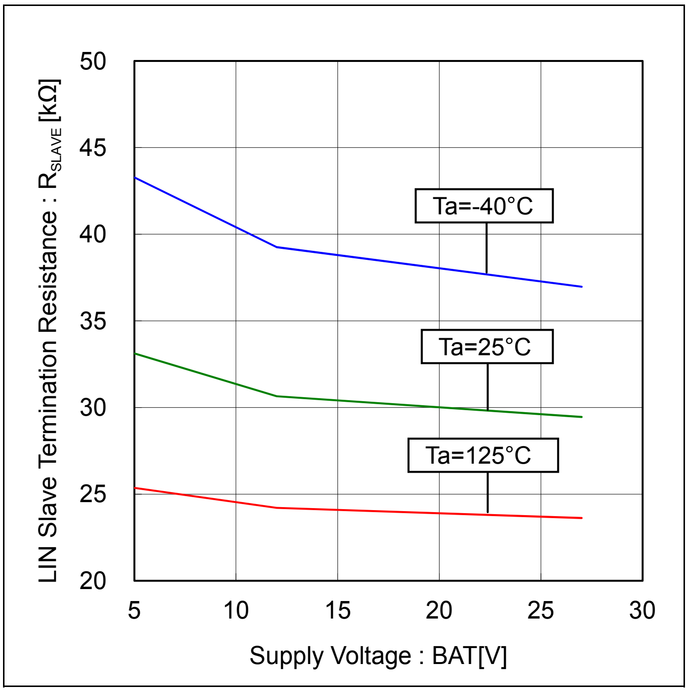


Figure 56. LIN Slave Termination Resistance- voltage characteristic

Typical Performance Curves - continued

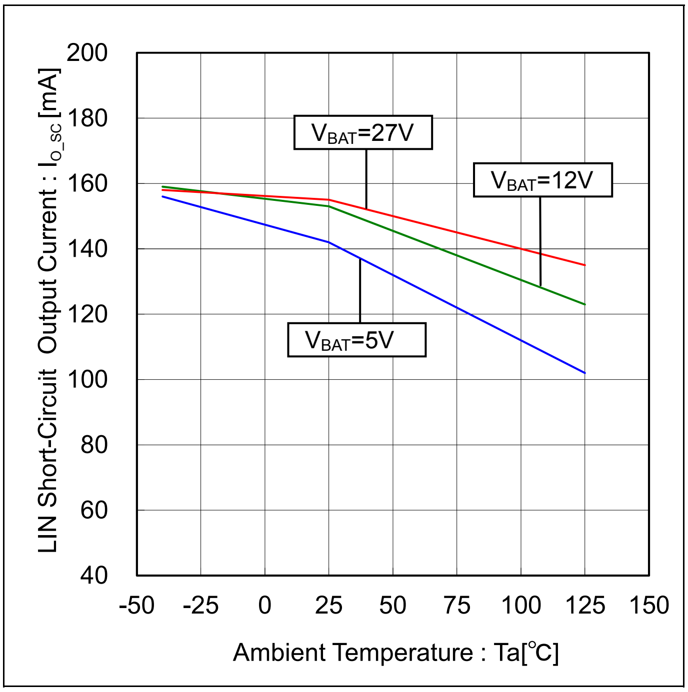


Figure 57. LIN Short-Circuit Output Current- temperature characteristic

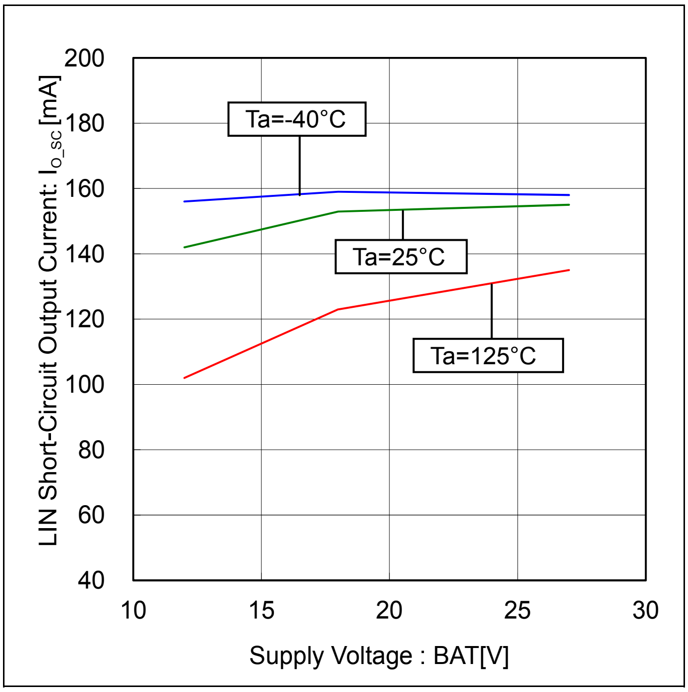


Figure 58. LIN Short-Circuit Output Current- voltage characteristic

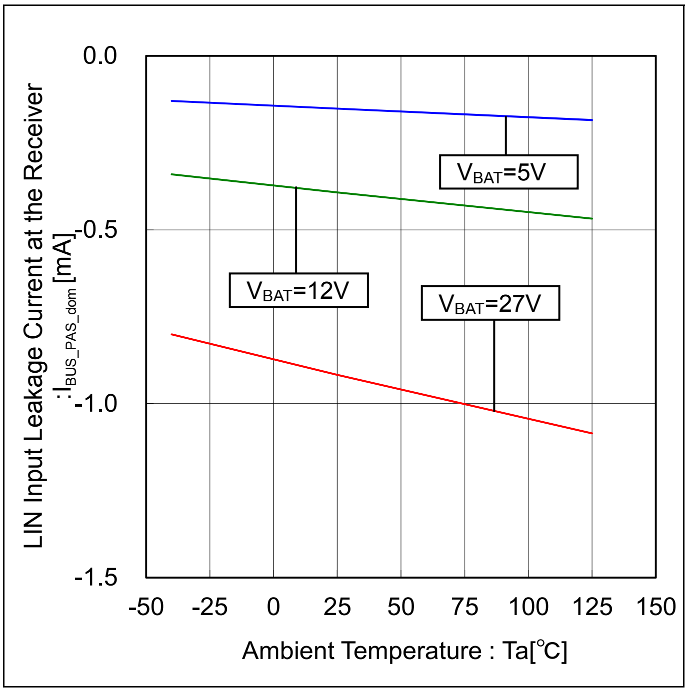


Figure 59. LIN Input Leakage Current at the Receiver- temperature characteristic

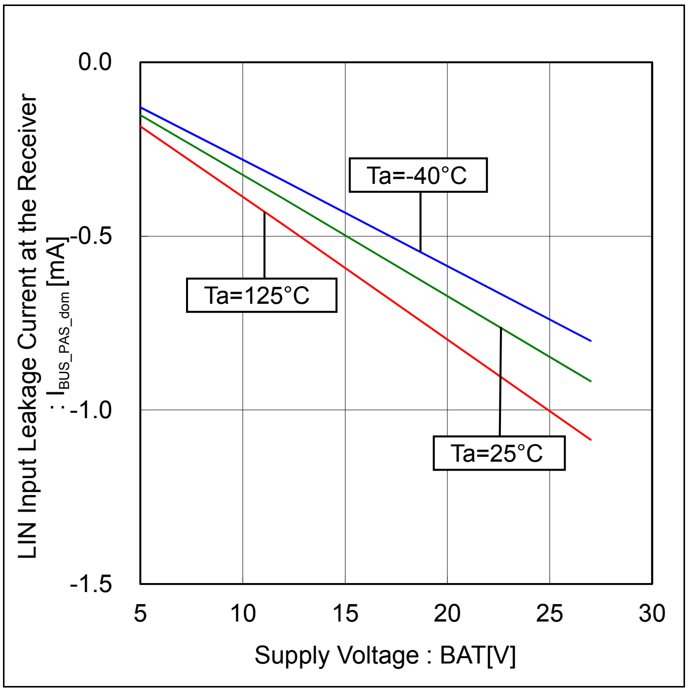


Figure 60. LIN Input Leakage Current at the Receiver- voltage characteristic

Typical Performance Curves - continued

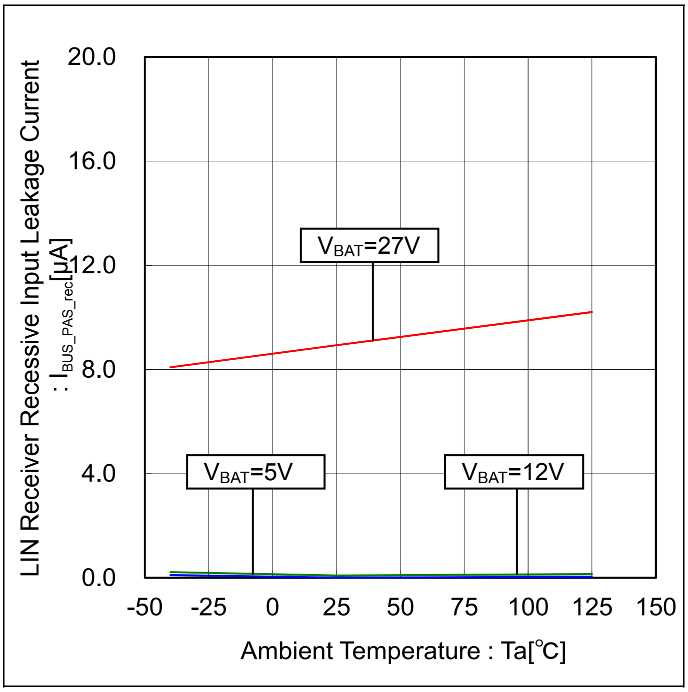


Figure 61. LIN Receiver Recessive Input Leakage Current-temperature characteristic

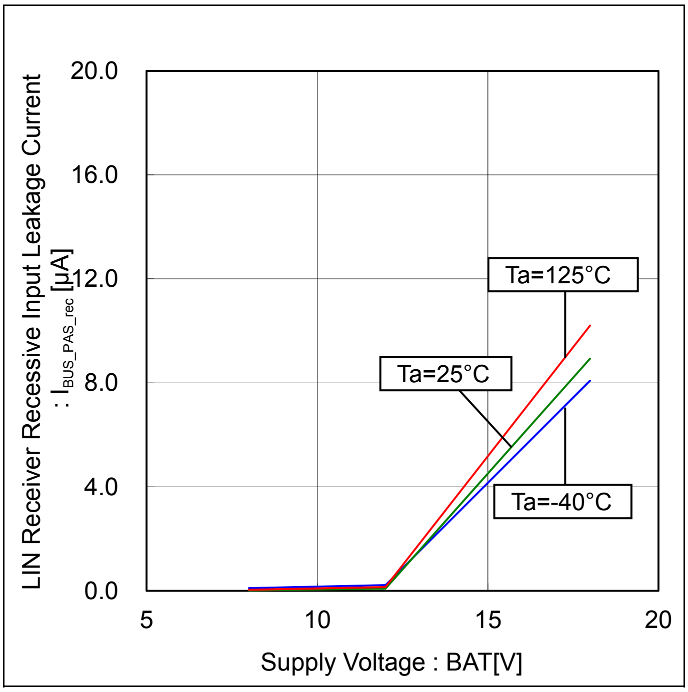


Figure 62. LIN Receiver Recessive Input Leakage Current-voltage characteristic

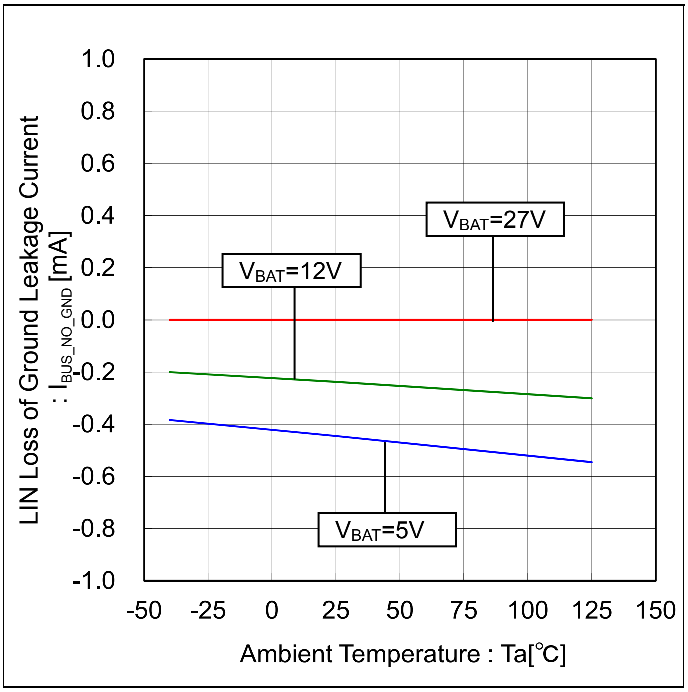


Figure 63. LIN Loss of Ground Leakage Current-temperature characteristic

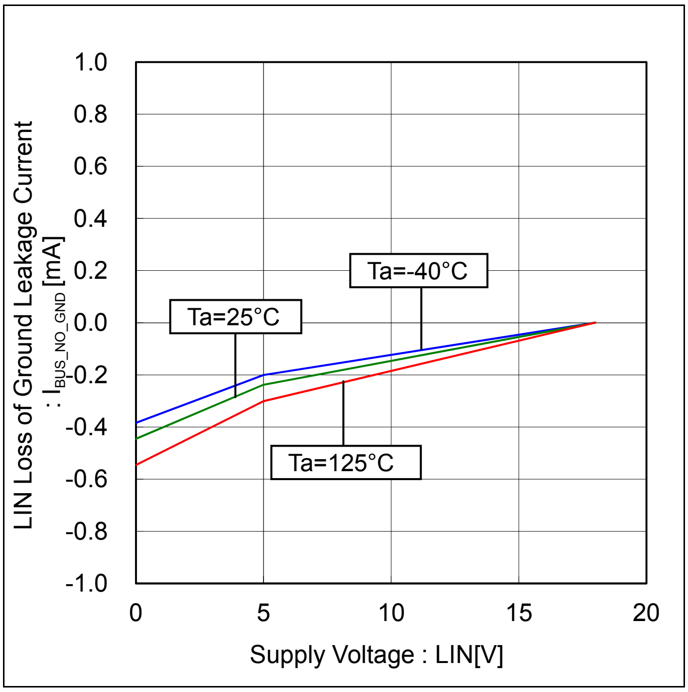


Figure 64. LIN Loss of Ground Leakage Current- voltage characteristic

Typical Performance Curves - continued

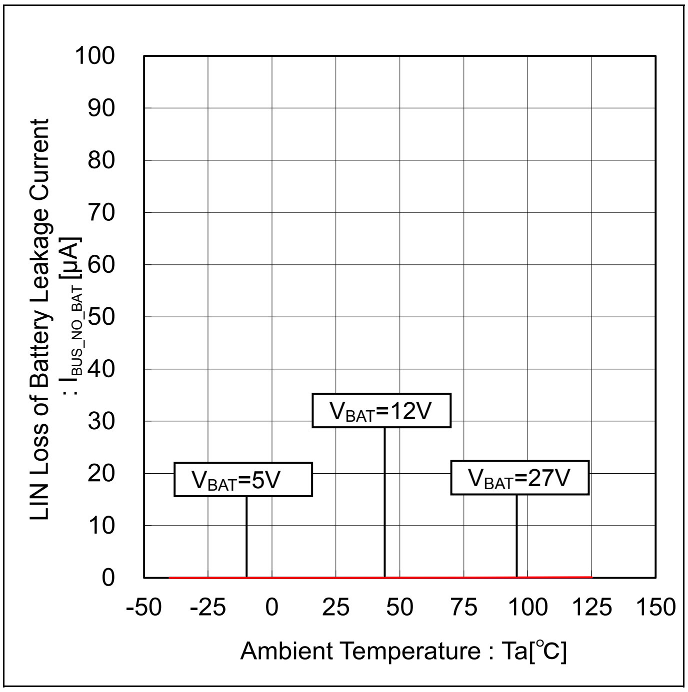


Figure 65. LIN Loss of Battery Leakage Current- temperature characteristic

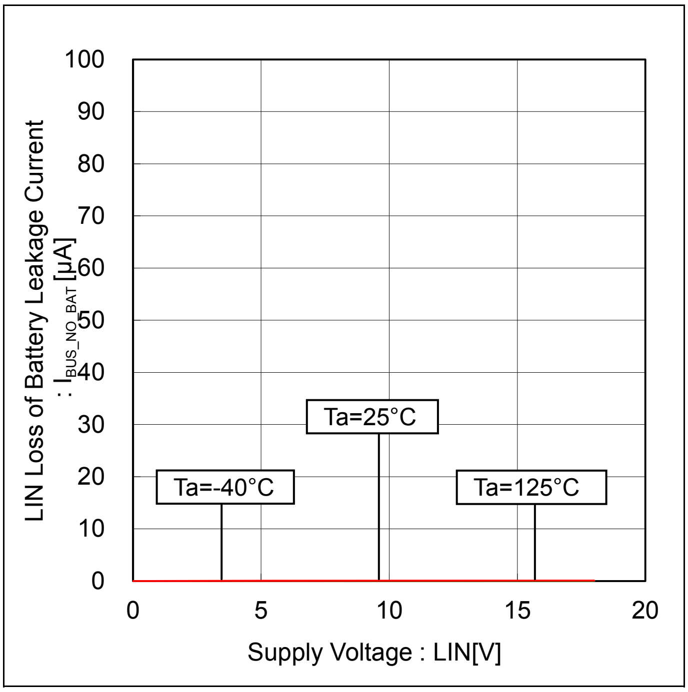


Figure 66. LIN Loss of Battery Leakage Current- voltage characteristic

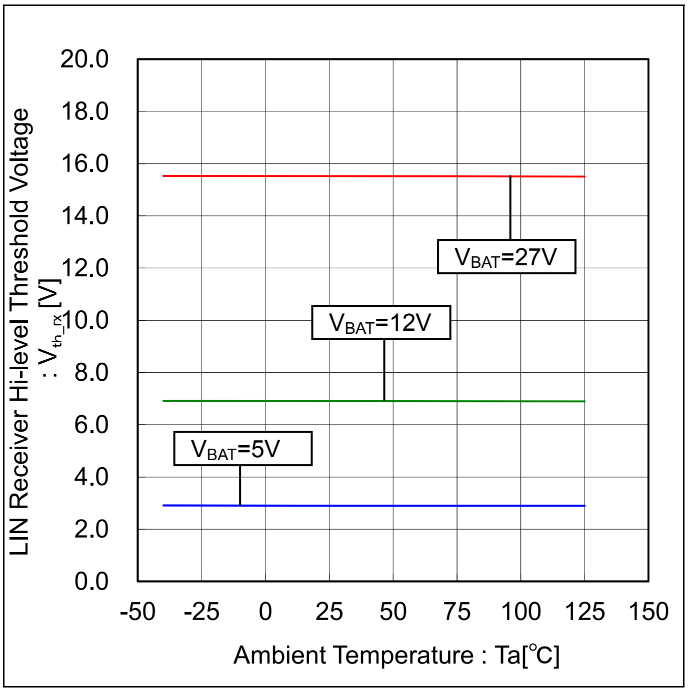


Figure 67. LIN Receiver Hi-level Threshold Voltage- temperature characteristic

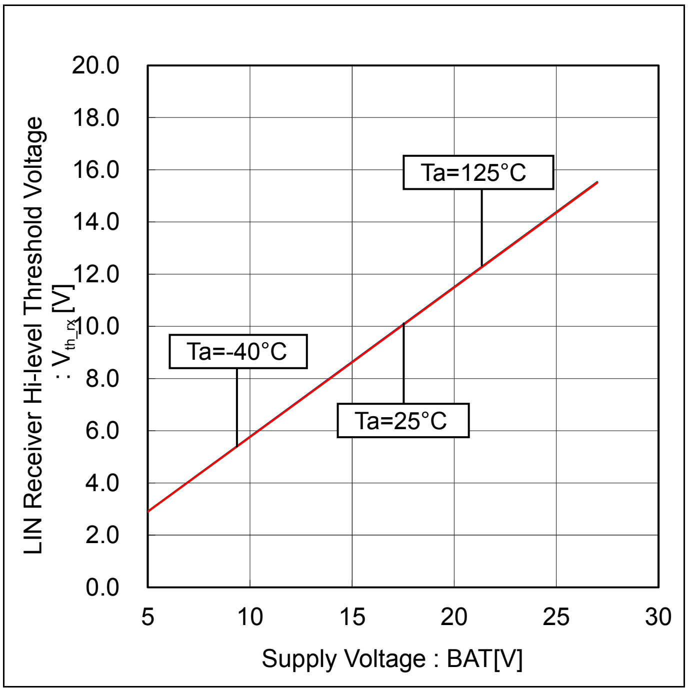


Figure 68. LIN Receiver Hi-level Threshold Voltage- voltage characteristic

Typical Performance Curves - continued

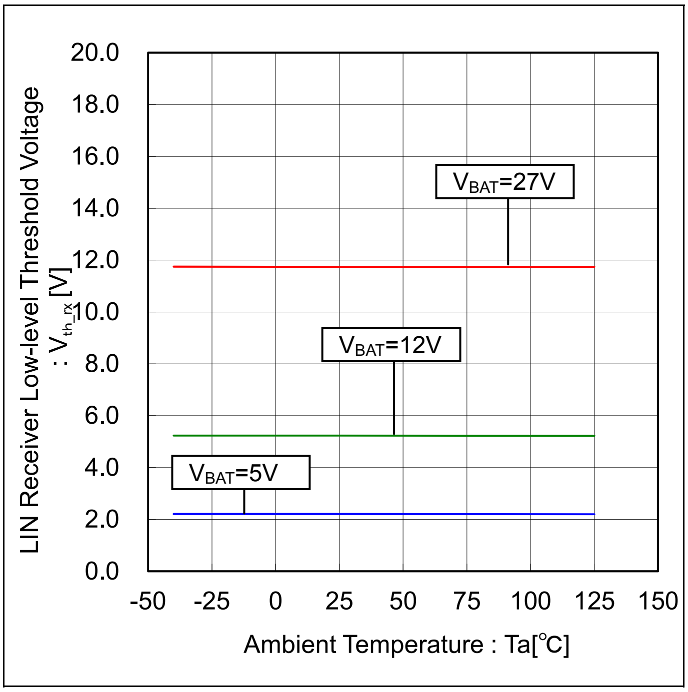


Figure 69. LIN Receiver Low-level Threshold Voltage-temperature characteristic

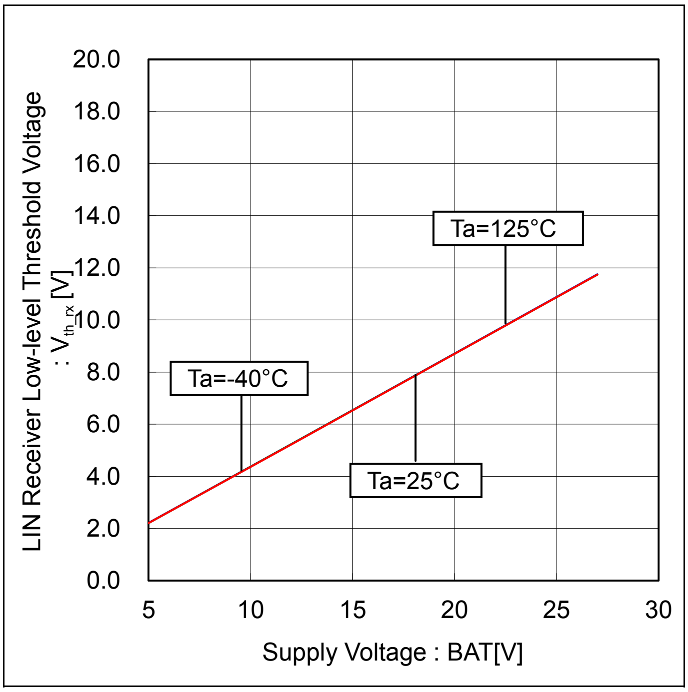


Figure 70. LIN Receiver Low-level Threshold Voltage-voltage characteristic

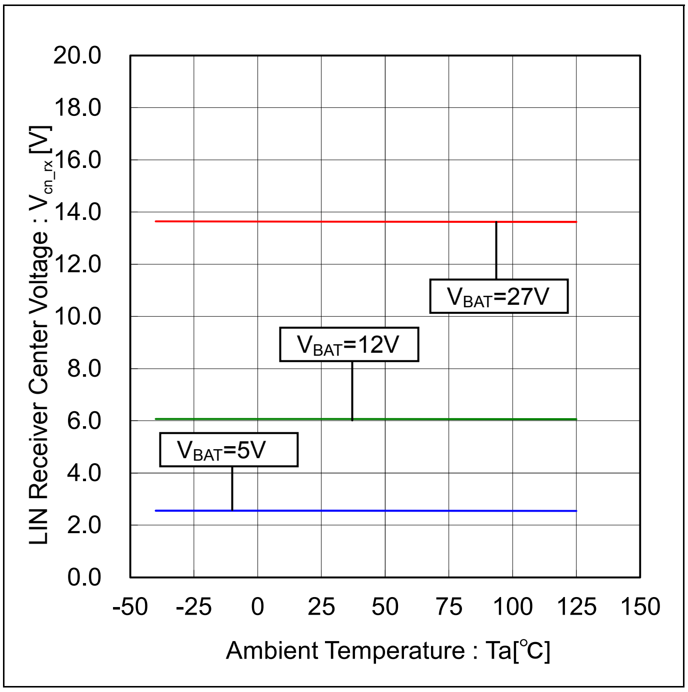


Figure 71. LIN Receiver Center Voltage- temperature characteristic

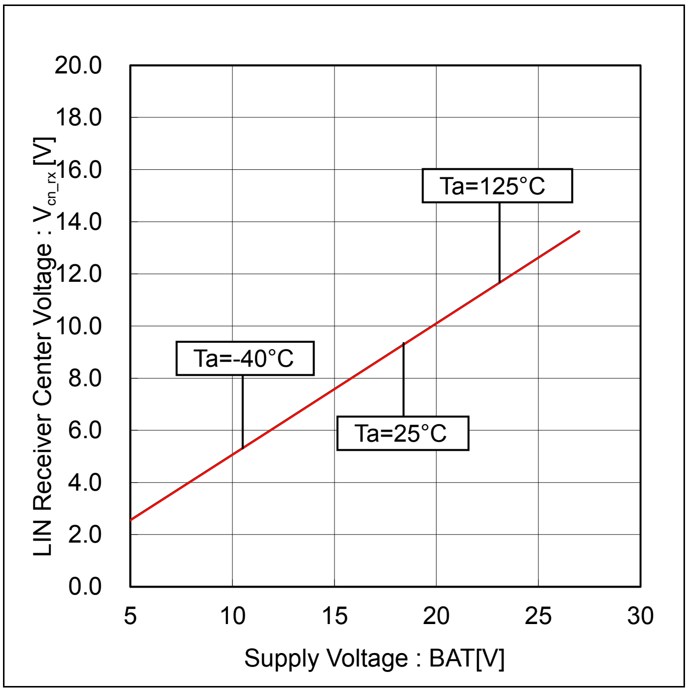


Figure 72. LIN Receiver Center Voltage- voltage characteristic

Typical Performance Curves - continued

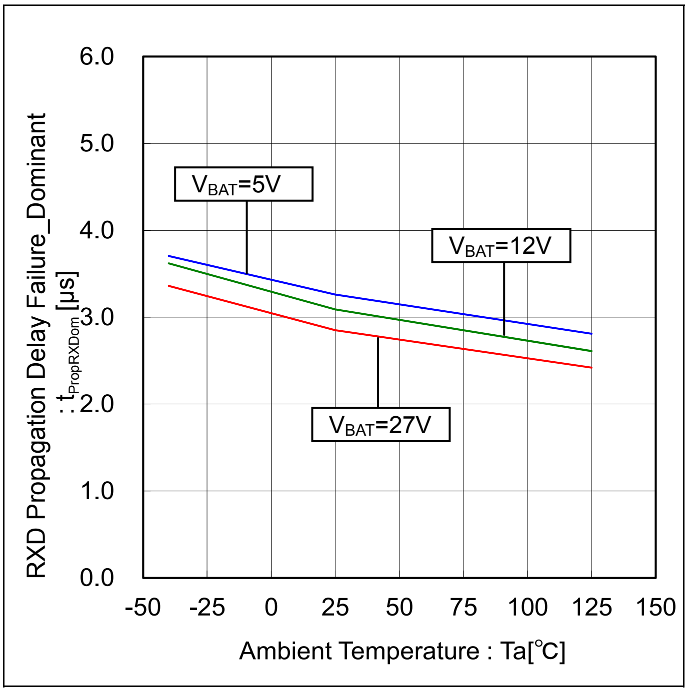


Figure 73. RXD Propagation Delay Failure_Dominant-temperature characteristic

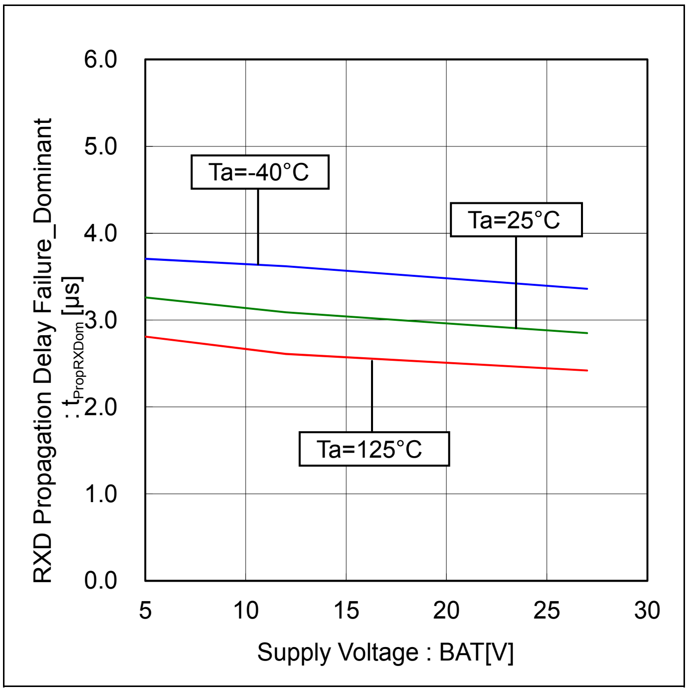


Figure 74. RXD Propagation Delay Failure_Dominant-voltage characteristic

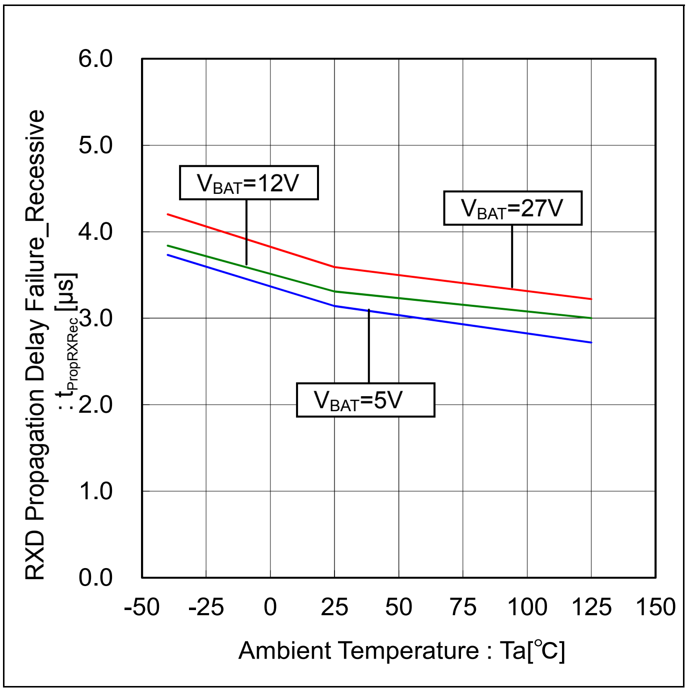


Figure 75. RXD Propagation Delay Failure_Recessive-temperature characteristic

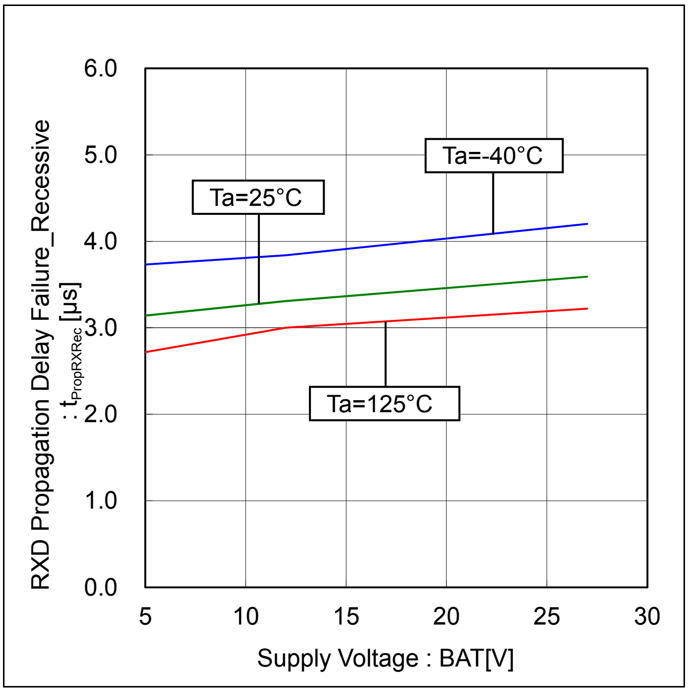


Figure 76. RXD Propagation Delay Failure_Recessive-voltage characteristic

Typical Performance Curves - continued

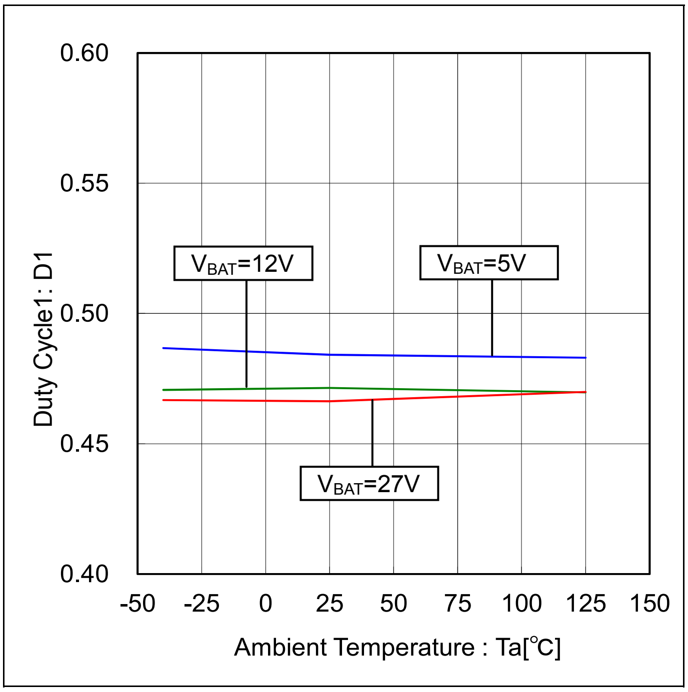


Figure 77. Duty Cycle1- temperature characteristic

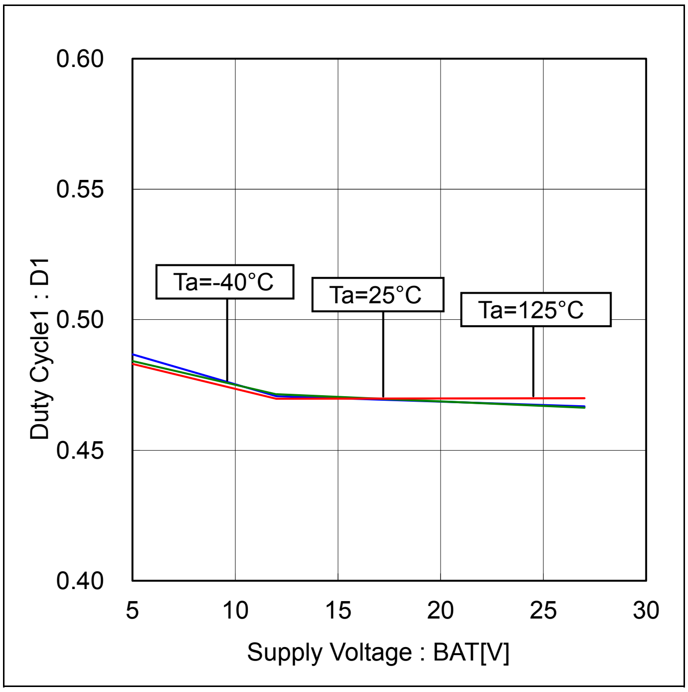


Figure 78. Duty Cycle1- voltage characteristic

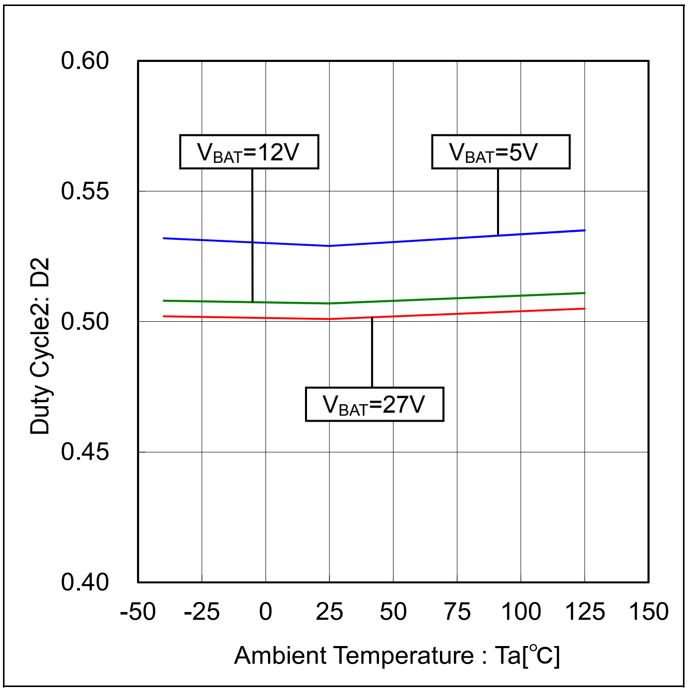


Figure 79. Duty Cycle2- temperature characteristic

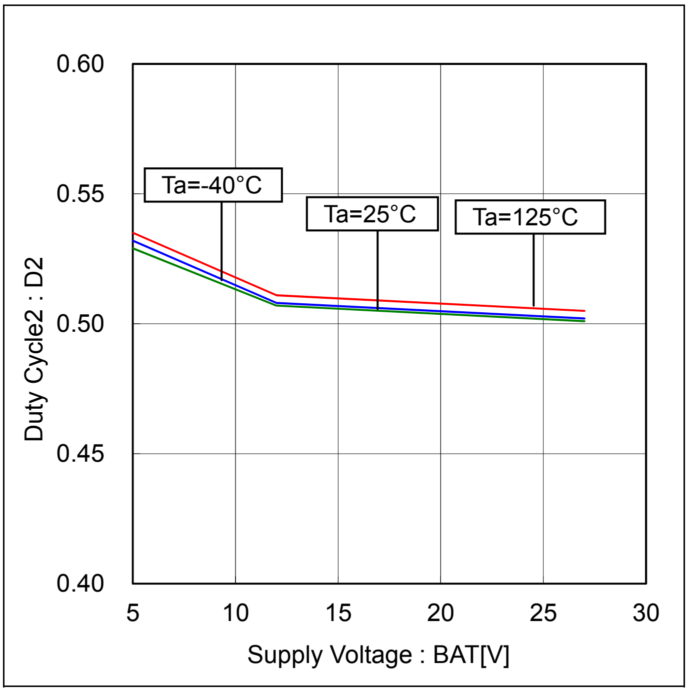


Figure 80. Duty Cycle2- voltage characteristic

Typical Performance Curves - continued

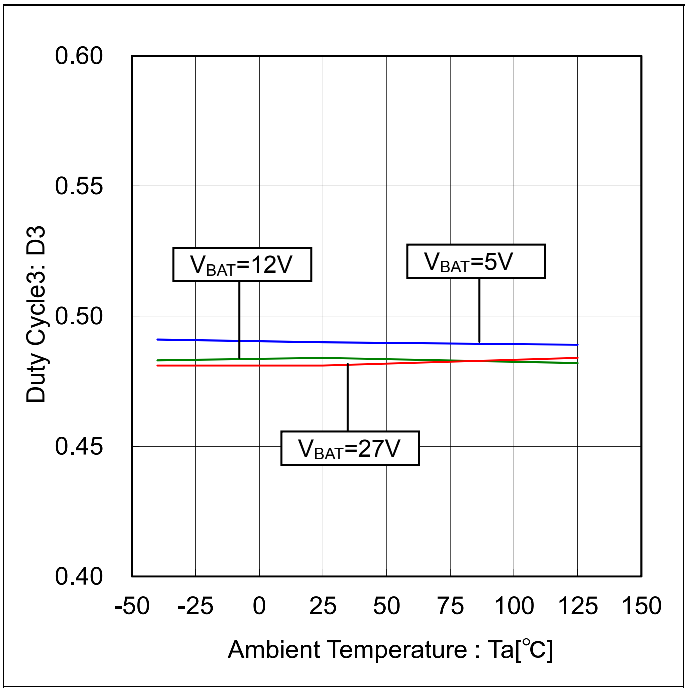


Figure 81. Duty Cycle3- temperature characteristic

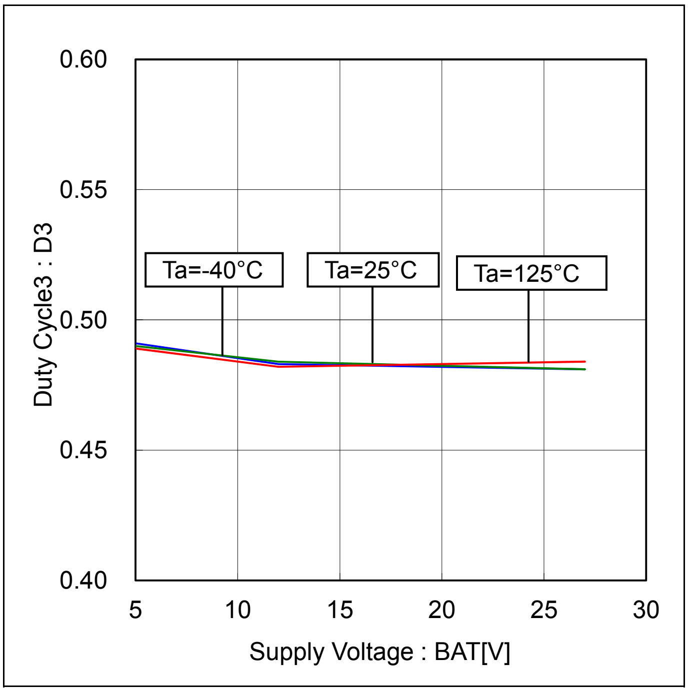


Figure 82. Duty Cycle3- voltage characteristic

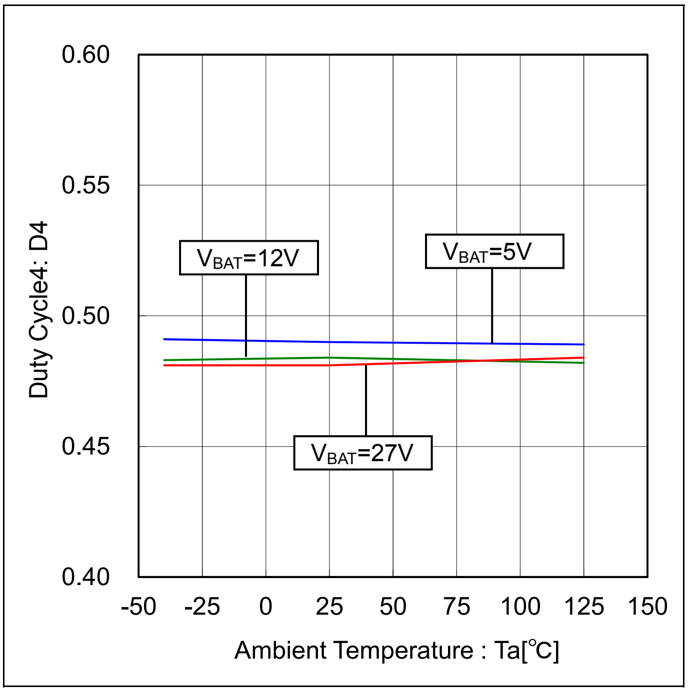


Figure 83. Duty Cycle4- temperature characteristic

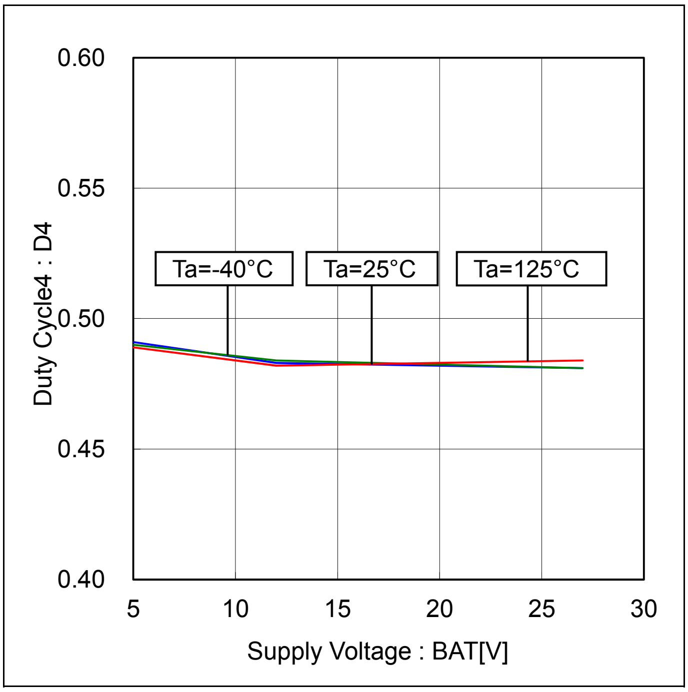


Figure 84. Duty Cycle4- voltage characteristic

Typical Performance Curves - continued

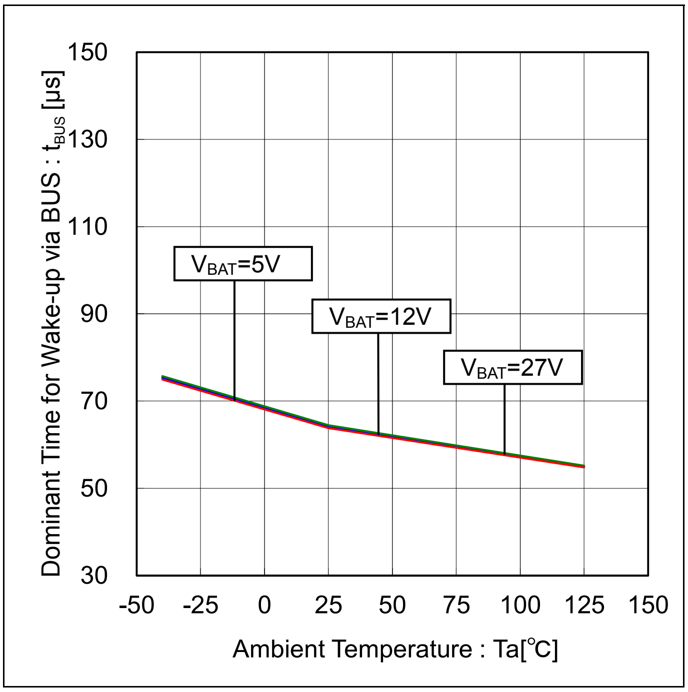


Figure 85. Dominant Time for Wake-up via BUS- temperature characteristic

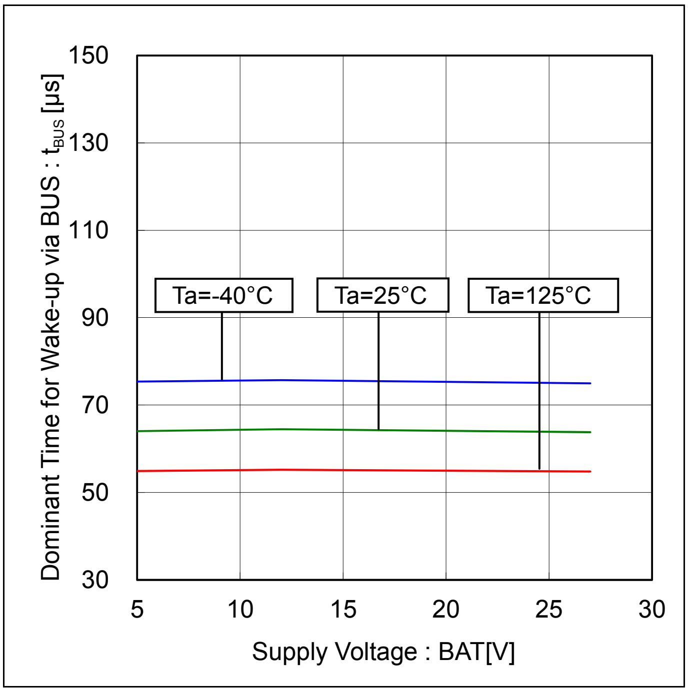


Figure 86. Dominant Time for Wake-up via BUS- voltage characteristic

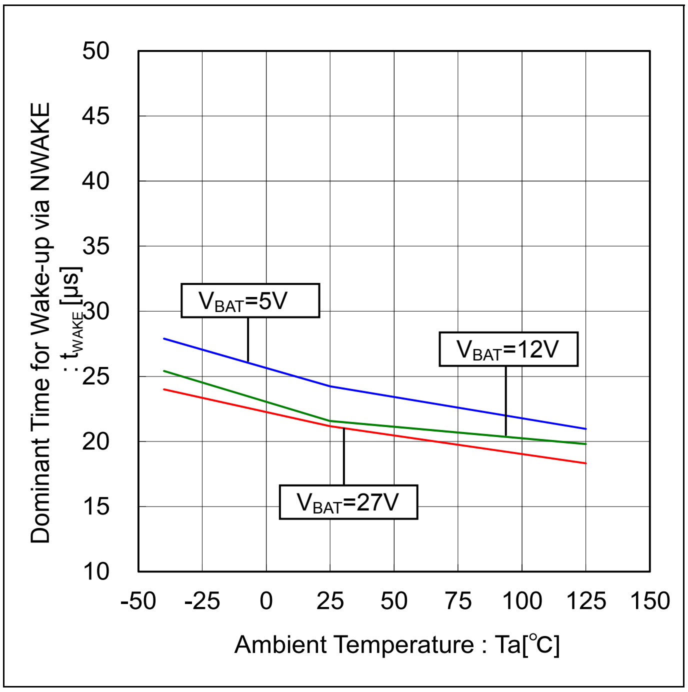


Figure 87. Dominant Time for Wake-up via NWAKE- temperature characteristic

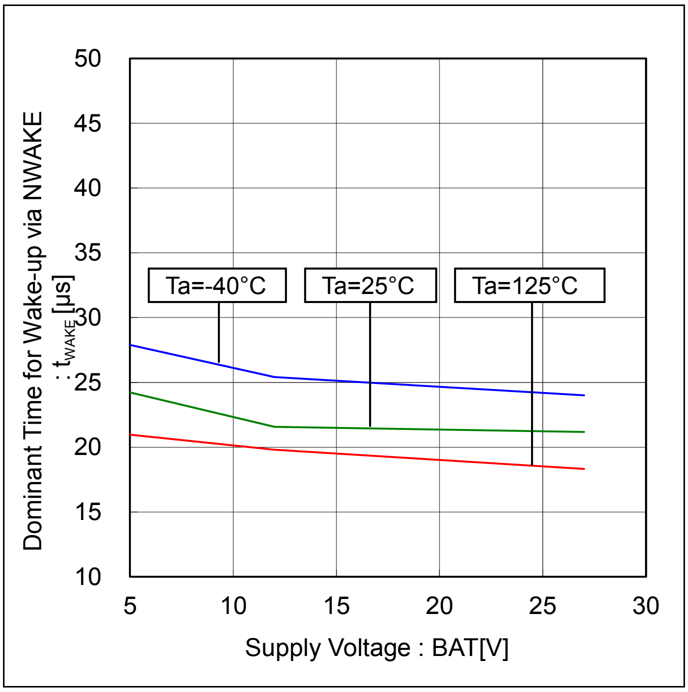


Figure 88. Dominant Time for Wake-up via NWAKE- voltage characteristic

Typical Performance Curves - continued

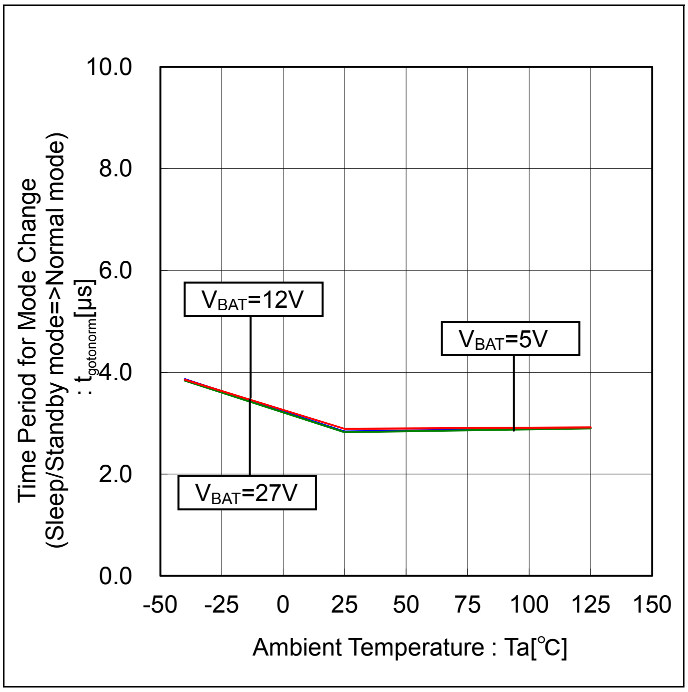


Figure 89. Time Period for Mode Change (Sleep/Standby mode=>Normal mode)- temperature characteristic

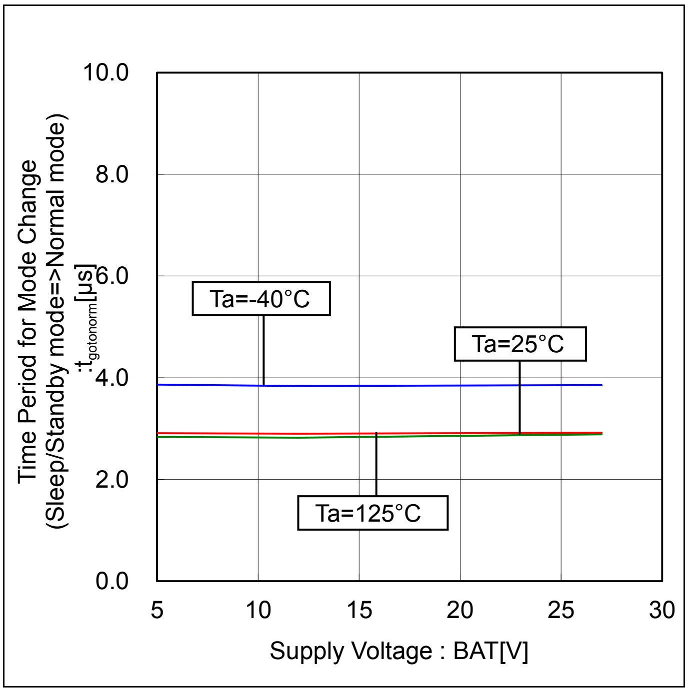


Figure 90. Time Period for Mode Change (Sleep/Standby mode=>Normal mode)- voltage characteristic

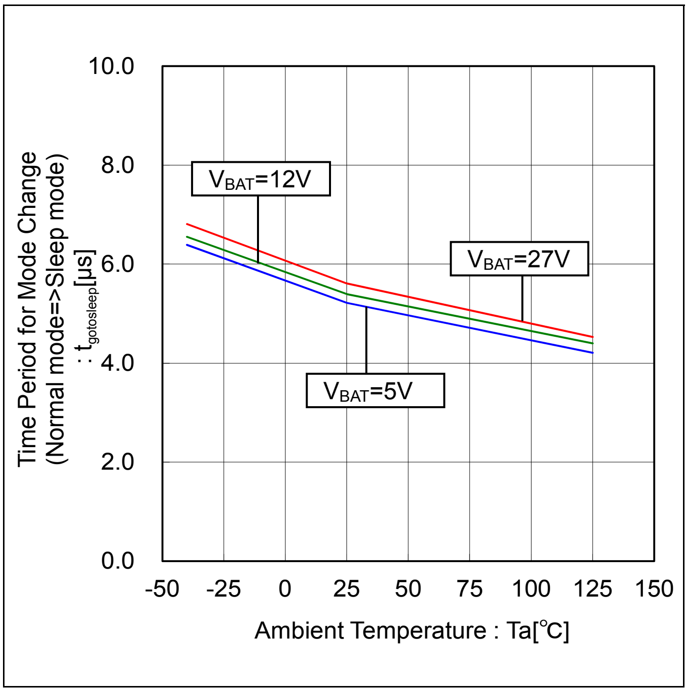


Figure 91. Time Period for Mode Change (Normal mode=>Sleep mode)- temperature characteristic

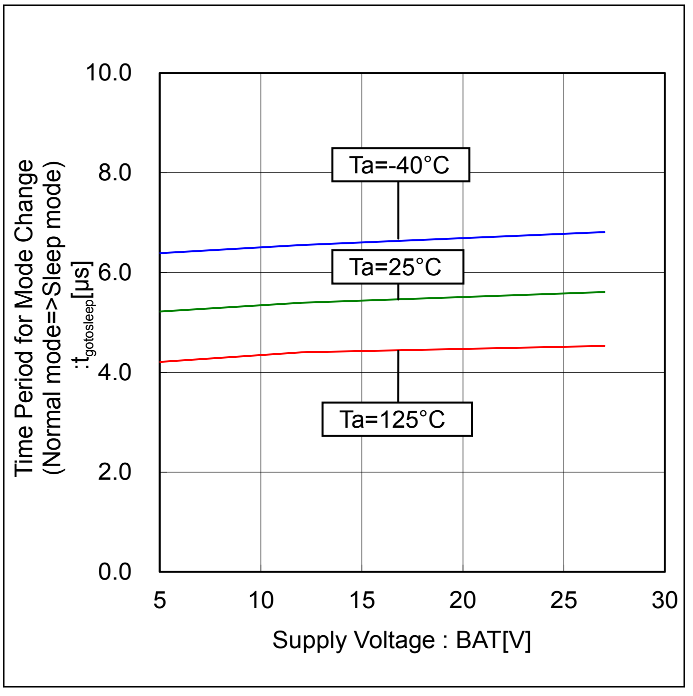


Figure 92. Time Period for Mode Change (Normal mode=>Sleep mode)- voltage characteristic

Typical Performance Curves - continued

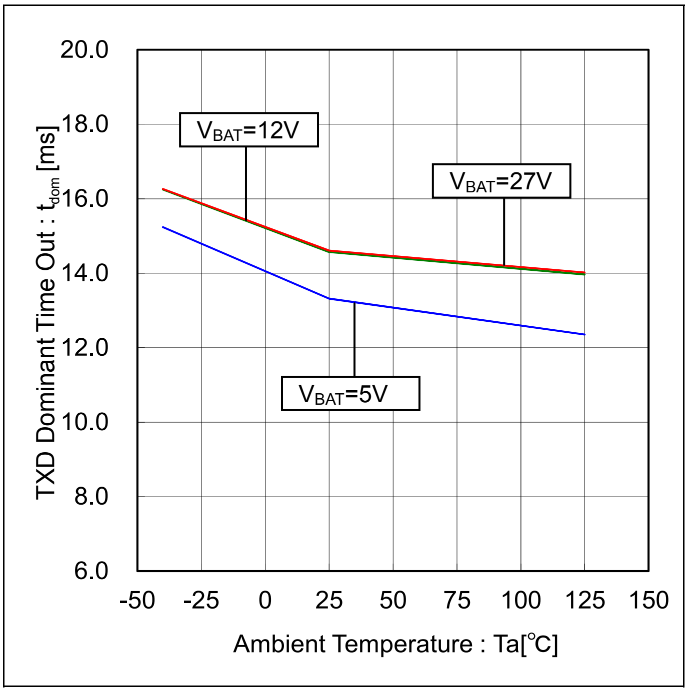


Figure 93. TXD Dominant Time Out- temperature characteristic

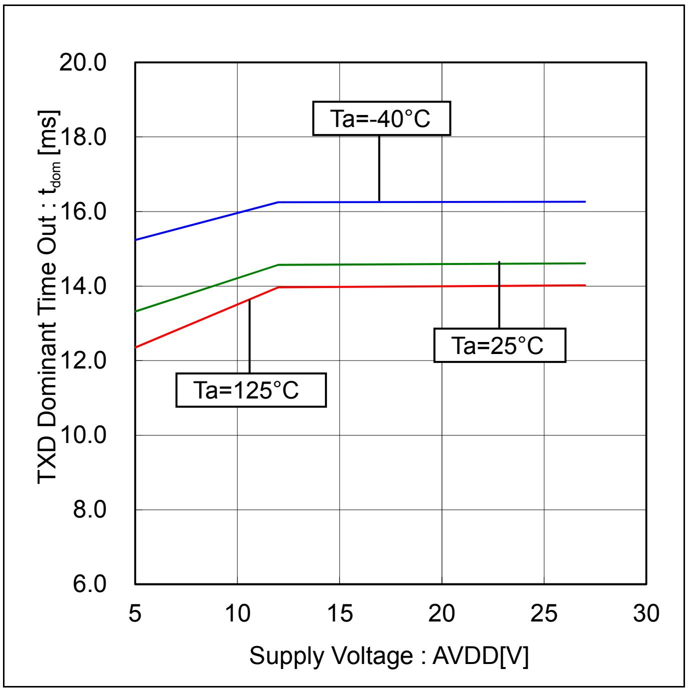


Figure 94. TXD Dominant Time Out- voltage characteristic

Timing Chart

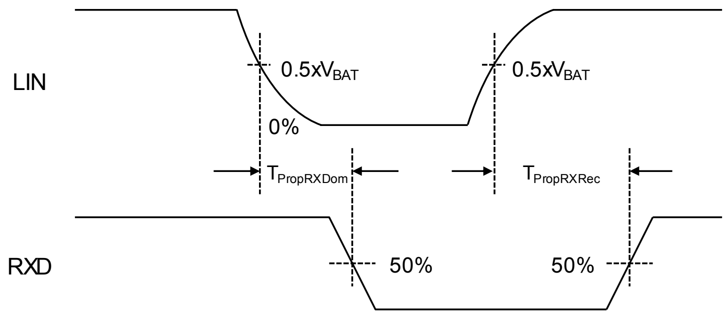


Figure 95. AC characteristic timing chart

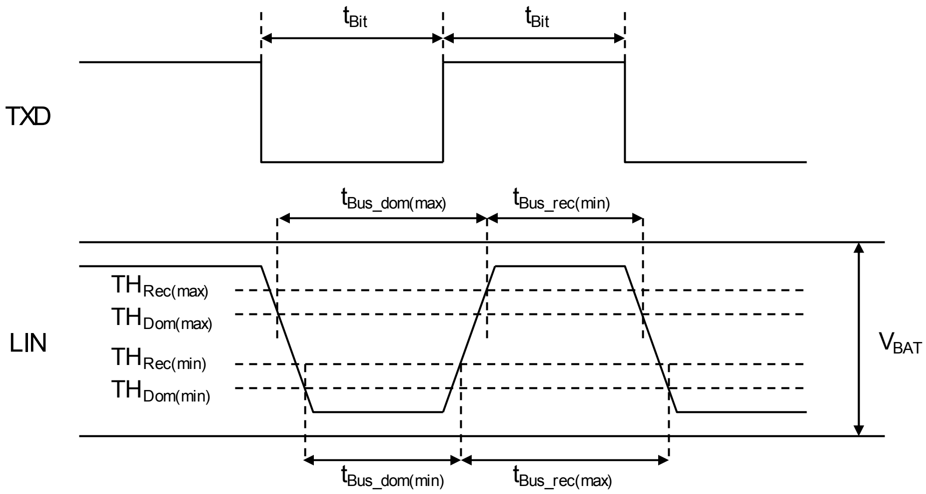


Figure 96. Bus timing chart

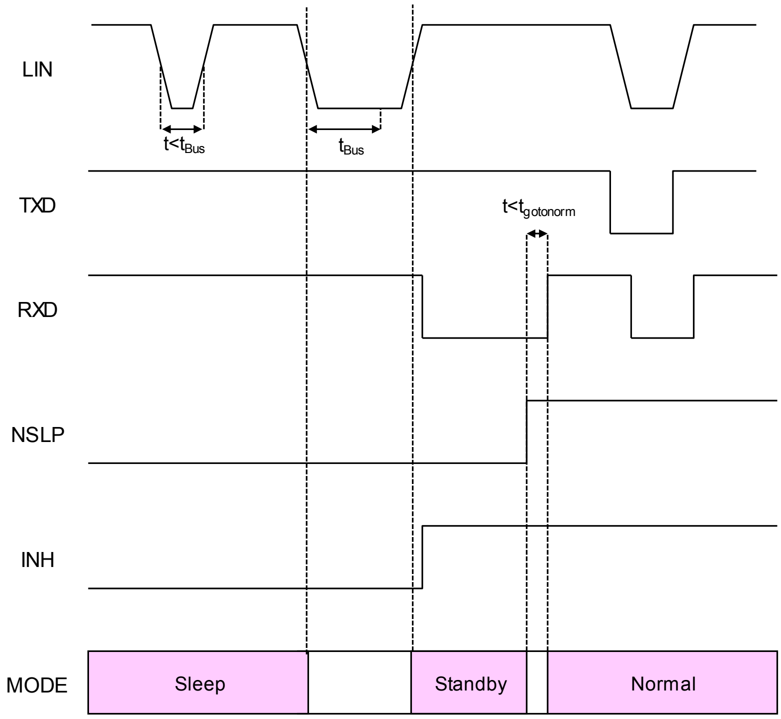


Figure 97. Remote wake-up (Sleep→Standby→Normal)

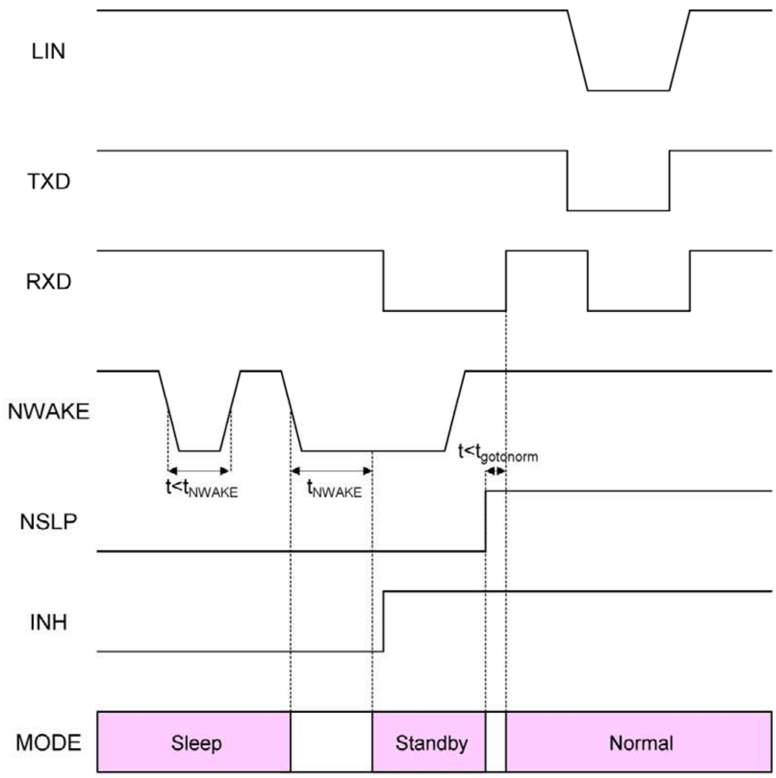


Figure 98. Local wake-up (Sleep→Standby→Normal)

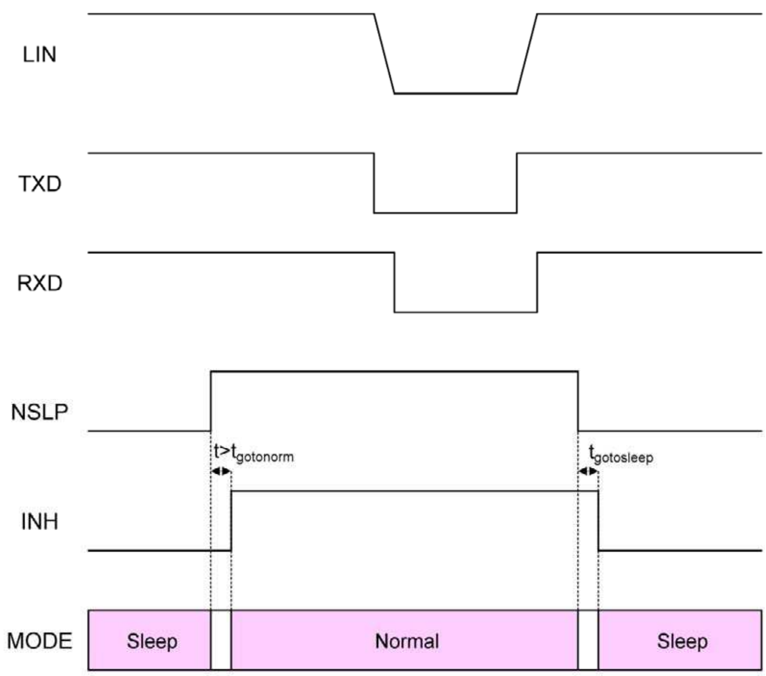


Figure 99. Wake-up/Sleep-in with NSLP (Sleep→Normal→Sleep)

Application Example(s)

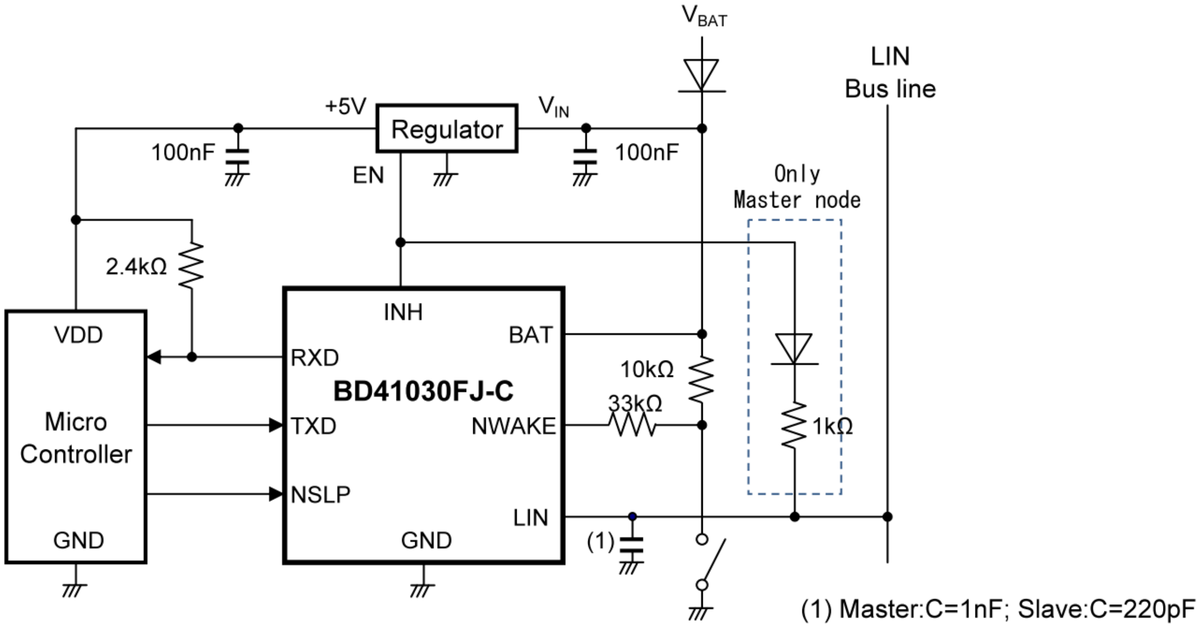
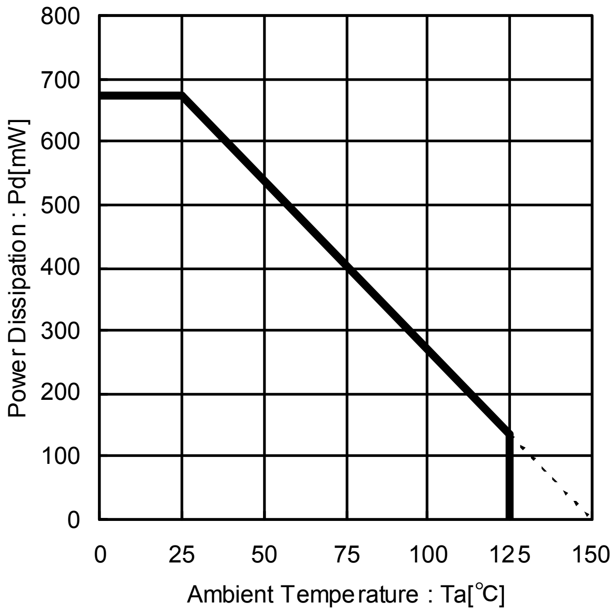


Figure 100. Application Example

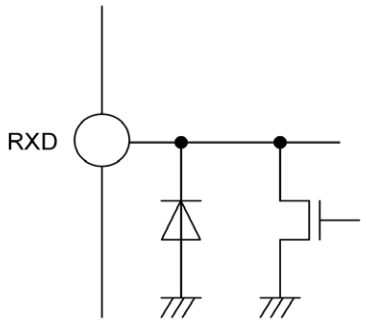
Power Dissipation

The value in the following graph is obtained at 25°C when ROHM standard substrate ($74.2 \times 74.2 \times 1.6mm^3$, surface layer copper foil : $34.09mm^2$, substrate material : FR4 and copper foil thickness : 18µm) is mounted.
The value shows a monotonous decrease above 25°C and becomes 0W at 150°C.

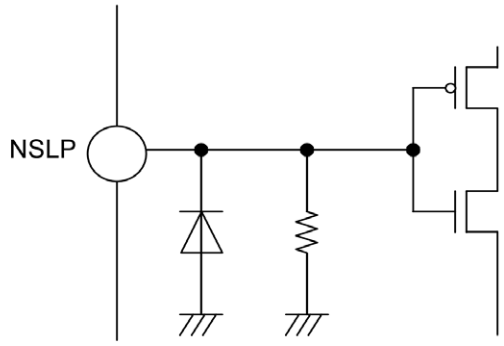


I/O equivalent circuit(s)

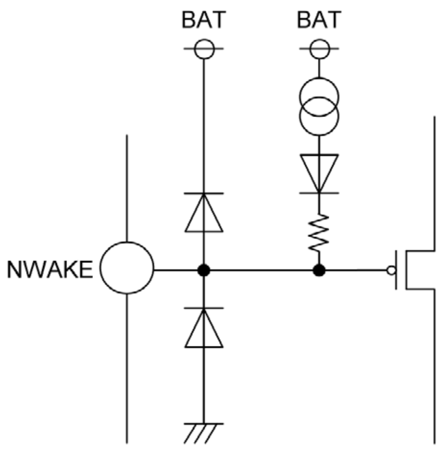
① RXD



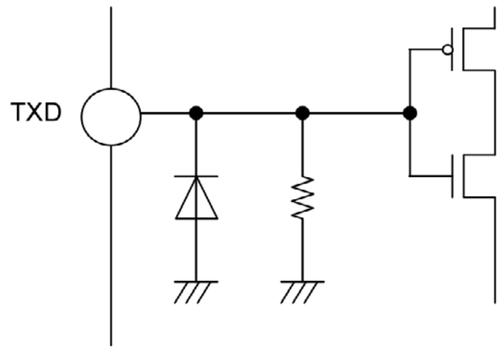
② NSLP



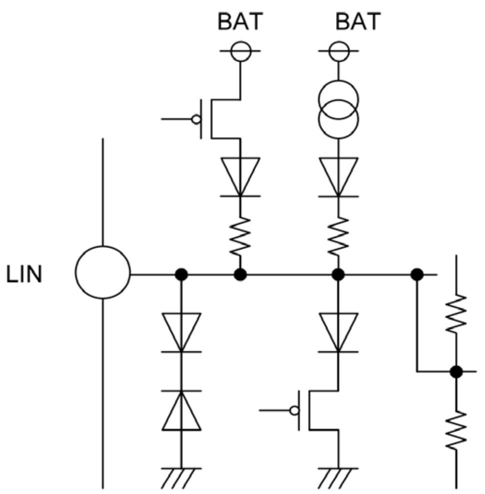
③ NWAKE



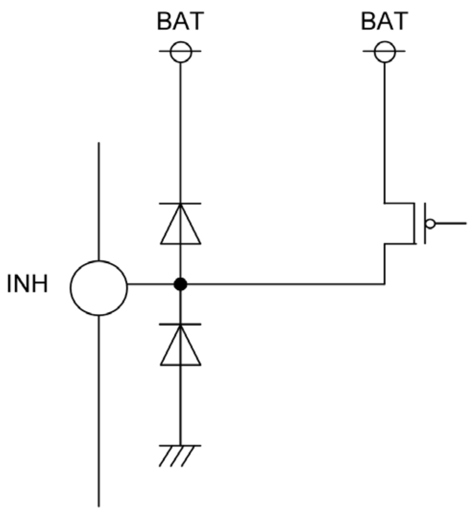
④ TXD



⑥ LIN



⑧ INH



Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

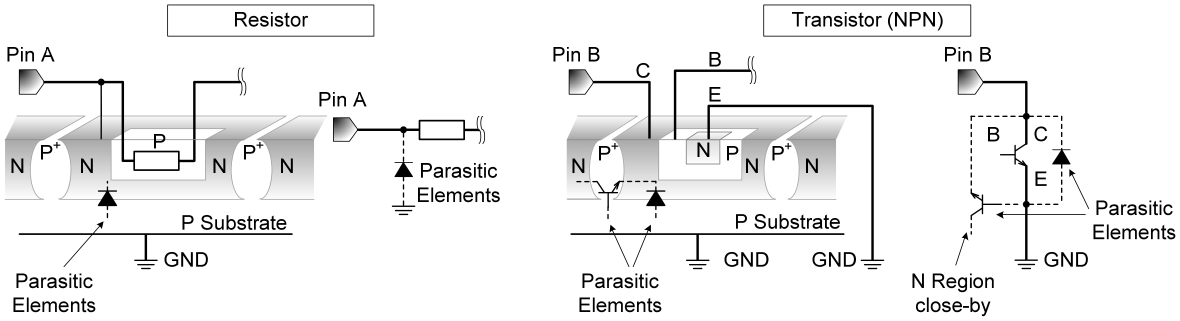


Figure 101. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

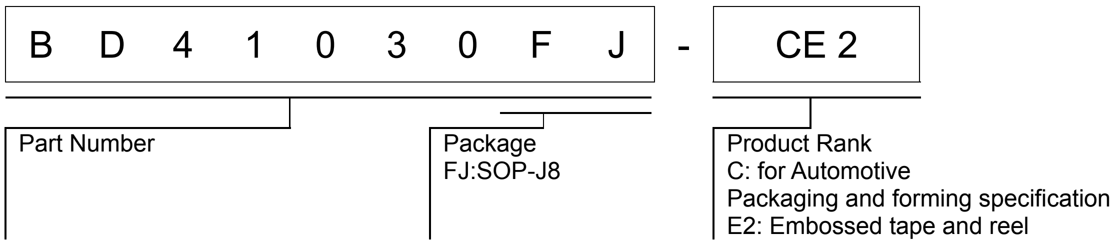
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

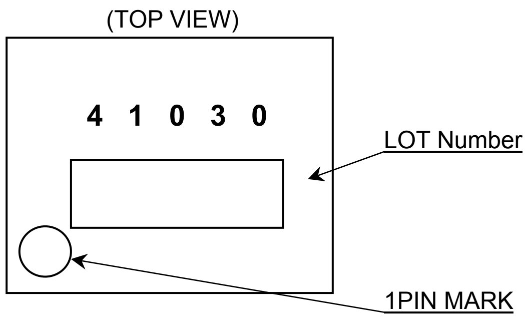
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

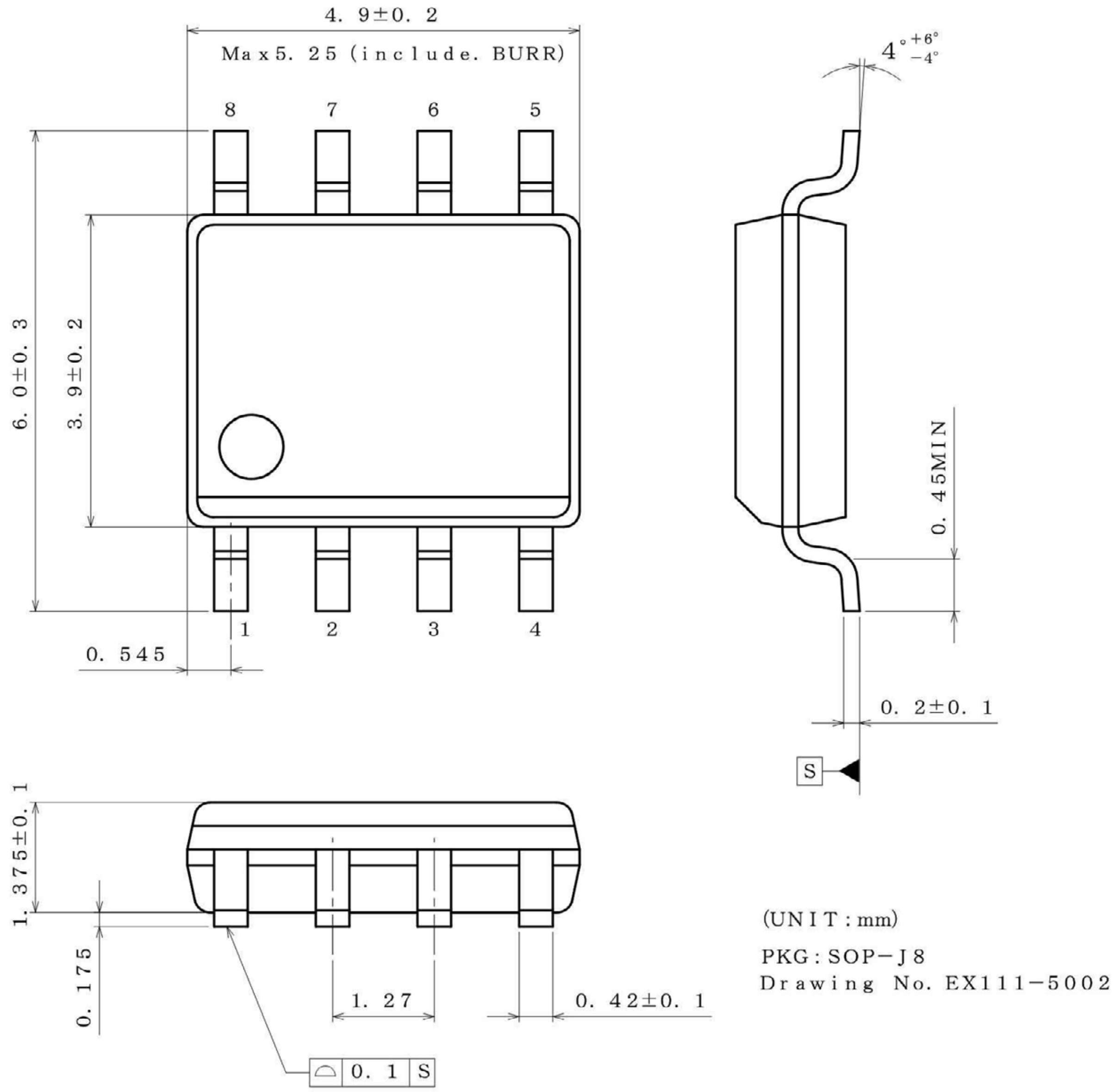


Marking Diagrams



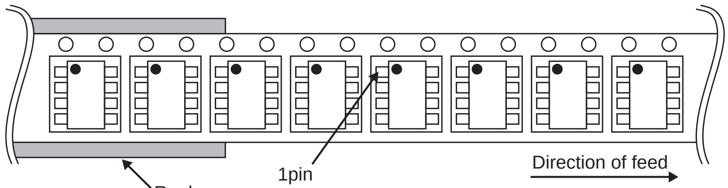
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
12.Jun.2015	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

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