19-3143; Rev 2; 9/05

EVALUATION KIT AVAILABLE

Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

MAX1126

General Description

The MAX1126 quad, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction. This ADC is optimized for low-power, high-dynamic performance for medical imaging, communications, and instrumentation applications. The MAX1126 operates from a 1.7V to 1.9V single supply and consumes only 563mW while delivering a 69.9dB signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1126 features an 813µA power-down mode for idle periods.

An internal 1.24V precision bandgap reference sets the ADC's full-scale range. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range.

A single-ended clock controls the conversion process. An internal duty-cycle equalizer allows for wide variations in input-clock duty cycle. An on-chip phase-locked loop (PLL) generates the high-speed serial low-voltage differential signaling (LVDS) clock.

The MAX1126 provides serial LVDS outputs for data, clock, and frame alignment signals. The output data is presented in two's complement or binary format.

Refer to the MAX1127 data sheet for a pin-compatible 65Msps version of the MAX1126.

The MAX1126 is available in a small, 10mm x 10mm x 0.9mm, 68-pin QFN package with exposed paddle and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

Ultrasound and Medical Imaging

Positron Emission Tomography (PET) Imaging

Multichannel Communication Systems

Instrumentation

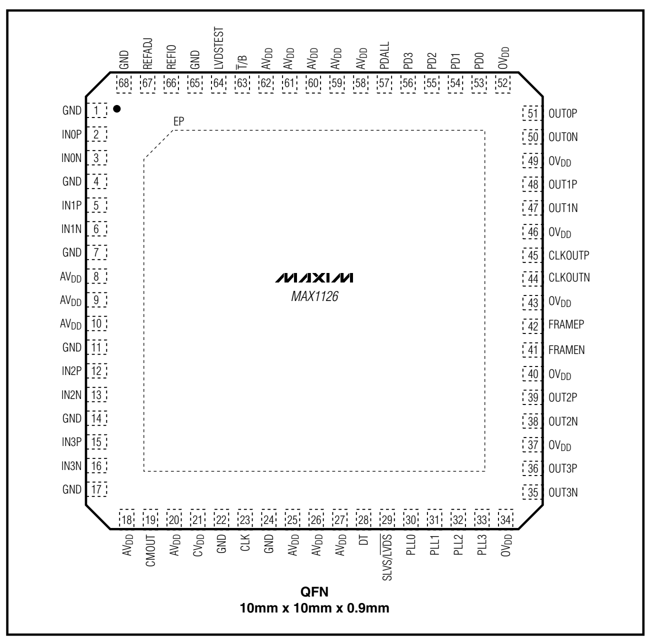
Features

- **Four ADC Channels with Serial LVDS/SLVS Outputs**
- **Excellent Dynamic Performance**
  - **69.9dB SNR at f_{IN} = 5.3MHz**
  - **93.7dBc SFDR at f_{IN} = 5.3MHz**
  - **-90dB Channel Isolation**
- **Ultra-Low Power**
  - **135mW per Channel (Normal Operation)**
  - **1.5mW Total (Shutdown Mode)**
- **Accepts 20% to 80% Clock Duty Cycle**
- **Self-Aligning Data-Clock to Data-Output Interface**
- **Fully Differential Analog Inputs**
- **Wide ±1.4V_{P-P} Differential Input Voltage Range**
- **Internal/External Reference Option**
- **Test Mode for Digital Signal Integrity**
- **LVDS Outputs Support Up to 30in FR-4 Backplane Connections**
- **Small, 68-Pin QFN with Exposed Paddle**
- **Evaluation Kit Available (MAX1127EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1126EGK	-40°C to +85°C	68 QFN 10mm x x 10mm x 0.9mm

Pin Configuration



Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND...-0.3V to +2.0V
CV_{DD} to GND ....-0.3V to +3.6V
OV_{DD} to GND ....-0.3V to +2.0V
IN_P, IN_N to GND...................................-0.3V to (AV_{DD} + 0.3V)
CLK to GND...-0.3V to (CV_{DD} + 0.3V)
OUT_P, OUT_N, FRAME_,
CLKOUT_ to GND................................-0.3V to (OV_{DD} + 0.3V)
DT, SLVS/$\overline{\text{LVDS}}$ to GND...........................-0.3V to (AV_{DD} + 0.3V)
PLL0, PLL1, PLL2, PLL3 to GND ....-0.3V to (AV_{DD} + 0.3V)
PD0, PD1, PD2, PD3, PDALL to GND......-0.3V to (AV_{DD} + 0.3V)
$\overline{\text{T}}$/B, LVDSTEST to GND ....-0.3V to (AV_{DD} + 0.3V)
REFIO, REFADJ, CMOUT, to GND ....-0.3V to (AV_{DD} + 0.3V)
I.C. to GND..-0.3V to (AV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
68-Pin QFN 10mm x 10mm x 0.9mm
(derated 41.7mW/°C above +70°C)........................3333.3mW
Operating Temperature Range ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature Range (soldering, 10s)......................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, C_{REFIO} to GND = 0.1µF, f_{CLK} = 40MHz (50% duty cycle), DT = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 2)		±0.4		LSB
Differential Nonlinearity	DNL	(Note 2)		±0.25		LSB
Offset Error		Fixed external reference (Note 2)			±1	% FS
Gain Error		Fixed external reference (Note 2)	-1.5	+0.9	+2.5	% FS
ANALOG INPUTS (IN_P, IN_N)						
Input Differential Range	V_{ID}	Differential input		1.4		V_{P-P}
Common-Mode Voltage Range	V_{CMO}	(Note 3)		0.76		V
Differential Input Impedance	R_{IN}	Switched capacitor load		2		kΩ
Differential Input Capacitance	C_{IN}			12.5		pF
CONVERSION RATE						
Maximum Conversion Rate	f_{SMAX}		40			MHz
Minimum Conversion Rate	f_{SMIN}			4		MHz
Data Latency				6.5		Cycles
DYNAMIC CHARACTERISTICS (differential inputs, 4096-point FFT)						
Signal-to-Noise Ratio (Note 2)	SNR	f_{IN} = 5.3MHz at -0.5dBFS		69.9		dB
		f_{IN} = 19.3MHz at -0.5dBFS, T_A ≥ +25°C	66.7	69.2		
Signal-to-Noise and Distortion (First Four Harmonics) (Note 2)	SINAD	f_{IN} = 5.3MHz at -0.5dBFS		69.8		dB
		f_{IN} = 19.3MHz at -0.5dBFS, T_A ≥ +25°C	66.7	69.1		
Effective Number of Bits (Note 2)	ENOB	f_{IN} = 5.3MHz at -0.5dBFS		11.4		Bits
		f_{IN} = 19.3MHz at -0.5dBFS		11.3		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, C_{REFIO} to GND = 0.1µF, f_{CLK} = 40MHz (50% duty cycle), DT = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range (Note 2)	SFDR	f_{IN} = 5.3MHz at -0.5dBFS		93.7		dBc
		f_{IN} = 19.3MHz at -0.5dBFS, $T_A \geq$ +25°C	77.3	89		
Total Harmonic Distortion (Note 2)	THD	f_{IN} = 5.3MHz at -0.5dBFS		-91.5		dBc
		f_{IN} = 19.3MHz at -0.5dBFS, $T_A \geq$ +25°C		-88.7	-76.3	
Intermodulation Distortion	IMD	f_1 = 12.40125MHz at -6.5dBFS, f_2 = 13.60125MHz at -6.5dBFS (Note 2)		87.0		dBc
Third-Order Intermodulation	IM3	f_1 = 12.40125MHz at -6.5dBFS, f_2 = 13.60125MHz at -6.5dBFS (Note 2)		89.3		dBc
Aperture Jitter	t_{AJ}	(Note 2)		< 0.4		ps_{RMS}
Aperture Delay	t_{AD}	(Note 2)		1		ns
Small-Signal Bandwidth	SSBW	Input at -20dBFS (Notes 2 and 4)		100		MHz
Full-Power Bandwidth	LSBW	Input at -0.5dBFS (Notes 2 and 4)		100		MHz
Output Noise		IN_P = IN_N		0.45		LSB_{RMS}
Overdrive Recovery Time	t_{OR}	R_S = 25Ω, C_S = 50pF		1		Clock cycles
COMMON-MODE OUTPUT (CMOUT)						
CMOUT Output Voltage	V_{CMOUT}			0.76		V
INTERNAL REFERENCE (REFADJ = GND, bypass REFIO to GND with 0.1µF)						
REFADJ Internal Reference Mode Enable Voltage		(Note 5)			0.1	V
REFADJ Low-Leakage Current				1.6		mA
REFIO Output Voltage	V_{REFIO}		1.18	1.24	1.30	V
Reference Temperature Coefficient	TC_{REFIO}			100		ppm/°C
EXTERNAL REFERENCE (REFADJ = AV_{DD})						
REFADJ External Reference Mode Enable Voltage		(Note 5)	AV_{DD} - 0.1V			V
REFADJ High-Leakage Current				125		µA
REFIO Input Voltage Range				1.24		V
REFIO Input Voltage Tolerance				±5		%
REFIO Input Current	I_{REFIO}			< 1		µA
CLOCK INPUT (CLK)						
Input High Voltage	V_{CLKH}		0.8 x AV_{DD}			V
Input Low Voltage	V_{CLKL}				0.2 x AV_{DD}	V
Clock Duty Cycle				50		%
Clock Duty-Cycle Tolerance				±30		%

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, C_{REFIO} to GND = 0.1µF, f_{CLK} = 40MHz (50% duty cycle), DT = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	DI_{IN}	Input at GND			5	µA
		Input at AV_{DD}			80	
Input Capacitance	DC_{IN}			5		pF
DIGITAL INPUTS (PLL_, LVDSTEST, DT, SLVS/$\overline{LVDS}$, PD_, PDALL, $\overline{T}$/B)						
Input High Threshold	V_{IH}		0.8 x AV_{DD}			V
Input Low Threshold	V_{IL}				0.2 x AV_{DD}	V
Input Leakage	DI_{IN}	Input at GND			5	µA
		Input at AV_{DD}			80	
Input Capacitance	DC_{IN}			5		pF
LVDS OUTPUTS (OUT_P, OUT_N, SLVS/$\overline{LVDS}$ = 0						
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω	250		450	mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω	1.125		1.375	V
Rise Time (20% to 80%)	t_R	R_{TERM} = 100Ω, C_{LOAD} = 5pF		150		ps
Fall Time (80% to 20%)	t_F	R_{TERM} = 100Ω, C_{LOAD} = 5pF		150		ps
SLVS OUTPUTS (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, FRAMEN), SLVS/$\overline{LVDS}$ = 1, DT = 1						
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω		205		mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω		220		mV
Rise Time (20% to 80%)	t_R	R_{TERM} = 100Ω, C_{LOAD} = 5pF		120		ps
Fall Time (80% to 20%)	t_F	R_{TERM} = 100Ω, C_{LOAD} = 5pF		120		ps
POWER-DOWN						
PD Fall to Output Enable	t_{ENABLE}			132		µs
PD Rise to Output Disable	$t_{DISABLE}$			10		ns
POWER REQUIREMENTS						
AV_{DD} Supply Voltage	AV_{DD}		1.7	1.8	1.9	V
OV_{DD} Supply Voltage	OV_{DD}		1.7	1.8	1.9	V
CV_{DD} Supply Voltage	CV_{DD}		1.7	1.8	3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, C_{REFIO} to GND = 0.1µF, f_{CLK} = 40MHz (50% duty cycle), DT = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AV_{DD} Supply Current	I_{AVDD}	f_{IN} = 19.3MHz at -0.5dBFS	PDALL = 0, all channels active		246	285	mA
			PDALL = 0, all channels active, DT = 1		246		mA
			PDALL = 0, 1 channel active		76		mA
			PDALL = 0, PD[3:0] = 1111		20		mA
			PDALL = 1, global power down, PD[3:0] =1111, no clock input		438		µA
OV_{DD} Supply Current	I_{OVDD}	f_{IN} = 19.3MHz at -0.5dBFS	PDALL = 0, all channels active		51	57	mA
			PDALL = 0, all channels active, DT = 1		63		mA
			PDALL = 0, 1 channel active		35		mA
			PDALL = 0, PD[3:0] = 1111		30		mA
			PDALL = 1, global power-down, PD[3:0] =1111, no clock input		375		µA
CV_{DD} Supply Current	I_{CVDD}	CV_{DD} is used only to bias ESD-protection diodes on CLK input, Figure 2			0		mA
Power Dissipation	P_{DISS}	f_{IN} = 19.3MHz at -0.5dBFS			535	616	mW
TIMING CHARACTERISTICS (Note 6)							
Data Valid to CLKOUT Rise/Fall	t_{OD}	f_{CLK} = 40MHz, Figure 5 (Notes 6 and 7)		(t_{SAMPLE}/ 24) - 0.15	t_{SAMPLE}/ 24	(t_{SAMPLE}/ 24) + 0.15	ns
CLKOUT Output Width High	t_{CH}	Figure 5			t_{SAMPLE}/ 12		ns
CLKOUT Output Width Low	t_{CL}	Figure 5			t_{SAMPLE}/ 12		ns
FRAME Rise to CLKOUT Rise	t_{CF}	Figure 4 (Note 7)		(t_{SAMPLE}/ 24) - 0.15	t_{SAMPLE}/ 24	(t_{SAMPLE}/ 24) + 0.15	ns
Sample CLK Rise to Frame Rise	t_{SF}	Figure 4 (Notes 7 and 8)		(t_{SAMPLE}/ 2) +0.9	(t_{SAMPLE}/ 2) +1.3	(t_{SAMPLE}/ 2) +1.7	ns

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, C_{REFIO} to GND = 0.1µF, f_{CLK} = 40MHz (50% duty cycle), DT = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHANNEL-TO-CHANNEL MATCHING						
Crosstalk		(Note 2)		-90		dB
Gain Matching		f_{IN} = 19.3MHz (Note 2)		±0.1		dB
Phase Matching		f_{IN} = 19.3.MHz (Note 2)		±1		Degrees

Note 1: Specifications at $T_A \geq$ +25°C are guaranteed by production testing. Specifications at $T_A <$ +25°C are guaranteed by design and characterization and not subject to production testing.

Note 2: See definition in the *Parameter Definitions* section.

Note 3: The MAX1126 internally sets the common-mode voltage to 0.76V (typ) (see Figure 1). The common-mode voltage can be overdriven to between 0.55V and 0.85V.

Note 4: Limited by MAX1127EVKIT input circuitry.

Note 5: Connect REFADJ to GND directly to enable internal reference mode. Connect REFADJ to AV_{DD} directly to disable the internal bandgap reference and enable external reference mode.

Note 6: Data valid to CLKOUT rise/fall timing is measured from 50% of data output level to 50% of clock output level.

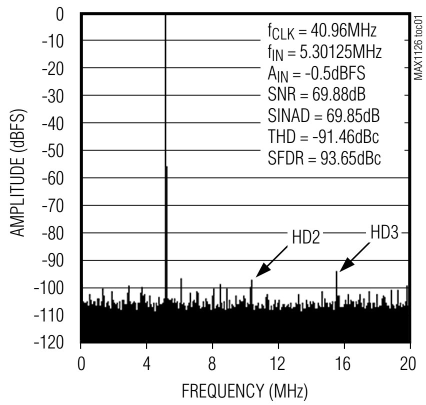
Note 7: Guaranteed by design and characterization. Not subject to production testing.

Note 8: Sample CLK Rise to FRAME RISE timing is measured from 50% of sample clock input level to 50% of FRAME output level.

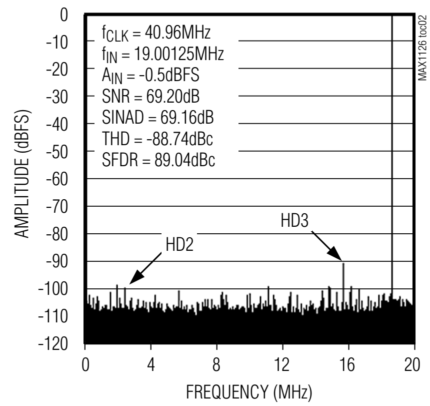
Typical Operating Characteristics

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

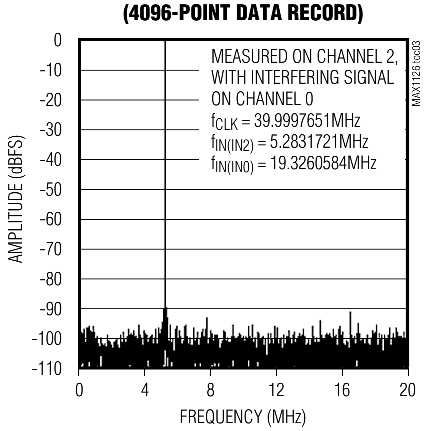
FFT PLOT (32,768-POINT DATA RECORD)



FFT PLOT (32,768-POINT DATA RECORD)



CROSSTALK (4096-POINT DATA RECORD)



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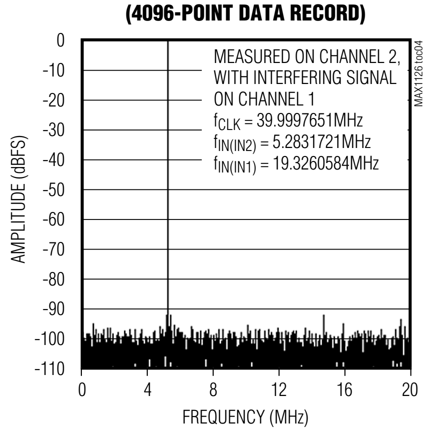
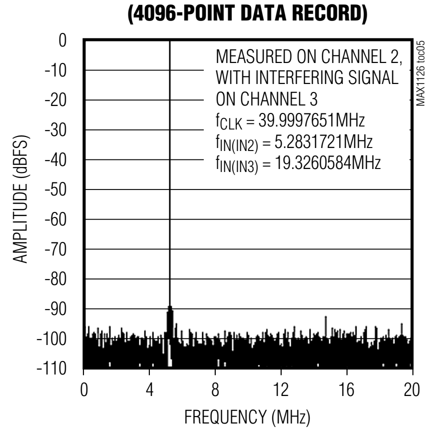
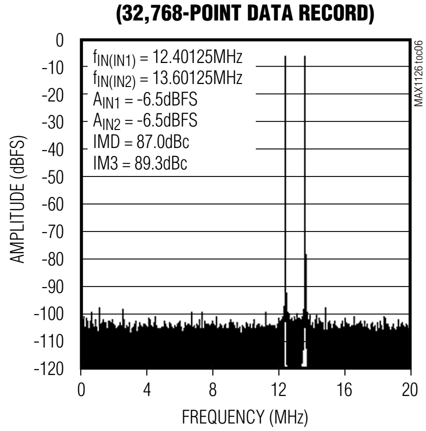


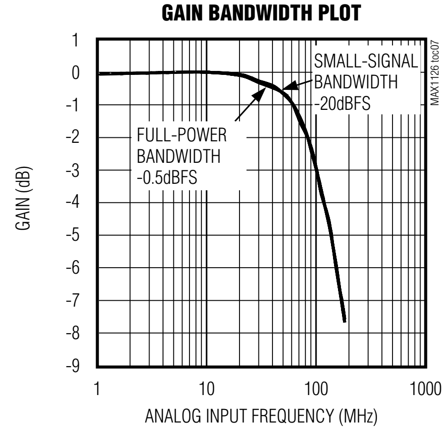
CROSSTALK (4096-POINT DATA RECORD)



TWO-TONE INTERMODULATION DISTORTION (32,768-POINT DATA RECORD)

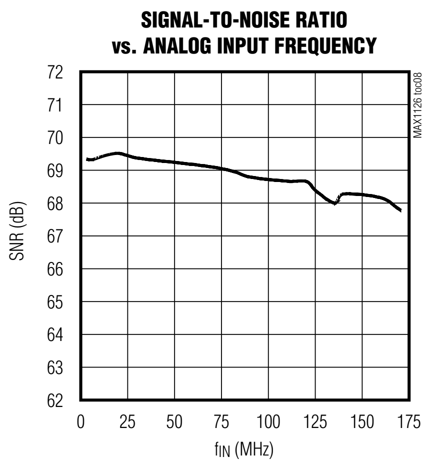


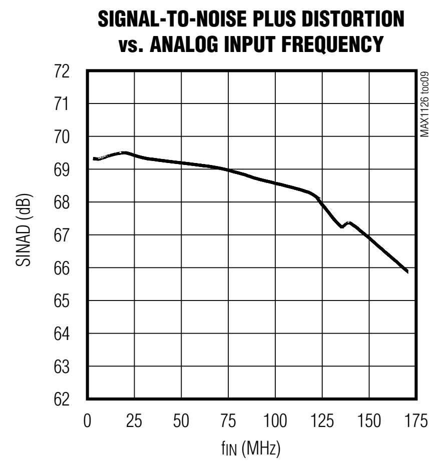
GAIN BANDWIDTH PLOT

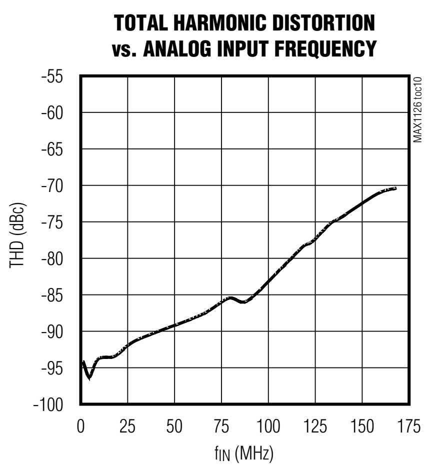


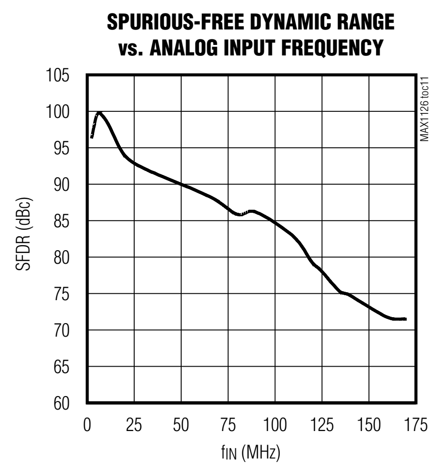
Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)









Typical Operating Characteristics (continued)

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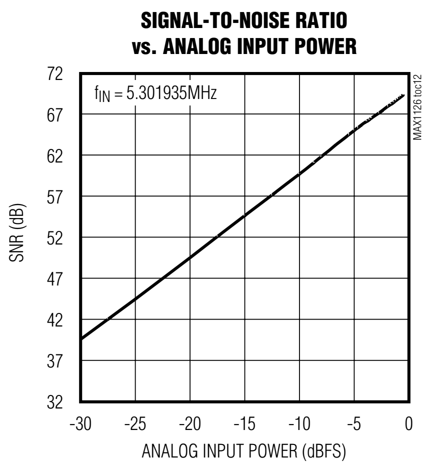
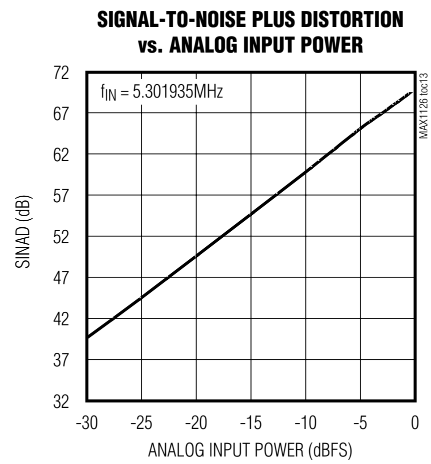
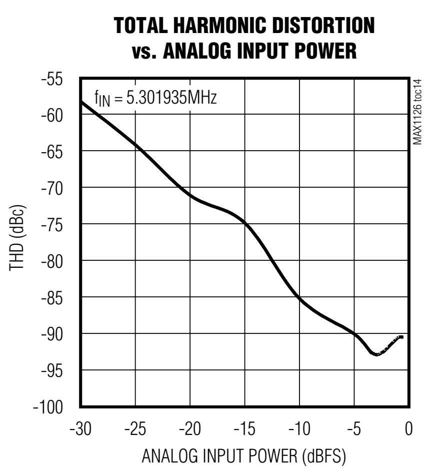
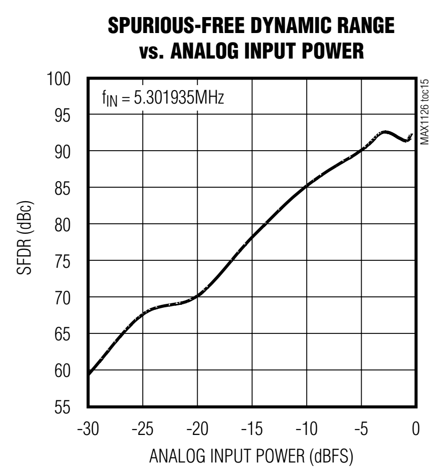




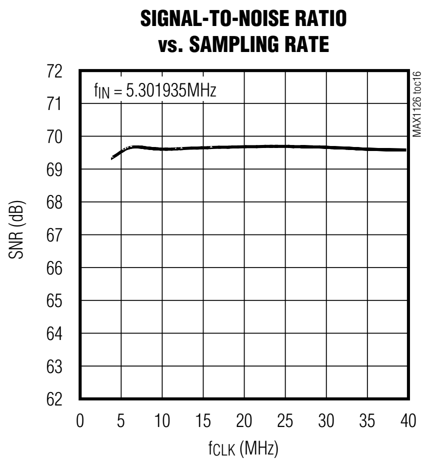


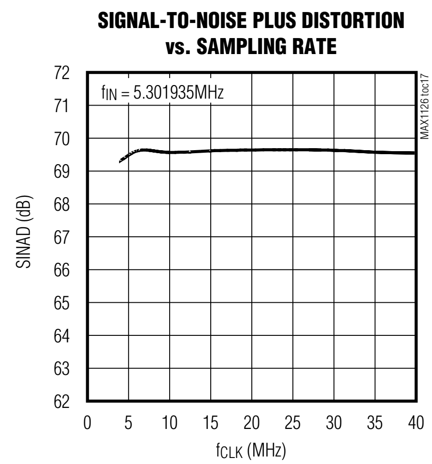


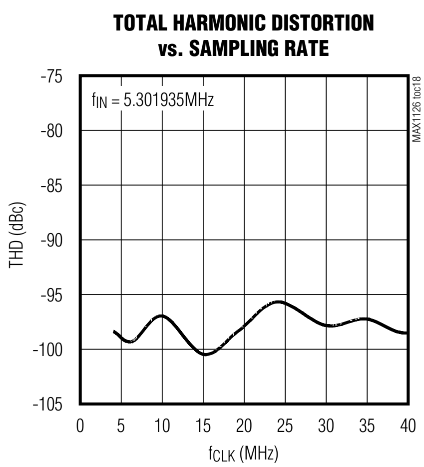
Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

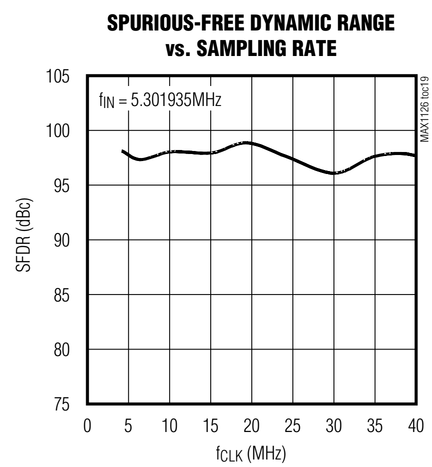
Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)



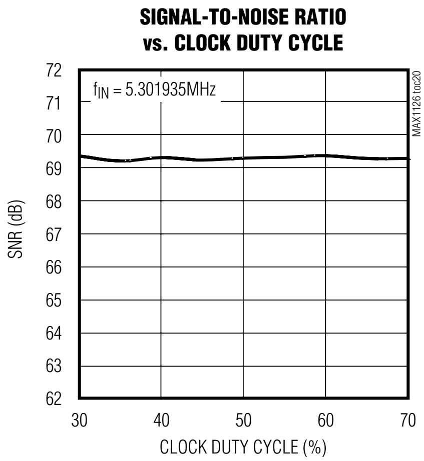


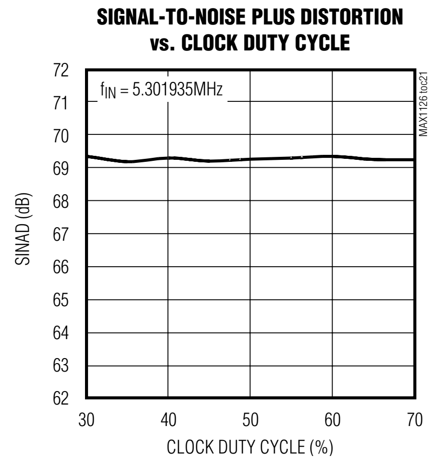


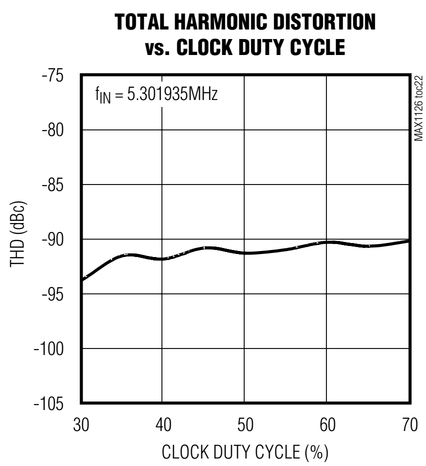


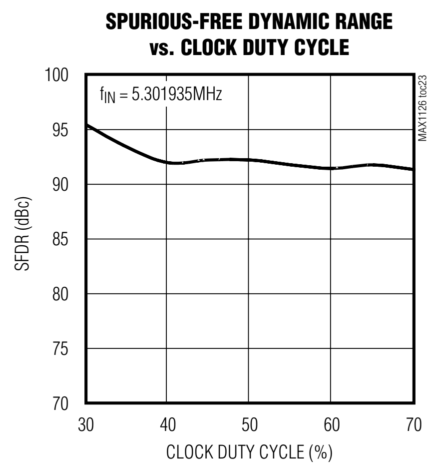
Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)







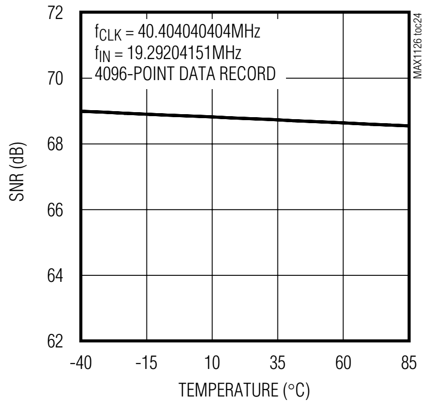


Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

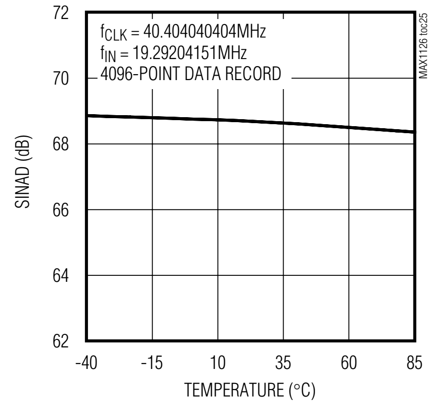
Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

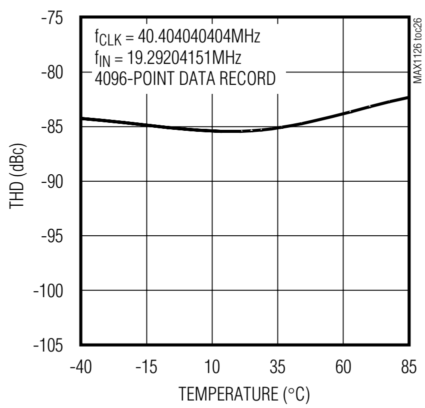
SIGNAL-TO-NOISE RATIO vs. TEMPERATURE



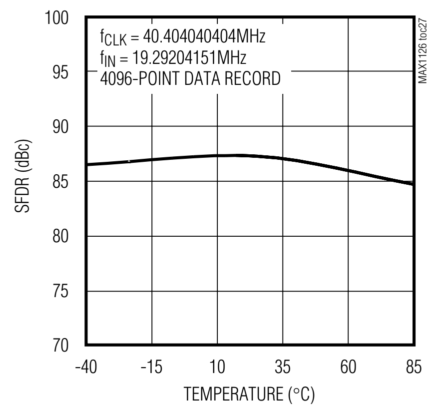
SIGNAL-TO-NOISE PLUS DISTORTION vs. TEMPERATURE



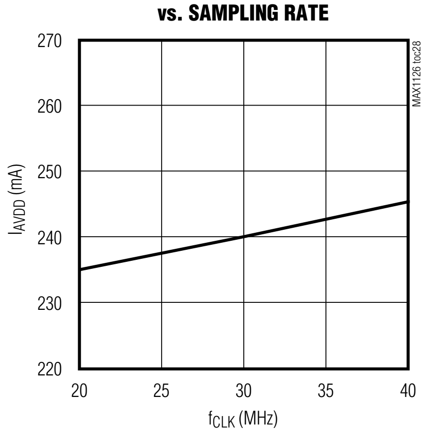
TOTAL HARMONIC DISTORTION vs. TEMPERATURE



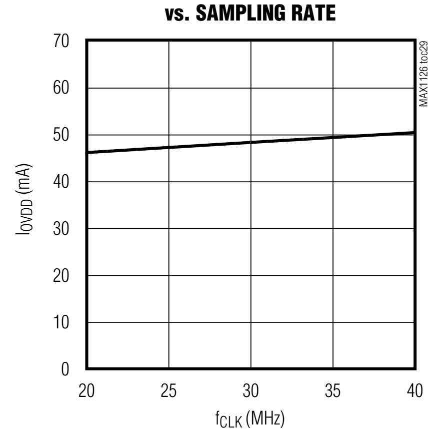
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



ANALOG SUPPLY CURRENT vs. SAMPLING RATE



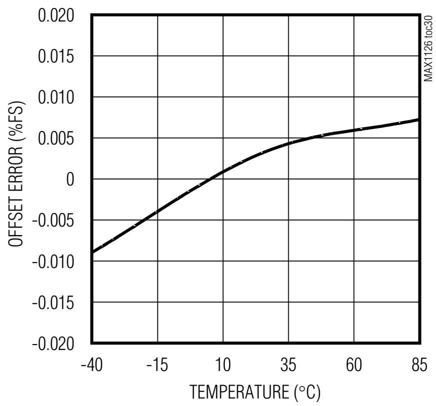
DIGITAL SUPPLY CURRENT vs. SAMPLING RATE



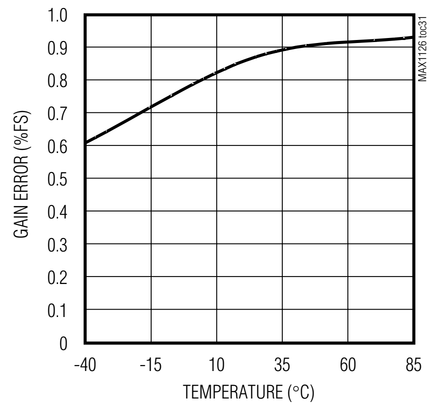
Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

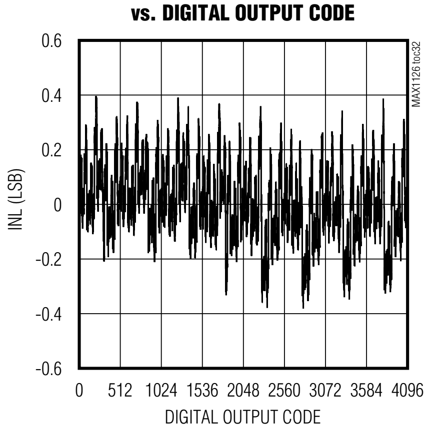
OFFSET ERROR vs. TEMPERATURE



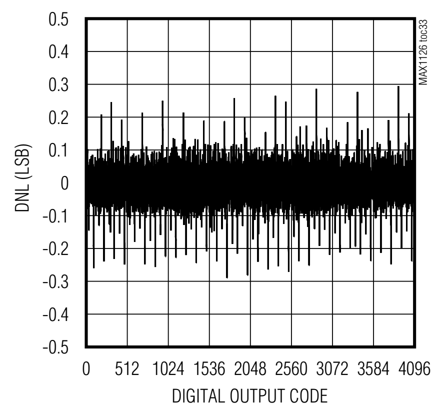
GAIN ERROR vs. TEMPERATURE



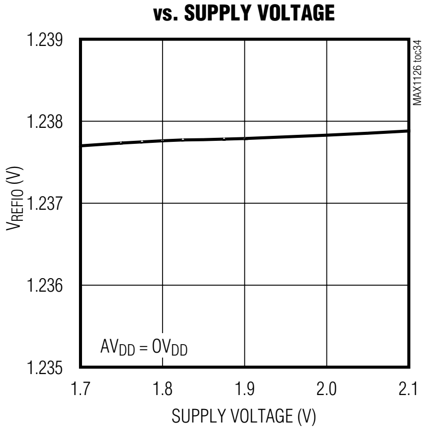
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



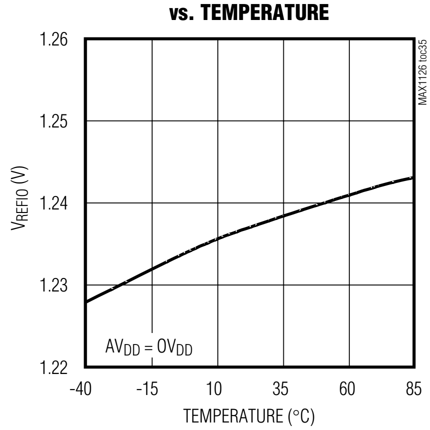
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



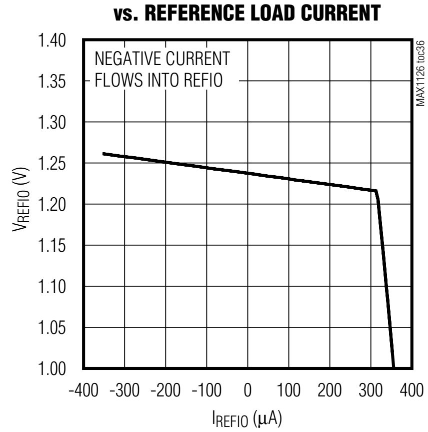
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



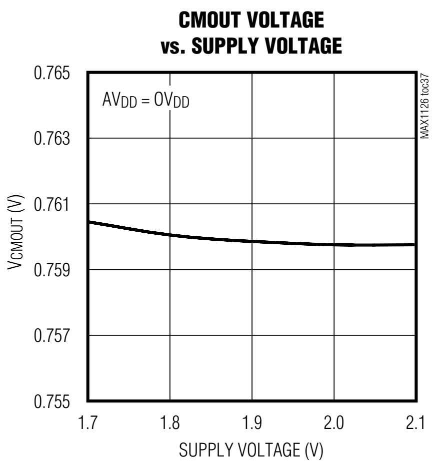
INTERNAL REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT

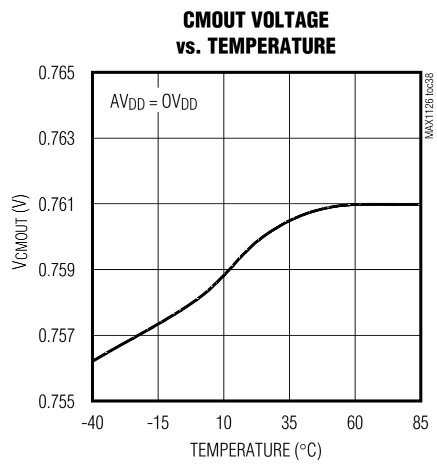


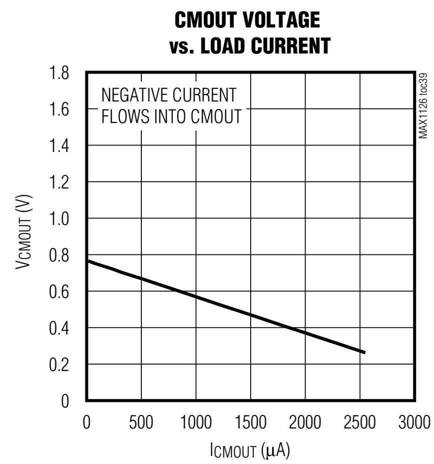
Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

Typical Operating Characteristics (continued)

(AV_{DD} = 1.8V, OV_{DD} = 1.8V, CV_{DD} = 1.8V, GND = 0, external V_{REFIO} = 1.24V, REFADJ = AV_{DD}, differential input at -0.5dBFS, f_{CLK} = 40MHz (50% duty cycle), DT = low, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)







Pin Description

PIN	NAME	FUNCTION
1, 4, 7, 11, 14, 17, 22, 24, 65, 68	GND	Ground. Connect all GND pins to the same potential.
2	IN0P	Channel 0 Positive Analog Input
3	IN0N	Channel 0 Negative Analog Input
5	IN1P	Channel 1 Positive Analog Input
6	IN1N	Channel 1 Negative Analog Input
8, 9, 10, 18, 20, 25, 26, 27, 58–62	AV_{DD}	Analog Power Input. Connect AV_{DD} to a 1.7V to 1.9V power supply. Bypass each AV_{DD} to GND with a 0.1µF capacitor as close to the device as possible. Bypass the AV_{DD} power plane to the GND ground plane with a bulk ≥ 2.2µF capacitor as close to the device as possible. Connect all AV_{DD} pins to the same potential.
12	IN2P	Channel 2 Positive Analog Input
13	IN2N	Channel 2 Negative Analog Input
15	IN3P	Channel 3 Positive Analog Input
16	IN3N	Channel 3 Negative Analog Input
19	CMOUT	Common-Mode Reference Voltage Output. Bypass CMOUT to GND with a 0.1µF capacitor.
21	CV_{DD}	Clock Power Input. Connect CV_{DD} to a 1.7V to 3.6V supply. Bypass CV_{DD} to GND with a 0.1µF capacitor in parallel with a ≥ 2.2µF capacitor. Install the bypass capacitors as close to the device as possible.
23	CLK	Single-Ended CMOS Clock Input
28	DT	Double Termination Select Input. Drive DT high to select the internal 100Ω termination between the differential output pairs. Drive DT low to select no internal output termination.

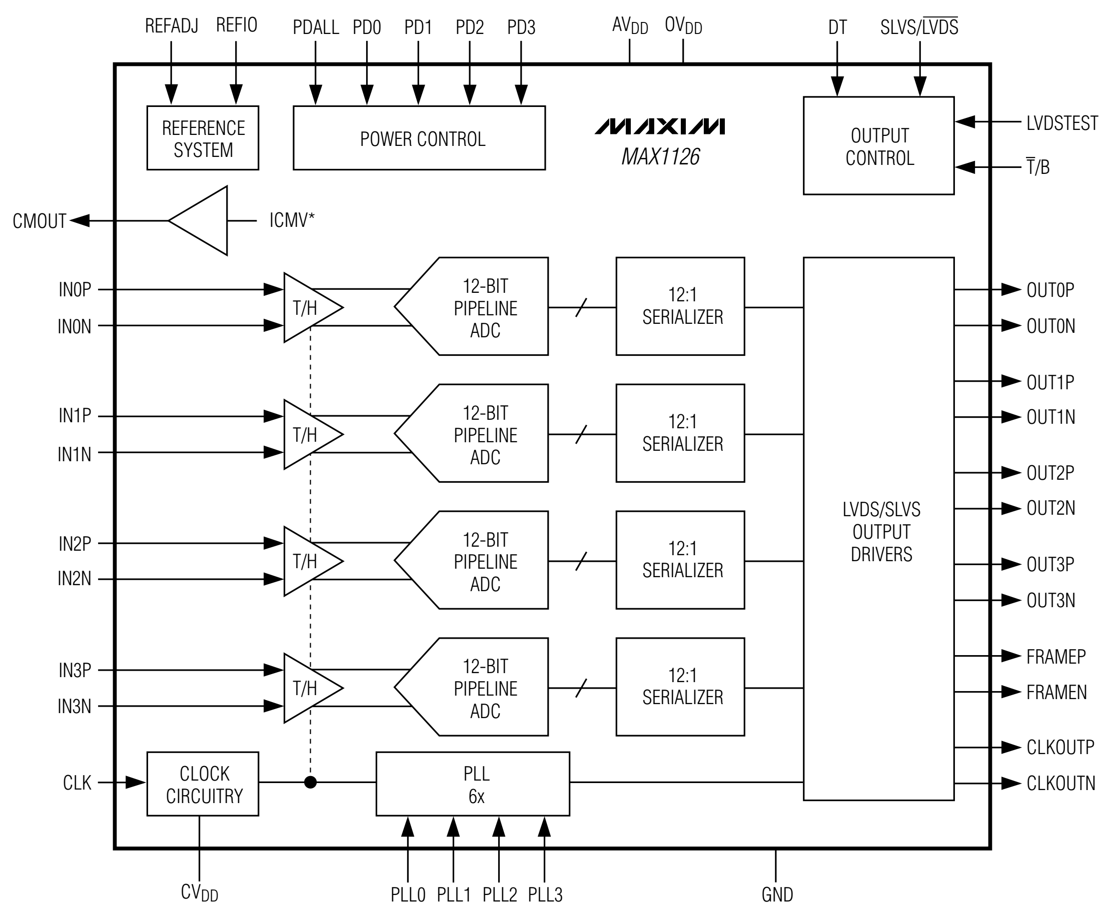
Pin Description (continued)

PIN	NAME	FUNCTION
29	SLVS/$\overline{\text{LVDS}}$	Differential Output Signal Format Select Input. Drive SLVS/$\overline{\text{LVDS}}$ high to select SLVS outputs. Drive SLVS/$\overline{\text{LVDS}}$ low to select LVDS outputs.
30	PLL0	PLL Control Input 0. PLL0 is reserved for factory testing only and must always be connected to GND.
31	PLL1	PLL Control Input 1. See Table 1 for details.
32	PLL2	PLL Control Input 2. See Table 1 for details.
33	PLL3	PLL Control Input 3. See Table 1 for details.
34, 37, 40, 43, 46, 49, 52	OV_{DD}	Output-Driver Power Input. Connect OV_{DD} to a 1.7V to 1.9V power supply. Bypass each OV_{DD} to GND with a 0.1µF capacitor as close to the device as possible. Bypass the OV_{DD} power plane to the GND ground plane with a bulk ≥2.2µF capacitor as close to the device as possible. Connect all OV_{DD} pins to the same potential.
35	OUT3N	Channel 3 Negative LVDS/SLVS Output
36	OUT3P	Channel 3 Positive LVDS/SLVS Output
38	OUT2N	Channel 2 Negative LVDS/SLVS Output
39	OUT2P	Channel 2 Positive LVDS/SLVS Output
41	FRAMEN	Negative Frame Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
42	FRAMEP	Positive Frame Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
44	CLKOUTN	Negative LVDS/SLVS Serial Clock Output
45	CLKOUTP	Positive LVDS/SLVS Serial Clock Output
47	OUT1N	Channel 1 Negative LVDS/SLVS Output
48	OUT1P	Channel 1 Positive LVDS/SLVS Output
50	OUT0N	Channel 0 Negative LVDS/SLVS Output
51	OUT0P	Channel 0 Positive LVDS/SLVS Output
53	PD0	Channel 0 Power-Down Input. Drive PD0 high to power-down channel 0. Drive PD0 low for normal operation.
54	PD1	Channel 1 Power-Down Input. Drive PD1 high to power-down channel 1. Drive PD1 low for normal operation.
55	PD2	Channel 2 Power-Down Input. Drive PD2 high to power-down channel 2. Drive PD2 low for normal operation.
56	PD3	Channel 3 Power-Down Input. Drive PD3 high to power-down channel 3. Drive PD3 low for normal operation.
57	PDALL	Global Power-Down Input. Drive PDALL high to power-down all channels and reference. Drive PDALL low for normal operation.
63	$\overline{\text{T}}$/B	Output Format Select Input. Drive $\overline{\text{T}}$/B high to select binary output format. Drive $\overline{\text{T}}$/B low to select two's complement output format.

Pin Description (continued)

PIN	NAME	FUNCTION
64	LVDSTEST	LVDS Test Pattern Enable Input. Drive LVDSTEST high to enable the output test pattern (000010111101 MSB→LSB). As with the analog conversion results, the test pattern data is output LSB first. Drive LVDSTEST low for normal operation.
66	REFIO	Reference Input/Output. For internal reference operation (REFADJ = GND), the reference output voltage is 1.24V. For external reference operation (REFADJ = AV_{DD}), apply a stable reference voltage at REFIO. Bypass to GND with a 0.1µF capacitor.
67	REFADJ	Internal/External Reference Mode Select Input. For internal reference mode, connect REFADJ directly to GND. For external reference mode, connect REFADJ directly to AV_{DD}. For reference-adjust mode, see the *Full-Scale Range Adjustments Using the Internal Reference* section.
—	EP	Exposed Paddle. EP is internally connected to GND. Externally connect EP to GND to achieve specified performance.

Functional Diagram



*ICMV = INPUT COMMON-MODE VOLTAGE (INTERNALLY GENERATED)

Detailed Description

The MAX1126 ADC features fully differential inputs, a pipelined architecture, and digital error correction for high-speed signal conversion. The ADC pipeline architecture moves the samples taken at the inputs through the pipeline stages every half clock cycle. The converted digital results are serialized and sent through the LVDS/SLVS output drivers. The total latency from input to output is 6.5 input clock cycles.

The MAX1126 offers four separate fully differential channels with synchronized inputs and outputs. Configure the outputs for binary or two's complement with the $\overline{T}$/B digital input. Power-down each channel individually or globally to minimize power consumption.

Input Circuit

Figure 1 displays a simplified functional diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the operational transconductance amplifier (OTA), and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. Analog inputs IN_P to IN_N are driven differentially. For differential inputs, balance the input impedance of IN_P and IN_N for optimum performance.

The MAX1126 analog inputs are self-biased at a common-mode voltage of 0.76V (typ) and allow a differential input voltage swing of $1.4V_{P-P}$. The common-mode voltage can be overdriven to between 0.55V and 0.85V. Drive the analog inputs of the MAX1126 in AC-coupled configuration to achieve best dynamic performance. See the *Using Transformer Coupling* section for a detailed discussion of this configuration.

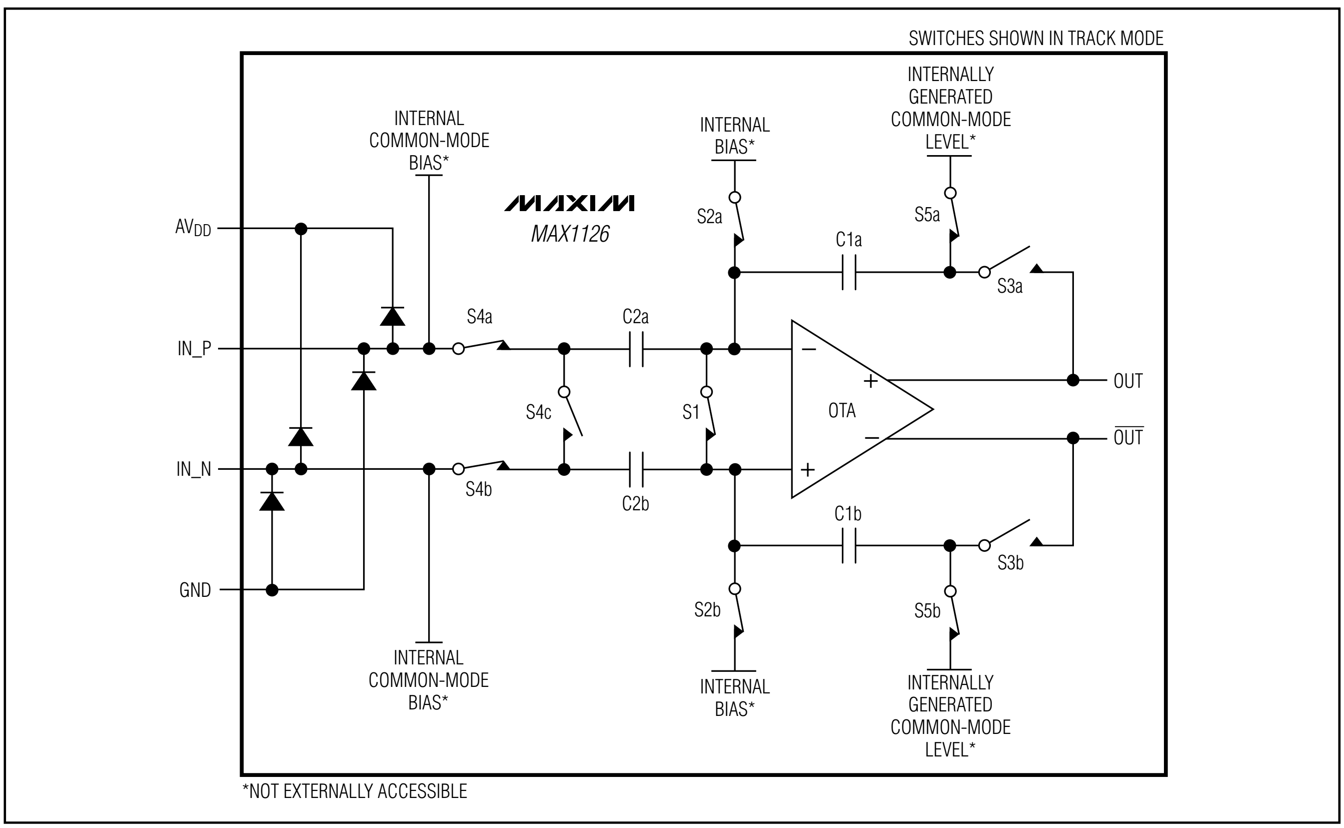


Figure 1. Internal Input Circuitry

Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

Reference Configurations (REFIO and REFADJ)

The MAX1126 provides an internal 1.24V bandgap reference or can be driven with an external reference voltage. The MAX1126 full-scale analog differential input range is ±FSR. Full-scale range (FSR) is given by the following equation:

$$FSR = 700mV \times \frac{V_{REFIO}}{1.24V}$$

where V_{REFIO} is the voltage at REFIO, generated internally or externally. For a V_{REFIO} = 1.24V, the full-scale input range is ±700mV (1.4V_{P-P}).

Internal Reference Mode

Connect REFADJ to GND to use the internal bandgap reference directly. The internal bandgap reference generates REFIO to be 1.24V with a 100ppm/°C temperature coefficient in internal reference mode. Connect an external ≥ 0.1µF bypass capacitor from REFIO to GND for stability. REFIO sources up to 200µA and sinks up to 200µA for external circuits, and REFIO has a load regulation of 83mV/mA. The global power-down input (PDALL) enables and disables the reference circuit. REFIO has > 1MΩ resistance to GND when the MAX1126 is in power-down mode. The internal reference circuit requires 132µs to power-up and settle when power is applied to the MAX1126 or when PDALL transitions from high to low.

To compensate for gain errors or to decrease or increase the ADC's full-scale range (FSR), add an external resistor between REFADJ and GND or REFADJ and REFIO. This adjusts the internal reference value of the MAX1126 by up to ±5% of its nominal value. See the *Full-Scale Range Adjustments Using the Internal Reference* section.

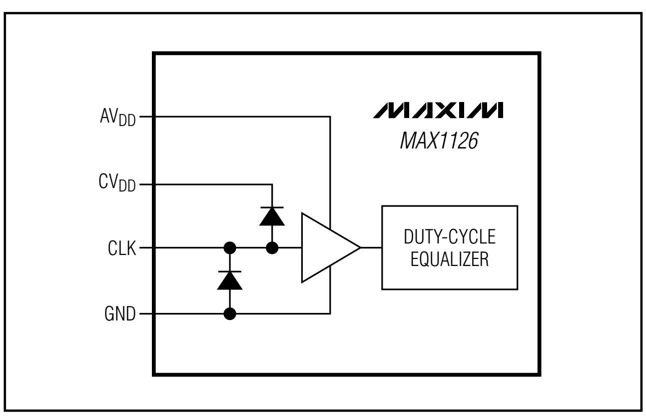


Figure 2. Clock Input Circuitry

External Reference Mode

The external reference mode allows for more control over the MAX1126 reference voltage and allows multiple converters to use a common reference. Connect REFADJ to AV_{DD} to disable the internal reference and enter external reference mode. Apply a stable 1.18V to 1.30V source at REFIO. Bypass REFIO to GND with a 0.1µF capacitor. The REFIO input impedance is > 1MΩ.

Clock Input (CLK)

The MAX1126 accepts a CMOS-compatible clock signal with a wide 20% to 80% input-clock duty cycle. Drive CLK with an external single-ended clock signal. Figure 2 shows the simplified clock input diagram.

Low clock jitter is required for the specified SNR performance of the MAX1126. Analog input sampling occurs on the rising edge of CLK, requiring this edge to provide the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter. Clock jitter is especially critical for undersampling applications. For example, assuming that clock jitter is the only noise source, to obtain the specified 69.2dB of SNR with an input frequency of 19.3MHz, the system must have less than 2.8ps_{RMS} of clock jitter. In actuality, there are other noise sources, such as thermal noise and quantization noise, that contribute to the system noise requiring the clock jitter to be less than 1.1ps_{RMS} to obtain the specified 69.2dB of SNR at 19.3MHz.

Table 1. PLL1, PLL2, and PLL3 Configuration

PLL1	PLL2	PLL3	CLOCK INPUT RANGE (MHz)	
			MIN	MAX
0	0	0	NOT USED	
0	0	1	32.5	40.0
0	1	0	22.5	32.5
0	1	1	16.3	22.5
1	0	0	11.3	16.3
1	0	1	8.1	11.3
1	1	0	5.6	8.1
1	1	1	4.0	5.6

**PLL0 is reserved for factory testing and must always be connected to GND.*

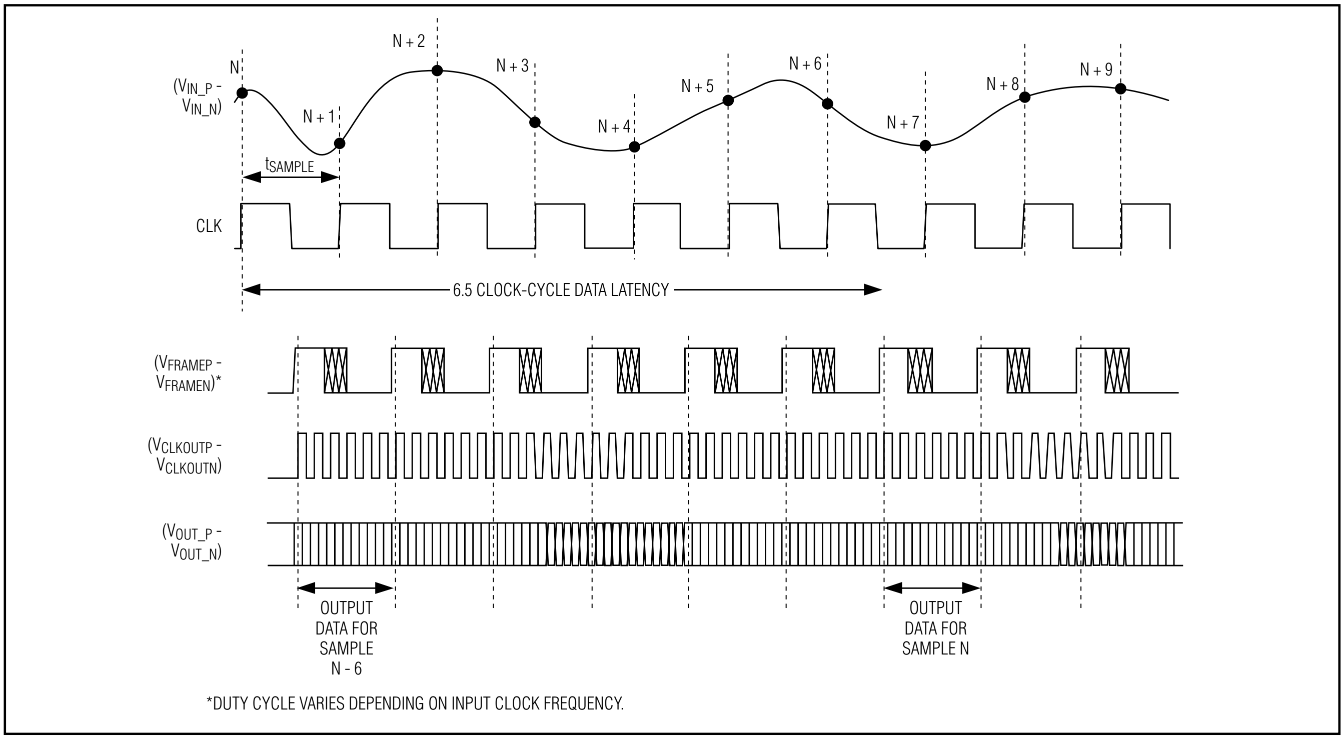


Figure 3. Global Timing Diagram

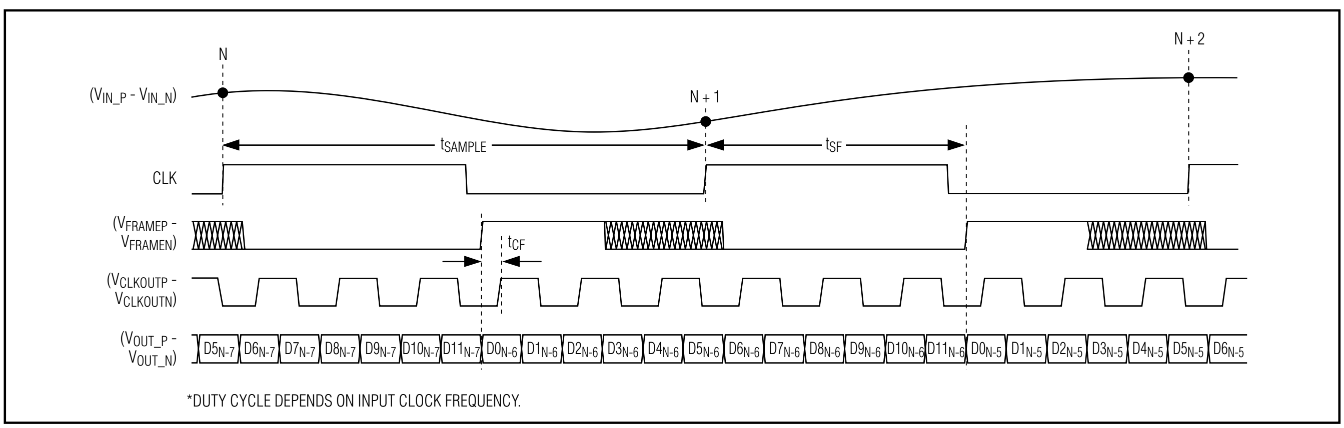


Figure 4. Detailed Two-Conversion Timing Diagram

PLL Inputs (PLL0–PLL3)

The MAX1126 features a PLL that generates an output clock signal with 6 times the frequency of the input clock. The output clock signal is used to clock data out of the MAX1126 (see the *System Timing Requirements* section). Set the PLL1, PLL2, and PLL3 bits according to the input clock range provided in Table 1. PLL0 is reserved for factory testing and must always be connected to GND.

System Timing Requirements

Figure 3 shows the relationship between the analog inputs, input clock, frame alignment output, serial clock output, and serial data output. The differential analog input (IN_P and IN_N) is sampled on the rising edge of the CLK signal and the resulting data appears at the digital outputs 6.5 clock cycles later. Figure 4 provides a detailed, two-conversion timing diagram of the relationship between the inputs and the outputs.

Quad, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

Clock Output (CLKOUTP, CLKOUTN)

The MAX1126 provides a differential clock output that consists of CLKOUTP and CLKOUTN. As shown in Figure 4, the serial output data is clocked out of the MAX1126 on both edges of the clock output. The frequency of the output clock is 6 times the frequency of CLK.

Frame Alignment Output (FRAMEP, FRAMEN)

The MAX1126 provides a differential frame alignment signal that consists of FRAMEP and FRAMEN. As shown in Figure 4, the rising edge of the frame alignment signal corresponds to the first bit (D0) of the 12-bit serial data stream. The frequency of the frame alignment signal is identical to the frequency of the sample clock.

Serial Output Data (OUT_P, OUT_N)

The MAX1126 provides its conversion results through individual differential outputs consisting of OUT_P and OUT_N. The results are valid 6.5 input clock cycles after the sample is taken. As shown in Figure 3, the output data is clocked out on both edges of the output clock, LSB (D0) first. Figure 5 provides the detailed serial output timing diagram.

Output Data Format ($\overline{T}$/B), Transfer Functions

The MAX1126 output data format is either offset binary or two's complement, depending on the logic input $\overline{T}$/B. With $\overline{T}$/B low, the output data format is two's complement. With $\overline{T}$/B high, the output data format is offset binary. The following equations, Table 2, Figure 6, and Figure 7 define the relationship between the digital

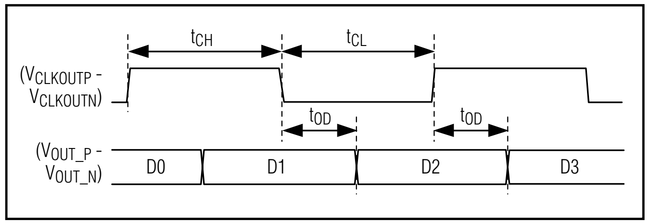


Figure 5. Serialized Output Detailed Timing Diagram

output and the analog input. For two's complement ($\overline{T}$/B = 0):

$$V_{IN\_P} - V_{IN\_N} = FSR \times 2 \times \frac{CODE_{10}}{4096}$$

and for offset binary ($\overline{T}$/B = 1):

$$V_{IN\_P} - V_{IN\_N} = FSR \times 2 \times \frac{CODE_{10} - 2048}{4096}$$

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 2. FSR is the full-scale range as shown in Figures 6 and 7.

Keep the capacitive load on the MAX1126 digital outputs as low as possible.

LVDS and SLVS Signals (SLVS/$\overline{LVDS}$)

Drive SLVS/$\overline{LVDS}$ low for LVDS or drive SLVS/$\overline{LVDS}$ high for scalable low-voltage signaling (SLVS) levels at the MAX1126 outputs (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN). For SLVS levels,

Table 2. Output Code Table (V_{REFIO} = 1.24V)

TWO'S COMPLEMENT DIGITAL OUTPUT CODE ($\overline{T}$/B = 0)			OFFSET BINARY DIGITAL OUTPUT CODE ($\overline{T}$/B = 1)			V_{IN_P} - V_{IN_P} (mV) (V_{REFIO} = 1.24V)
BINARY D11 → D0	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0	BINARY D11 → D0	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0	
0111 1111 1111	0x7FF	+2047	1111 1111 1111	0xFFF	+4095	+699.66
0111 1111 1110	0x7FE	+2046	1111 1111 1110	0xFFE	+4094	+699.32
0000 0000 0001	0x001	+1	1000 0000 0001	0x801	+2049	+0.34
0000 0000 0000	0x000	0	1000 0000 0000	0x800	+2048	0
1111 1111 1111	0xFFF	-1	0111 1111 1111	0x7FF	+2047	-0.34
1000 0000 0001	0X801	-2047	0000 0000 0001	0x001	+1	-699.66
1000 0000 0000	0x800	-2048	0000 0000 0000	0x000	0	-700.00

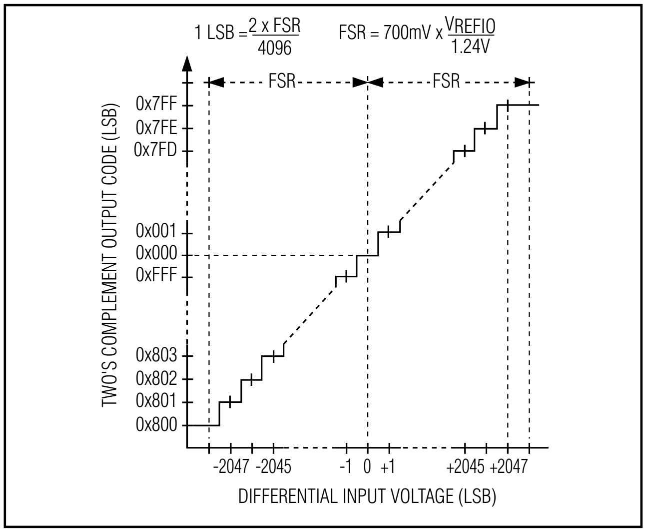


Figure 6. Bipolar Transfer Function with Two's Complement Output Code ($\overline{T}$/B = 0)

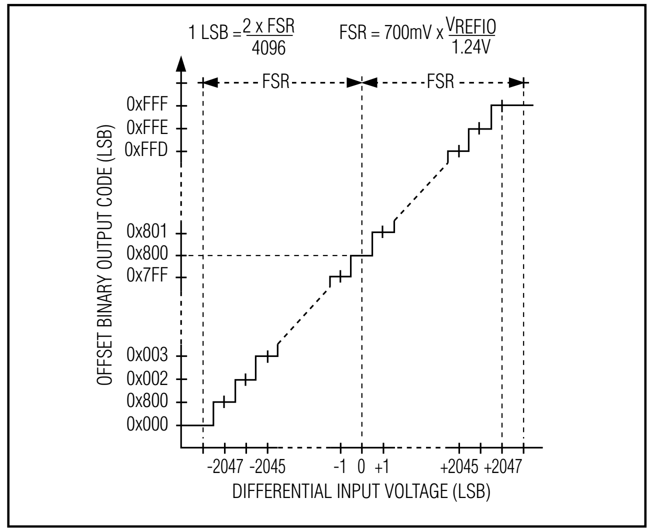


Figure 7. Bipolar Transfer Function with Offset Binary Output Code ($\overline{T}$/B = 1)

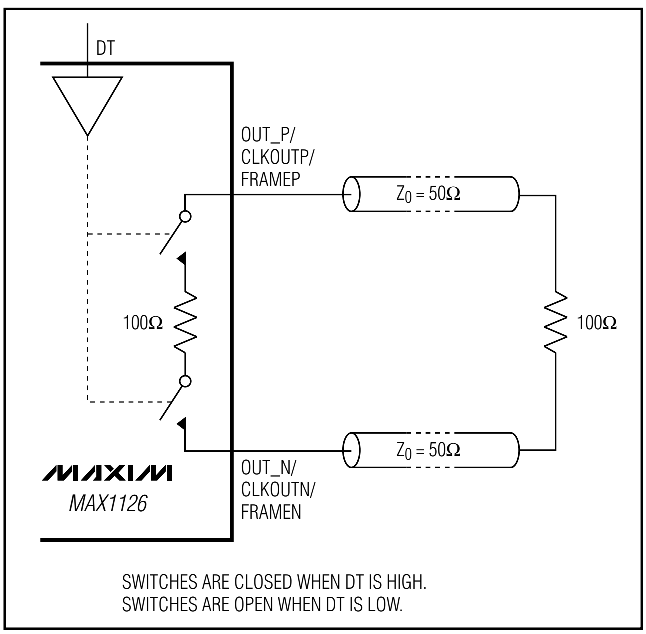


Figure 8. Double Termination

enable double termination by driving DT high. See the *Electrical Characteristics* table for LVDS and SLVS output voltage levels.

LVDS Test Pattern (LVDSTEST)

Drive LVDSTEST high to enable the output test pattern on all LVDS or SLVS output channels. The output test pattern is 0000 1011 1101 MSB→LSB. As with the analog conversion results, the test pattern data is output LSB first. Drive LVDSTEST low for normal operation (test pattern disabled).

Common-Mode Output Voltage (CMOUT)

CMOUT provides a common-mode reference for DC-coupled analog inputs. If the input is DC-coupled, match the output common-mode voltage of the circuit driving the MAX1126 to the output voltage at V_{CMOUT} to within ±50mV. It is recommended that the output common-mode voltage of the driving circuit be derived from CMOUT.

Double Termination (DT)

As shown in Figure 8, the MAX1126 offers an optional, internal 100Ω termination between the differential output pairs (OUT_P and OUT_N, CLKOUTP and CLKOUTN, FRAMEP and FRAMEN). In addition to the termination at the end of the line, a second termination directly at the outputs helps eliminate unwanted reflections down the line. This feature is useful in applications where trace lengths are long (> 5in) or with mismatched impedance. Drive DT high to select double termination, or drive DT low to disconnect the internal termination resistor (single termination). Selecting double termination increases the OV_{DD} supply current (see the *Electrical Characteristics* table).

Power-Down Modes

The MAX1126 offers two types of power-down inputs, PD0–PD3 and PDALL. The power-down modes allow the MAX1126 to efficiently use power by transitioning to a low-power state when conversions are not required.

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Independent Channel Power-Down (PD0–PD3)

PD0–PD3 control the power-down mode of each channel independently. Drive a power-down input high to power down its corresponding input channel. For example, to power down channel 1, drive PD1 high. Drive a power-down input low to place the corresponding input channel in normal operation. The differential output impedance of a powered-down output channel is approximately 378Ω, when DT is low. The output impedance of OUT_P, with respect to OUT_N, is 100Ω when DT is high. See the *Electrical Characteristics* table for typical supply currents with powered-down channels.

The state of the internal reference is independent of the PD0–PD3 inputs. To power down the internal reference circuitry, drive PDALL high (see the *Global Power-Down (PDALL)* section).

Global Power-Down (PDALL)

PDALL controls the power-down mode of all channels and the internal reference circuitry. Drive PDALL high to enable global power-down. In global power-down mode, the output impedance of all the LVDS/SLVS outputs is approximately 378Ω, if DT is low. The output impedance of the differential LVDS/SLVS outputs is 100Ω when DT is high. See the *Electrical Characteristics* table for typical supply currents with global power-down. The following list shows the state of the analog inputs and digital outputs in global power-down mode:

- IN_P, IN_N analog inputs are disconnected from the internal input amplifier.
- REFIO has > 1MΩ resistance to GND.
- OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN have approximately 378Ω between the output pairs when DT is low. When DT is high, the differential output pairs have 100Ω between each pair.

When operating from the internal reference, the wake-up time from global power-down is typically 132µs. When using an external reference, the wake-up time is dependent on the external reference drivers.

Applications Information

Full-Scale Range Adjustments Using the Internal Reference

The MAX1126 supports a full-scale adjustment range of 10% (±5%). To decrease the full-scale range, add a 25kΩ to 250kΩ external resistor or potentiometer (R_{ADJ}) between REFADJ and GND. To increase the full-scale range, add a 25kΩ to 250kΩ resistor between REFADJ and REFIO. Figure 9 shows the two possible configurations.

The following equations provide the relationship between R_{ADJ} and the change in the analog full-scale range:

$$FSR = 0.7V\left(1 + \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and REFIO, and

$$FSR = 0.7V\left(1 - \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and GND.

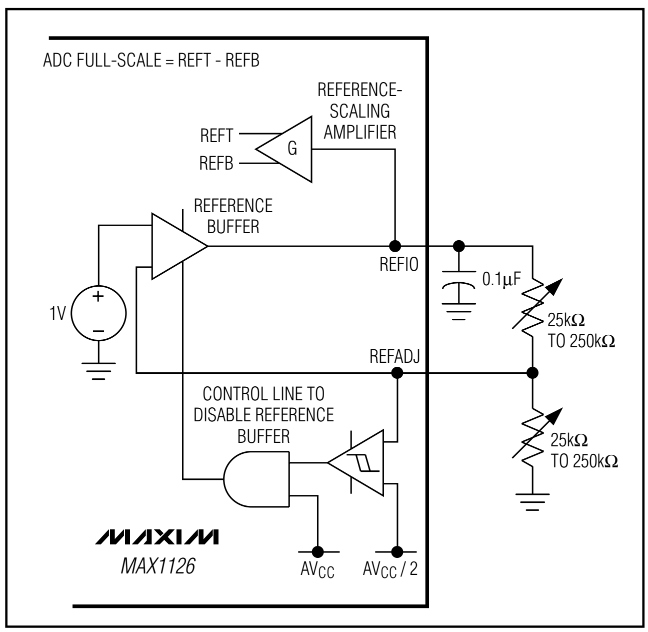

Figure 9. Circuit Suggestions to Adjust the ADC's Full-Scale Range

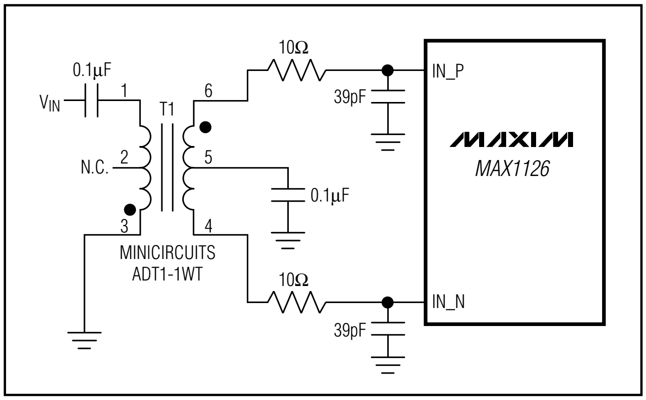

Figure 10. Transformer-Coupled Input Drive

Using Transformer Coupling

An RF transformer (Figure 10) provides an excellent solution to convert a single-ended input source signal to a fully differential signal, required by the MAX1126 for optimum performance. The MAX1126 input common-mode voltage is internally biased to 0.76V (typ) with f_{CLK} = 40MHz. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion.

Grounding, Bypassing, and Board Layout

The MAX1126 requires high-speed board layout design techniques. Refer to the MAX1127 EV kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass AV_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a ≥ 2.2µF ceramic capacitor. Bypass OV_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a ≥ 2.2µF ceramic capacitor. Bypass CV_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a ≥ 2.2µF ceramic capacitor.

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. Connect MAX1126 ground pins and the exposed backside paddle to the same ground plane. The MAX1126 relies on the exposed backside paddle connection for a low-inductance ground connection. Isolate the ground plane from any noisy digital system ground planes.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX1126 EV kit data sheet for an example of symmetric input layout.

Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For the MAX1126, this straight line is between the end points of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX1126, DNL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. For the MAX1126, the ideal midscale digital output transition occurs when there is -1/2 LSB across the analog inputs (Figures 6 and 7). Bipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1126, the gain error is the difference of the measured full-scale and zero-scale transition points minus the difference of the ideal full-scale and zero-scale transition points.

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For the bipolar devices (MAX1126), the full-scale transition point is from 0x7FE to 0x7FF for two's complement output format (0xFFE to 0xFFF for offset binary) and the zero-scale transition point is from 0x800 to 0x801 for two's complement (0x000 to 0x001 for offset binary).

Crosstalk

Crosstalk indicates how well each analog input is isolated from the others. For the MAX1126, a 5.3MHz, -0.5dBFS analog signal is applied to one channel while a 19.3MHz, -0.5dBFS analog signal is applied to all other channels. An FFT is taken on the channel with the 5.3MHz analog signal. From this FFT, the crosstalk is measured as the difference in the 5.3MHz and 19.3MHz amplitudes.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken. See Figure 10.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay. See Figure 11.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc.

For the MAX1126, SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

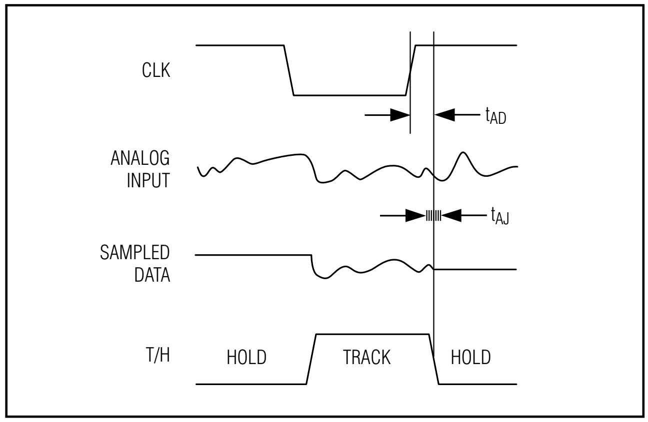

Figure 11. Aperture Jitter/Delay Specifications

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency, excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2 + V_7{}^2}}{V_1}\right)$$

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, f1 and f2. The individual input tone levels are at -6.5dBFS. The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): f1 + f2, f2 - f1
- 3rd-order intermodulation products (IM3): 2 x f1 - f2, 2 x f2 - f1, 2 x f1 + f2, 2 x f2 + f1
- 4th-order intermodulation products (IM4): 3 x f1 - f2, 3 x f2 - f1, 3 x f1 + f2, 3 x f2 + f1
- 5th-order intermodulation products (IM5): 3 x f1 - 2 x f2, 3 x f2 - 2 x f1, 3 x f1 + 2 x f2, 3 x f2 + 2 x f1

Third-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones f1 and f2. The individual input tone levels are at -6.5dBFS. The 3rd-order intermodulation products are 2 x f1 - f2, 2 x f2 - f1, 2 x f1 + f2, 2 x f2 + f1.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC so the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Gain Matching

Gain matching is a figure of merit that indicates how well the gain of all four ADC channels is matched to each other. For the MAX1126, gain matching is measured by applying the same 19.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 40MHz and the maximum deviation in amplitude is reported in dB as gain matching in the *Electrical Characteristics* table.

Phase Matching

Phase matching is a figure of merit that indicates how well the phase of all four ADC channels is matched to each other. For the MAX1126, phase matching is measured by applying the same 19.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 40MHz and the maximum deviation in phase is reported in degrees as phase matching in the *Electrical Characteristics* table.

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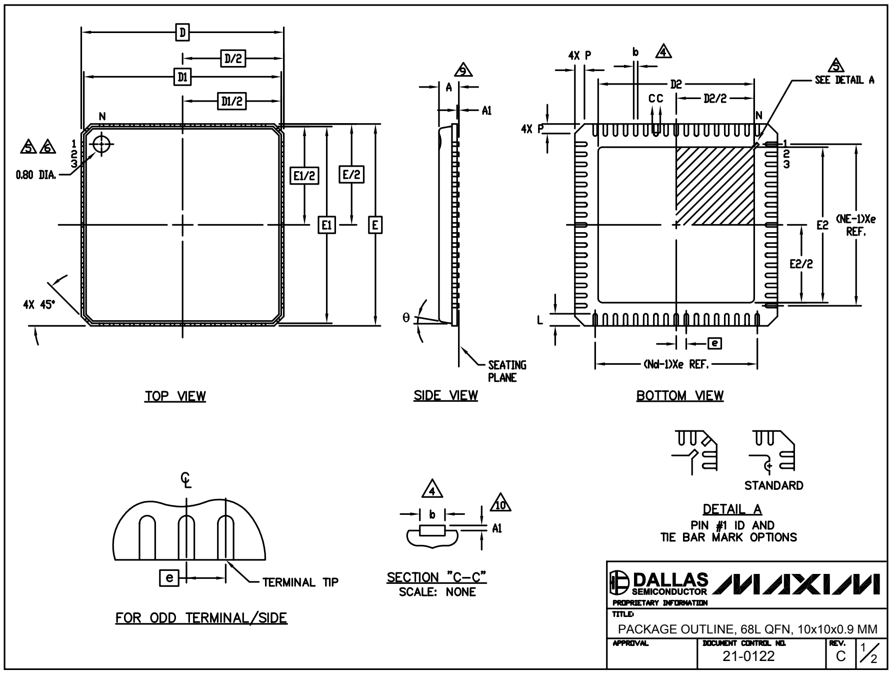
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

Note: For the MAX1126 Exposed Pad Variation, the package code is G6800-4.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0122 | REV. C | 2/2

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