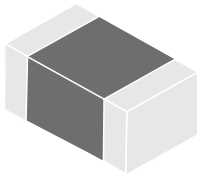
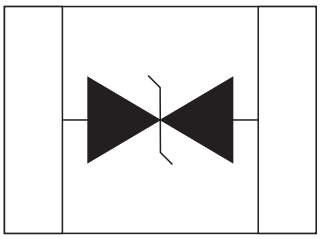
Electro-Static Discharge for Aotomobile
AUSD05BT
Low Capacitance Bidirection ESD Protection

0402



Pin Configuration



Features

- With TVS Diode
- ESD Protection:Level 4
- Low clamping voltage
- 45 Watts peak pulse power per line(tp=8/20μs)
- Ultra low capacitance:0.3pf typ.(any I/O to GND.)
- Protection one line I/O port
- AEC-Q101

IEC Compatibility

- IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
- IEC61000-4-4 (EFT) :40A (5/50ηs)
- IEC61000-4-5(Surge):2A(8/20μs)
- EN61000-4

Applications

- Lan equipment
- Cellphone/Tablet
- DVI
- High Speed Data Line
- Ethernet
- USB 2.0 Power and Data line Protection

Mechanical Characteristics

- JEDEC 0402 Package
- Molding Compound Flammability Rating : UL 94V-O
- Quantity Per Reel : 10,000pcs
- Reel Size : 7 inch
- Halgen Free

Maximum Ratings(T_A=25℃ unless otherwise specified)

Parameter	Symbol	Value	Units
Peak Pulse Power(tp=8/20μs)	P_{PP}	45	Watts
Lead Soldering Temperature	T_L	260(10 sec.)	℃
Operating Temperature Range	T_J	-55~150	℃
Storage Temperature Range	T_{STG}	-55~150	℃

Electrical Characteristics(T_A=25℃ unless otherwise specified)

AUSD05BT(Marking:L)

Parameter	Symbol	Conditions	Min.	Max.	Units
Reverse Stand-off Voltage	V_{RWM}			5	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	7	11	V
Reverse Leakage Current	I_R	@V_{RWM}		0.1	μA
Clamping Voltage	V_C	I_{PP}=1A,tp=8/20μs		15	V
Peak Pulse Current	I_{PP}	tp=8/20μs		2	A
Junction Capacitance	$C_{I/O}$	0Vdc,f=1MHz Between I/O Pins and GND		0.5	pF

Ratings and Characteristic Curves

Fig.1 Power Derating Curve

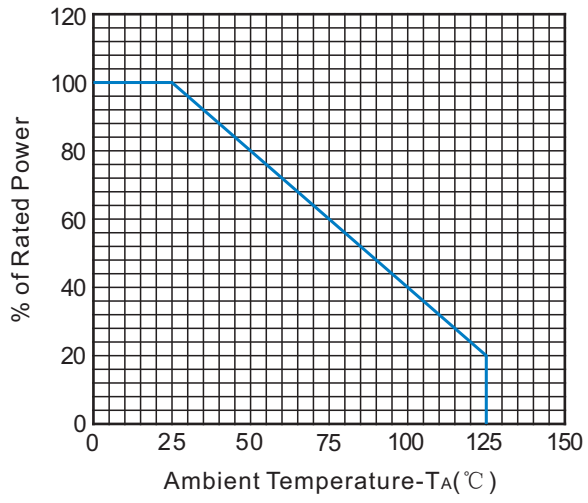
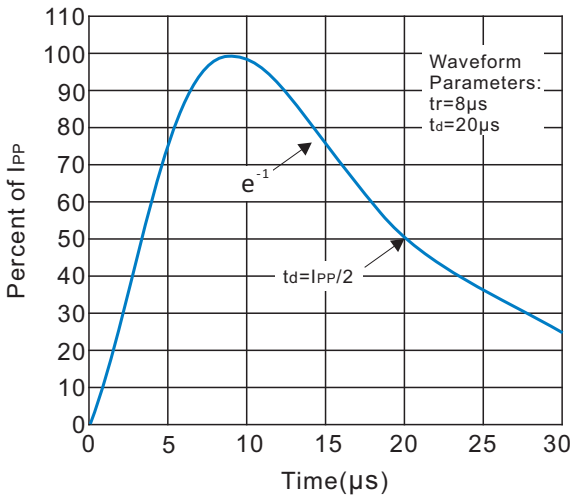


Fig.2 Pulse Waveform



Ratings and Characteristic Curves

Fig.3 ESD Clamping of I/O_1 to I/O_2
(+8kV Contact per IEC61000-4-2)

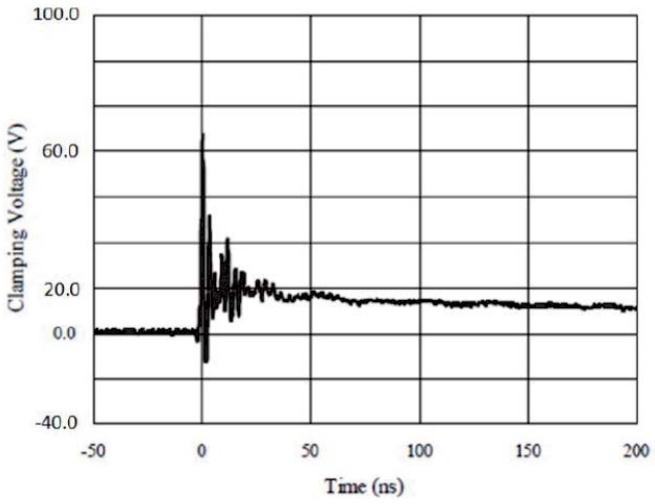
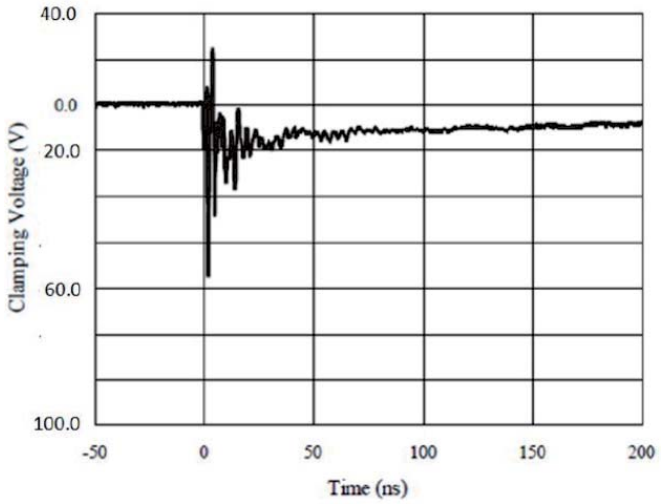
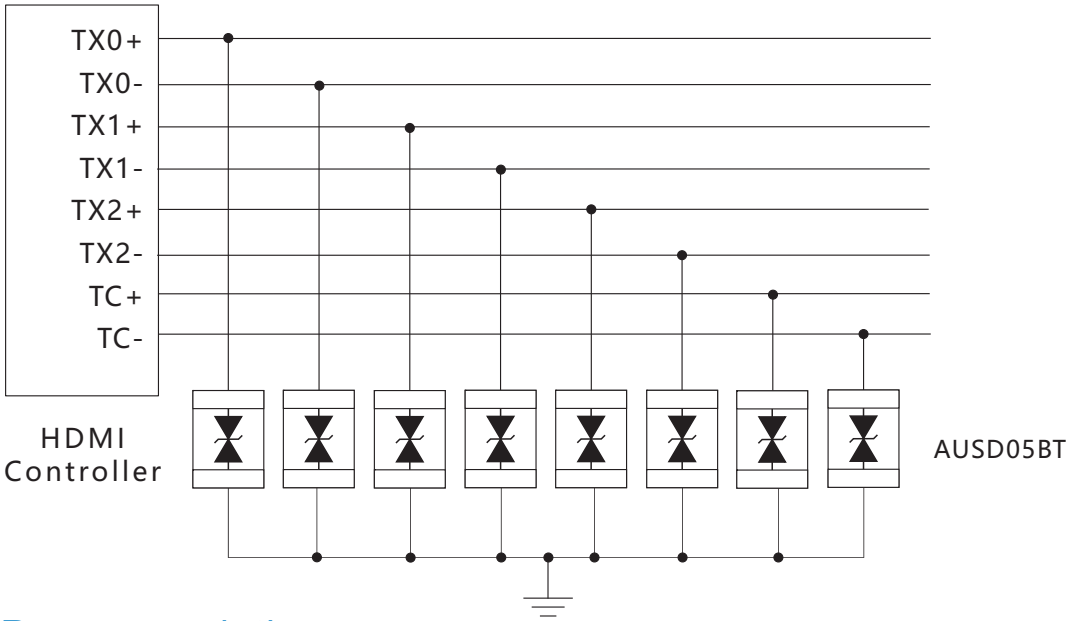


Fig.4 ESD Clamping of I/O_1 to I/O_2
(-8kV Contact per IEC61000-4-2)



Application Information

HDMI Protection



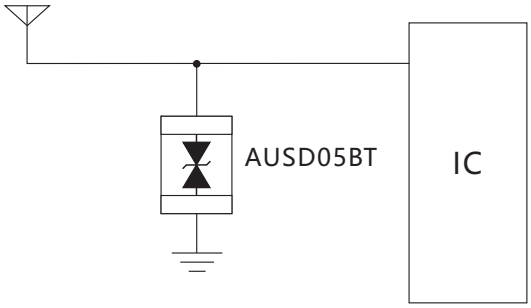
PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the HDMI protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the HDMI connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high.speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

Application Information

RF Protection

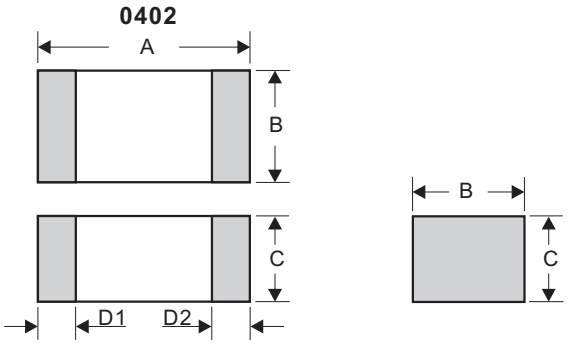


PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the RF protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the RF connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high.speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

Dimensions(0402)



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
B	0.50	0.70	0.020	0.027
C		0.60		0.023
D1/D2	0.10	0.40	0.004	0.016

Recommended Mounting Pad Layout