1GB DDR2 – SDRAM SO-DIMM

200 Pin SO-DIMM

SEN01G64E1CH2MT-30

1024MB PC2-5300 in FBGA Technique

RoHS compliant

Options:

- Frequency / Latency — Marking
  DDR2 667 MHz CL5 — -30
- Module densities
  1024MB with 8 dies and 2 ranks
- Standard Grade (t_A) 0℃ to 70℃
  (t_C) 0℃ to 85℃

Environmental Requirements:

- Operating temperature (ambient)
  Standard Grade 0℃ to 70℃
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55℃ to 100℃
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50℃

Features:

- 200-pin 64-bit Small Outline, Dual-In-Line Double Data Rate synchronous DRAM Module
- Module organization: dual rank 128M x 64
- Serial Presence Detect with EEPROM
- DLL to align DQ and DQS transitions with CK
- Adjustable data-output drive strength
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC2-5300 spec. and JEDEC- Standard MO 224C. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR2 - SDRAM component base Micron MT47H64M16 Die Rev. H**
- 64Mx16 DDR2 SDRAM in FBGA-84 package
- V_{DD} = 1.8V ±0.1V, V_{DDQ} 1.8V ±0.1V
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- 1.8V I/O (SSTL_18 compatible)
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Four bit prefetch architecture
- On-die termination (ODT)

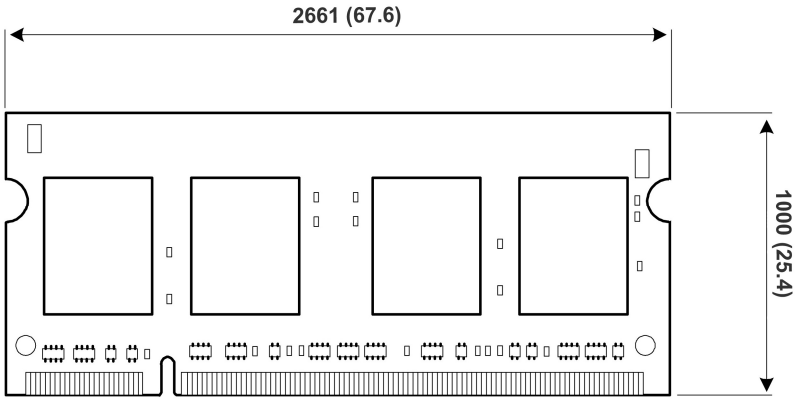


Figure: mechanical dimensions

This Swissbit module is an industry standard 200-pin 8-byte DDR2 SDRAM Small Outline Dual-In-line Memory Module (SO-DIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured oct-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.
The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-DIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Col. Addr.	Refresh	Module Bank Select
128M x 64bit	8 x 64M x 16bit (1Gbit)	13	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
67.60 (long) x 25.4(high) x 3.80 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SEN01G64E1CH2MT-30R	1024 MB	5.3 GB/s	3.0ns/667MT/s	5300-555

Pin Name

A0-9, A11 – A12	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 –BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable

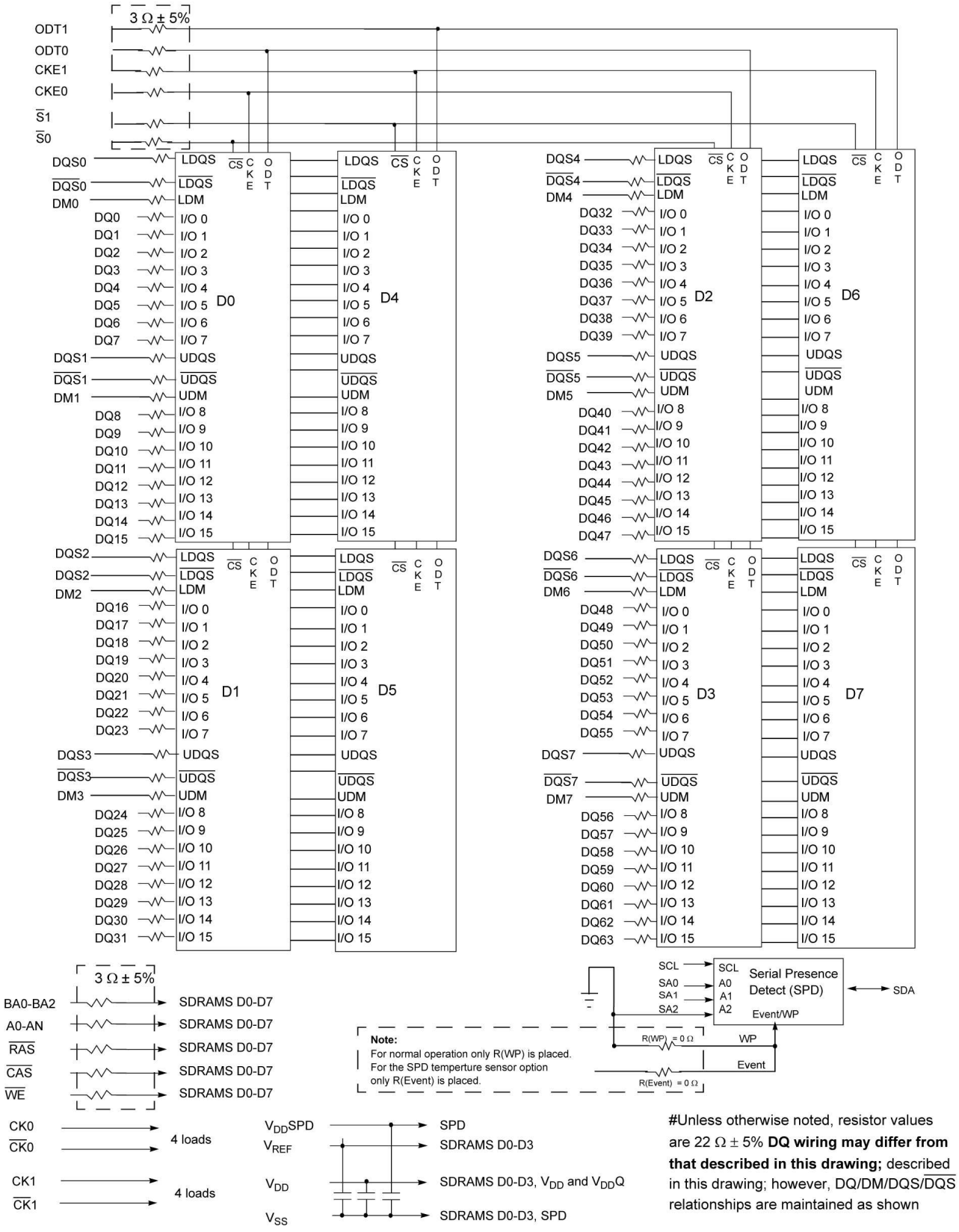
CK0 – CK1	Clock Inputs, positive line
CK0# – CK1#	Clock Inputs, negative line
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0#, S1#	Chip Select
V_{DD}	Supply Voltage (1.8V± 0.1V)
V_{REF}	Input / Output Reference
V_{SS}	Ground
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	2	VSS	101	A1	102	A0
3	VSS	4	DQ4	103	VDD	104	VDD
5	DQ0	6	DQ5	105	A10/AP	106	BA1
7	DQ1	8	VSS	107	BA0	108	RAS#
9	VSS	10	DM0	109	WE#	110	S0#
11	DQS0#	12	VSS	111	VDD	112	VDD
13	DQS0	14	DQ6	113	CAS#	114	ODT0
15	VSS	16	DQ7	115	S1#	116	NC/A13
17	DQ2	18	VSS	117	VDD	118	VDD
19	DQ3	20	DQ12	119	ODT1	120	NC
21	VSS	22	DQ13	121	VSS	122	VSS
23	DQ8	24	VSS	123	DQ32	124	DQ36
25	DQ9	26	DM1	125	DQ33	126	DQ37
27	VSS	28	VSS	127	VSS	128	VSS
29	DQS1#	30	CK0	129	DQS4#	130	DM4
31	DQS1	32	CK0#	131	DQS4	132	VSS
33	VSS	34	VSS	133	VSS	134	DQ38
35	DQ10	36	DQ14	135	DQ34	136	DQ39
37	DQ11	38	DQ15	137	DQ35	138	VSS
39	VSS	40	VSS	139	VSS	140	DQ44
41	VSS	42	VSS	141	DQ40	142	DQ45
43	DQ16	44	DQ20	143	DQ41	144	VSS
45	DQ17	46	DQ21	145	VSS	146	DQS5#
47	VSS	48	VSS	147	DM5	148	DQS5
49	DQS2#	50	NC	149	VSS	150	VSS
51	DQS2	52	DM2	151	DQ42	152	DQ46

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	Vss	54	Vss	153	DQ43	154	DQ47
55	DQ18	56	DQ22	155	Vss	156	Vss
57	DQ19	58	DQ23	157	DQ48	158	DQ52
59	Vss	60	Vss	159	DQ49	160	DQ53
61	DQ24	62	DQ28	161	Vss	162	Vss
63	DQ25	64	DQ29	163	NC	164	CK1
65	Vss	66	Vss	165	Vss	166	CK1#
67	DM3	68	DQS3#	167	DQS6#	168	Vss
69	NC	70	DQS3	169	DQS6	170	DM6
71	Vss	72	Vss	171	Vss	172	Vss
73	DQ26	74	DQ30	173	DQ50	174	DQ54
75	DQ27	76	DQ31	175	DQ51	176	DQ55
77	Vss	78	Vss	177	Vss	178	Vss
79	CKE0	80	CKE1	179	DQ56	180	DQ60
81	VDD	82	VDD	181	DQ57	182	DQ61
83	NC	84	NC	183	Vss	184	Vss
85	NC/BA2	86	NC	185	DM7	186	DQS7#
87	VDD	88	VDD	187	Vss	188	DQS7
89	A12	90	A11	189	DQ58	190	Vss
91	A9	92	A7	191	DQ59	192	DQ62
93	A8	94	A6	193	Vss	194	DQ63
95	VDD	96	VDD	195	SDA	196	Vss
97	A5	98	A4	197	SCL	198	SA0
99	A3	100	A2	199	VDDSPD	200	SA1

FUNCTIONAL BLOCK DIAGRAMM 1024MB DDR2 SDRAM SoDIMM, 2 RANKS AND 8 COMPONENTS



#Unless otherwise noted, resistor values are 22 Ω ± 5% **DQ wiring may differ from that described in this drawing;** described in this drawing; however, DQ/DM/DQS/$\overline{\text{DQS}}$ relationships are maintained as shown

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	-1.0	2.3	V
I/O Supply Voltage		$V_{DD}Q$	-0.5	2.3	V
$V_{DD}L$ Supply Voltage		$V_{DD}L$	-0.5	2.3	V
Voltage on any pin relative to V_{SS}		V_{in}, V_{out}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)		I_I			µA
	Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
	CK, CK#		-20	20	
	DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-5	5	µA
	DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level		I_{VREF}	-16	16	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DD}Q$	1.7	1.8	1.9	V
$V_{DD}L$ Supply Voltage	$V_{DD}L$	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51x $V_{DD}Q$	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.125		$V_{DD}Q$ + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.125	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.25	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.25	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition		Symbol	max. 5300-555	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DDO}	568	mA
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	548	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2P}	56	mA
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	520	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	560	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast PDN Exit MR[12] = 0	I_{DD3P}	240	mA
	Slow PDN Exit MR[12] = 1		80	
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	600	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	908	mA

Parameter & Test Condition	Symbol	max. 5300-555	Unit
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	828	mA
BURST REFRESH CURRENT: t_{CK} = t_{CK} (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	2160	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	56	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); t_{CK} = t_{CK} (I_{DD}), t_{RC} = t_{RC} (I_{DD}), t_{RRD} = t_{RRD} (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	1428	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS		
SYMBOL	**5300-555**	**Unit**
CL (I_{DD})	5	t_{CK}
t_{RCD} (I_{DD})	15	ns
t_{RC} (I_{DD})	60	ns
t_{RRD} (I_{DD})	7.5	ns
t_{CK} (I_{DD})	3.0	ns
t_{RAS} MIN (I_{DD})	45	ns
t_{RAS} MAX (I_{DD})	70,000	ns
t_{RP} (I_{DD})	15	ns
t_{RFC} (I_{DD})	105	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS			5300-555		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Unit**
Clock cycle time	CL = 5	t_{CK} (5)	3.0	8.0	ns
	CL = 4	t_{CK} (4)	3.75	8.0	ns
	CL = 3	t_{CK} (3)	5.0	8.0	ns
CK high-level width		t_{CH}	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.45	0.55	t_{CK}
Half clock period		t_{HP}	min (t_{CH}, t_{CL})		ps
Access window (output) of DQ_S from CK/CK#		t_{AC}	-0.45	+0.45	ns
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.45 (= t_{AC} max)	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.45 (= t_{AC} min)	+0.45 (= t_{AC} max)	ns
DQ and DM input setup time relative to DQS		t_{DSa}	0.10		ns
DQ and DM input hold time relative to DQS		t_{DHa}	0.30		ns
DQ and DM input setup time relative to DQS		t_{DSb}	0.10		ns
DQ and DM input hold time relative to DQS		t_{DHb}	0.175		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		t_{CK}
Data hold skew factor		t_{QHS}		0.34	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		ns
Data valid output window		t_{DVW}	t_{QH} - t_{DQSQ}		ns
DQS input high pulse width		t_{DQSH}	0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		t_{CK}
DQS output access time from CK/CK#		t_{DQSCK}	-0.40	+0.40	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.24	ns
DQS read preamble		t_{RPRE}	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	t_{CK}
DQS write preamble		t_{WPRE}	0.35		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		ns
DQS write postamble		t_{WPST}	0.4	0.6	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	t_{CK}
Write command to first DQS latching transition			WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	0.6		t_{CK}
Address and control input setup time		t_{ISa}	0.4		ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		5300-555		
PARAMETER	SYMBOL	MIN	MAX	Unit
Address and control input hold time	t_{IHa}	0.4		ns
Address and control input setup time	t_{ISb}	0.20		ns
Address and control input hold time	t_{IHb}	0.275		ns
CAS# to CAS# command delay	t_{CCD}	2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	55		ns
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		ns
Four bank Activate period	t_{FAW}	37.5		ns
ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		ns
Write recovery time	t_{WR}	15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		ns
PRECHARGE command period	t_{RP}	15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$		ns
LOAD MODE command cycle time	t_{MRD}	2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	105	70,000	ns
Average periodic refresh interval (0℃<= T_{CASE} <= 85 ℃)	t_{REFI}		7.8	µs
(85℃<= T_{CASE} <= 95 ℃)	t_{REFI}		3.9	µs
Exit SELF REFRESH to non-READ command	t_{XSNR}	t_{RFC}(min) + 10		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		ps
ODT turn-on delay	t_{AOND}	2	2	t_{CK}
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1,000	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 600	ps
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT to power-down entry latency	t_{ANPD}	3		t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		5300-555		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**Unit**
ODT power-down exit latency	t_{AXPD}	8		t_{CK}
ODT enable from MRS command	T_{MOD}	12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2		t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	7 – AL		t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2		t_{CK}
CKE minimum high/low time	t_{CKE}	3		t_{CK}

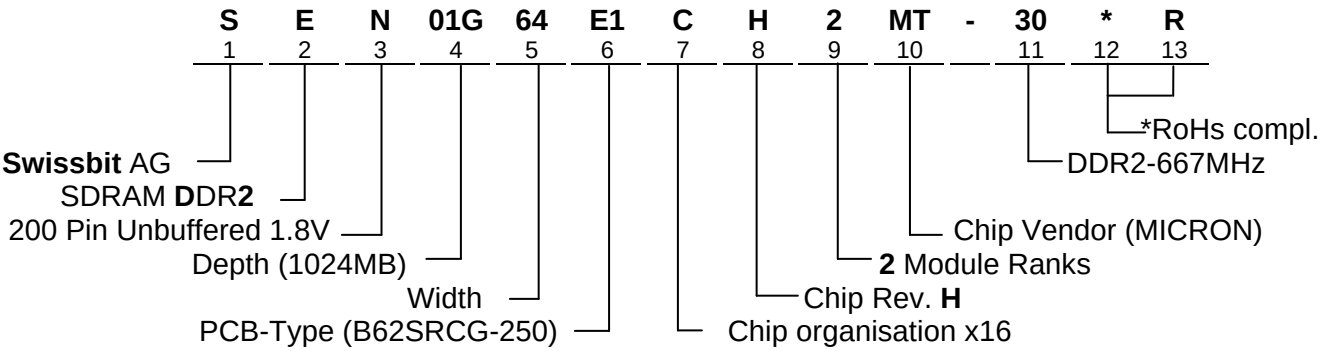
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	5300-555
0	NUMBER OF SPD BYTES USED	0x80
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08
2	FUNDAMENTAL MEMORY TYPE	0x08
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0D
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A
5	DIMM HIGHT AND MODULE RANKS	0x21
6	MODULE DATA WIDTH	0x40
7	MODULE DATA WIDTH (continued)	0x00
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	0x05
9	SDRAM CYCLE TIME, (t_{CK}) [max CL] CAS LATENCY = 5 (5300), CL = 4 (4200)	0x30
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL] CAS LATENCY = 5 (5300); CL = 4 (4200)	0x45
11	MODULE CONFIGURATION TYPE	0x00
12	REFRESH RATE / TYPE	0x82
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x10
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00
16	BURST LENGTHS SUPPORTED	0x0C
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08
18	CAS LATENCIES SUPPORTED	0x38
19	MODULE THICKNESS	0x01
20	DDR2 DIMM TYPE	0x04
21	SDRAM MODULE ATTRIBUTES	0x00
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x3D
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x45
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2] CAS LATENCY = 3 (5300)	0x50
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2] CAS LATENCY = 3 (5300)	0x45
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x28
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D
31	MODULE BANK DENSITY	0x80

SERIAL PRESENCE-DTECT MATRIX (continued)

BYTE	DESCRIPTION	5300-555
32	ADDRESS AND COMMAND SETUP TIME, (t_{ISb})	0x20
33	ADDRESS AND COMMAND HOLD TIME, (t_{IHb})	0x27
34	DATA / DATA MASK INPUT SETUP TIME, (t_{DSb})	0x10
35	DATA / DATA MASK INPUT HOLD TIME, (t_{DHb})	0x17
36	WRITE RECOVERY TIME, (t_{WR})	0x3C
37	WRITE to READ Command Delay, (t_{WTR})	0x1E
38	READ to PRECHARGE Command Delay, (t_{RTP})	0x1E
39	Mem Analysis Probe	0x00
40	Extension for Bytes 41 and 42	0x06
41	MIN ACTIVE AUTO REFRESH TIME, (t_{RC})	0x3C
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x7F
43	SDRAM DEVICE MAX CYCLE TIME, (t_{CKMAX})	0x80
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t_{DQSQ})	0x18
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t_{QHS})	0x22
46	PLL Relock Time	0x00
47-61	Optional Features, not supported	0x00
62	SPD REVISION	0x13
63	CHECKSUM FOR BYTES 0-62	0x40
64-67	MANUFACTURER`S JEDEC ID CODE	0x7F7F7FDA
68-71	MANUFACTURER`S JEDEC ID CODE (continued)	0x00
72	MANUFACTURING LOCATION	x
73-90	MODULE PART NUMBER (ASCII)	“SEN01G64E1CH2MT-30R”
91	PCB IDENTIFICATION CODE	0x52
92	IDENTIFICATION CODE (continued)	0x00
93	YEAR OF MANUFACTURE IN BCD	x
94	WEEK OF MANUFACTURE IN BCD	x
95-98	MODULE SERIAL NUMBER	x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00
128-255	Open for customer use	0xff

Part Number Code



* optional / additional information

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