DS1181L

20MHz to 134MHz Spread-Spectrum Clock Modulator for LCD Panels

General Description

The DS1181L is a spread-spectrum clock modulator IC that reduces EMI in high clock-frequency-based, digital electronic equipment.

Using an integrated phase-locked loop (PLL), the DS1181L accepts an input clock signal in the range of 20MHz to 134MHz and delivers a spread-spectrum modulated output clock signal. The PLL modulates, or dithers, the output clock about the center input frequency at a pin-selectable magnitude, allowing direct EMI control and optimization. In addition, through an enable pin the dithering can be enabled or disabled for easy comparison of system performance during EMI testing. This same input pin also allows the DS1181L output to be three-stated.

By dithering the system clock, all the address, data, and timing signals generated from this signal are also dithered so that the measured EMI at the fundamental and harmonic frequencies is greatly reduced. This is accomplished without changing clock rise/fall times or adding the space, weight, design time, and cost associated with mechanical shielding.

The DS1181L is provided in an 8-pin TSSOP package and operates over a full automotive temperature range of -40°C to +125°C.

Applications

- LCD Panels for TVs, Desktop Monitors, and Notebook and Tablet PCs
- Printers

Features

- Modulates a 20MHz to 134MHz Clock with Center Spread-Spectrum Dithering
- Selectable Spread-Spectrum Modulation Magnitudes of:
  - ±0.5%
  - ±1.0%
  - ±1.5%
  - ±2.0%
- Low 75ps Cycle-to-Cycle Jitter
- Spread-Spectrum Disable Mode
- Pin Compatible with Alliance/PulseCore Semiconductor P2040 Series Devices
- Clock Output Disable
- Low Cost
- Low Power Consumption
- 3.3V Single Voltage Supply
- -40°C to +125°C Temperature Range
- Small 8-Pin TSSOP Package

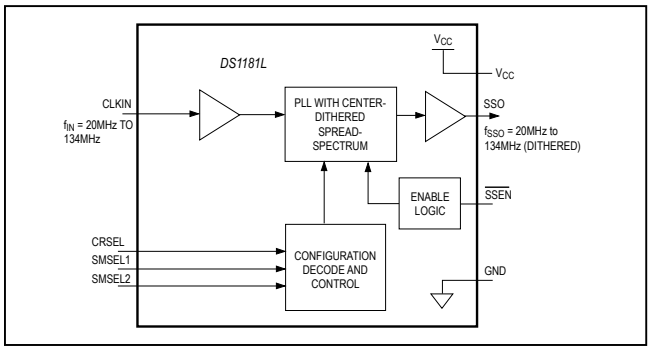
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1181LE+	-40°C to +125°C	8 TSSOP
DS1181LE+T	-40°C to +125°C	8 TSSOP

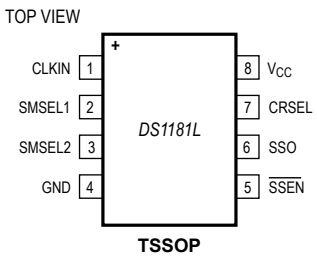
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

Block Diagram



Pin Configuration



19-7502; Rev 2; 2/15

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Absolute Maximum Ratings

Voltage Range on V_{CC} Relative to GND .....-0.5V to +4.3V
Voltage Range on Any Lead Relative to GND.....-0.5V to (V_{CC} + 0.5V), not to exceed +4.3V
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature .....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	3.0		3.6	V
Input Logic 1	V_{IH}		0.8 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		0.2 x V_{CC}	V
Input Logic Float ($\overline{SSEN}$, CRSEL)	I_{FLOAT}	0V < V_{IN} < V_{CC}			±1	µA
SSO Load	C_L	SSO < 80MHz			15	pF
		80MHz ≤ SSO < 134MHz			7	
CLKIN Frequency	f_{IN}		20		134	MHz
CLKIN Duty Cycle	f_{INDC}		40		60	%

DC Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	C_L = 7pF, f_{IN} = 134MHz			18	mA
SMSEL1/SMSEL2/CLKIN Input Leakage	$I_{IL:1}$	0V < V_{IN} < V_{CC}	-1		+1	µA
CRSEL/$\overline{SSEN}$ Input Leakage	$I_{IL:2}$	0V < V_{IN} < V_{CC}	-100		+100	µA
Output Leakage (SSO)	I_{OZ}	$\overline{SSEN}$ = float	-1		+1	µA
Low-Level Output Voltage (SSO)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage (SSO)	V_{OH}	I_{OH} = -4mA	2.4			V

AC Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSO Duty Cycle	f_{SSODC}	Measured at V_{CC}/2	40		60	%
SSO Rise Time	t_R	C_L = 7pF		1		ns
SSO Fall Time	t_F	C_L = 7pF		1		ns
Peak Cycle-to-Cycle Jitter	t_J	T_A = -40°C to +85°C, 10,000 cycles		75		ps
Power-Up Time	t_{POR}	(Note 2)			50	ms

Note 1: All voltages referenced to ground. Currents into the IC are positive and out of the IC are negative.
Note 2: Time between power applied to device and stable output.

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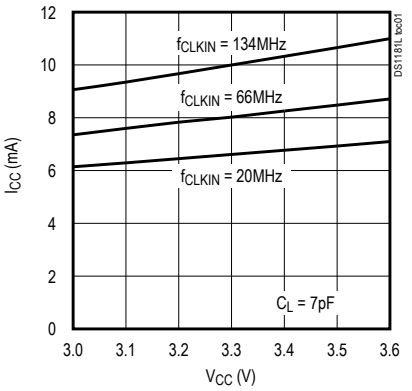
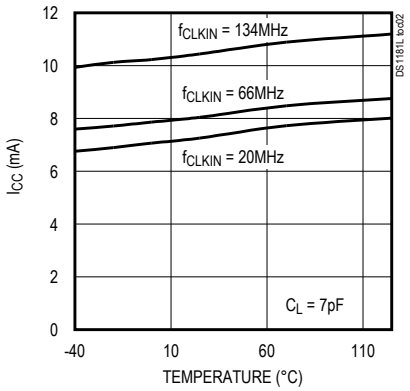
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

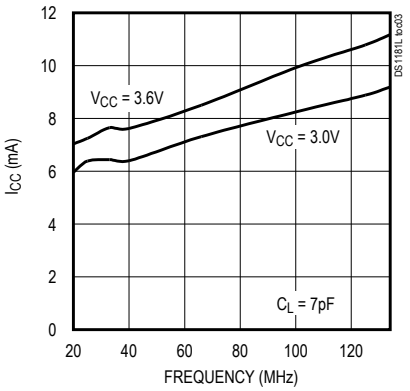
SUPPLY CURRENT vs. SUPPLY VOLTAGE



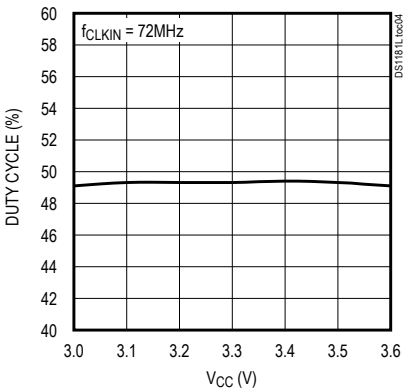
SUPPLY CURRENT vs. TEMPERATURE



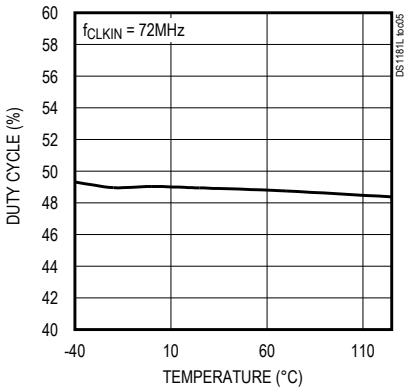
SUPPLY CURRENT vs. FREQUENCY



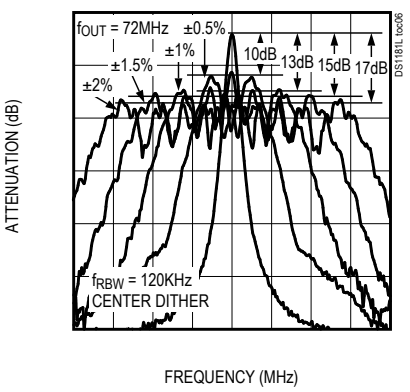
DUTY CYCLE vs. SUPPLY VOLTAGE



DUTY CYCLE vs. TEMPERATURE



SPECTRUM ATTENUATION vs. FREQUENCY AT DIFFERENT DITHER AMPLITUDES



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Pin Description

PIN	NAME	FUNCTION		
1	CLKIN	Clock Input. 20MHz to 134MHz clock input (f_{IN}).		
2	SMSEL1	Spread-Spectrum Magnitude Select Inputs. These digital inputs select the desired spread-spectrum magnitude as shown in the table below.		
		SMSEL2	**SMSEL1**	**MAGNITUDE SELECTED (%)**
		0	0	±2.0
3	SMSEL2	0	1	±1.5
		1	0	±1.0
		1	1	±0.5
4	GND	Ground		
5	$\overline{SSEN}$	Spread-Spectrum Enable. Three-level input to enable/disable spread-spectrum and to three-state the output. 0 = Power-up/spread-spectrum enabled Float = SSO three-stated 1 = Power-up/spread-spectrum disabled (not a bypass mode).		
6	SSO	Spread-Spectrum Clock Output. Outputs a center-dithered spread-spectrum version of the clock input at CLKIN.		
7	CRSEL	Clock Range and Dither Rate Select. Three-level input that determines the dither rate. See the *Detailed Description* section for details.		
		CRSEL	**CLKIN RANGE (MHz)**	**DITHER RATE**
		0	66 to 134	$f_{IN}/832$
		Float	33 to 80	
		1	20 to 38	
8	V_{CC}	Supply Voltage		

Detailed Description

The DS1181L modulates an input clock to generate a center-dithered spread-spectrum output. A 20MHz to 134MHz clock is applied to the CLKIN pin. An internal PLL dithers the output clock about its center frequency at a user-selectable magnitude.

Spread-Spectrum Dither Magnitude

The DS1181L can generate dither magnitudes up to ±2%. The desired magnitude is selected using input pins SMSEL1 and SMSEL2 as shown in Table 1.

Table 1. Dither Magnitude

SMSEL2	SMSEL1	MAGNITUDE SELECTED (%)
0	0	±2.0
0	1	±1.5
1	0	±1.0
1	1	±0.5

Spread-Spectrum Dither Rate

The output spread-spectrum dither rate is fixed at $f_{IN}/832$.

Table 2. Dither Rate

CRSEL	CLKIN RANGE (MHz)	DITHER RATE
0	66 to 134	$f_{IN}/832$
Float	33 to 80	
1	20 to 38	

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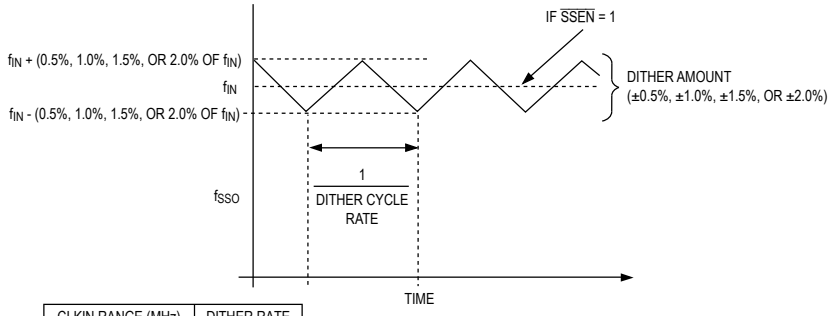
Spread-Spectrum Enable

On power-up, the output clock (SSO) remains three-stated until the internal PLL reaches a stable frequency. The $\overline{SSEN}$ input can be used to disable the spread-spectrum modulation and to three-state the SSO output. If the $\overline{SSEN}$ pin is pulled high, the spread-spectrum modulation is turned off, but the device still uses the internal PLL to generate the clock signal at SSO. If the $\overline{SSEN}$ pin is floated, the output is three-stated.

Applications Information

Power-Supply Decoupling

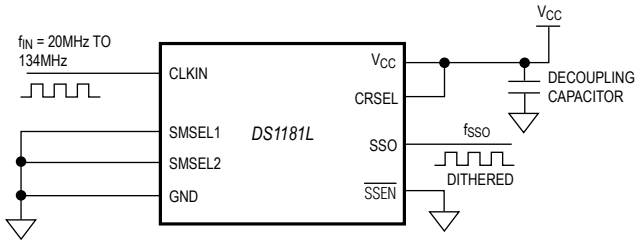
To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power-supply pins. Typical values of decoupling capacitors are 0.01µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.



CLKIN RANGE (MHz)	DITHER RATE
20 TO 134	$f_{IN}/832$

Figure 1. DS1181L Spread-Spectrum Frequency Modulation

Typical Operating Circuit



NOTE: IN THE ABOVE CONFIGURATION WITH SMSEL1, SMSEL2, AND $\overline{SSEN}$ CONNECTED TO GND AS WELL AS CRSEL CONNECTED TO V_{CC}, THE DEVICE IS CONFIGURED WITH A SPREAD-SPECTRUM MAGNITUDE OF 2.0%, AND ALLOWS A CLKIN BETWEEN 20MHz and 38MHz.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
8 TSSOP	H8+3	21-0175	90-0248

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/07	Initial release.	—
1	8/08	Increased the absolute maximum ratings range from +3.63V to +4.3V.	2
2	2/15	Removed automotive reference from data sheet	1

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