DRV8847 Dual H-Bridge Motor Driver

ADVANCE INFORMATION

1 Features

- Dual H-Bridge Motor Driver
  - Single or Dual Brushed DC Motors
  - One Bipolar Stepper Motor
  - Solenoid Loads
- 2.7-V to 18-V Operating Voltage Range
- High Output Current per H-bridge
  - 1-A RMS Driver Current at T_A = 25°C
  - 2-A RMS Driver Current in Parallel Mode at T_A = 25°C
- Low On-State Resistance
  - 1000-mΩ $R_{DS(ON)}$ (HS + LS) at T_A = 25°C
- Simple Control Interface Options
  - 4-Pin Interface
  - 2-Pin Interface
  - Parallel Bridge Interface
  - Independent Bridge Interface
- Current Regulation With 20-μs Fixed Off Time
- Torque Scalar for Scaling Output Current to 50%
- Supports 1.8-V, 3.3-V, 5-V Logic Inputs
- Low-Power Sleep Mode
  - 3-μA Sleep Mode Supply Current
- I^2C Device Variant Available (DRV8847S)
  - Detailed Diagnostics on I^2C Registers
  - Multi-Slave Operation Support
  - Supports Standard and Fast I^2C Mode
- Small Packages and Footprints
  - 16 Pin TSSOP (No Thermal Pad)
  - 16 Pin HTSSOP PowerPAD™ Package
  - 16 Pin WQFN Thermal Package
- Built-In Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Open Load Detection (OLD)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Refrigerator Damper and Ice Maker
- Washers, Dryers and Dishwashers
- Electronic Point-of-Sale (ePOS) Printers
- Stage Lighting Equipment
- Miniature Circuit Breakers and Smart Meters

3 Description

The DRV8847 device is a dual H-bridge motor driver for industrial applications, home appliances, ePOS printers, and other mechatronic applications. This device can be used for driving two DC motors, a bipolar stepper motor, or other loads such as relays. A simple PWM interface allows easy interface with the controller. The DRV8847 device operates off a single power supply and supports a wide input supply range from 2.7 to 18 V.

The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges to drive motor windings or four independent half bridges (in independent bridge interface). A fixed off time controls the peak current in the bridge which can drive a 1-A load (2-A in parallel mode with proper heat sinking, at 25°C T_A).

A low-power sleep mode is provided to achieve a low quiescent current draw by shutting down much of the internal circuitry. Additionally, a torque scalar is provided which dynamically scales the output current through a digital input pin. This feature lets the controller decrease the current required for lower power consumption.
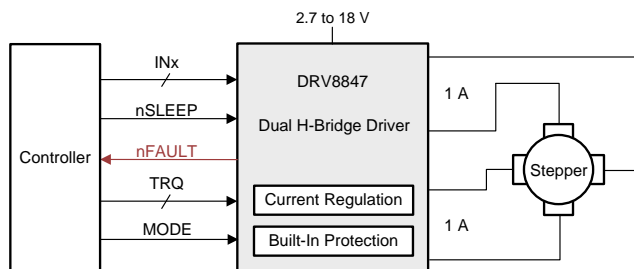
Internal protection functions are provided for undervoltage-lockout, overcurrent protection on each FET, short circuit protection, open-load detection, and overtemperature. Fault conditions are indicated by on the nFAULT pin. The I^2C device variant (DRV8847S) has detailed diagnostics.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8847	HTSSOP (16)	5.00 mm × 6.40 mm
	TSSOP (16)	5.00 mm × 6.40 mm
	WQFN (16)	3.00 mm × 3.00 mm
DRV8847S	TSSOP (16)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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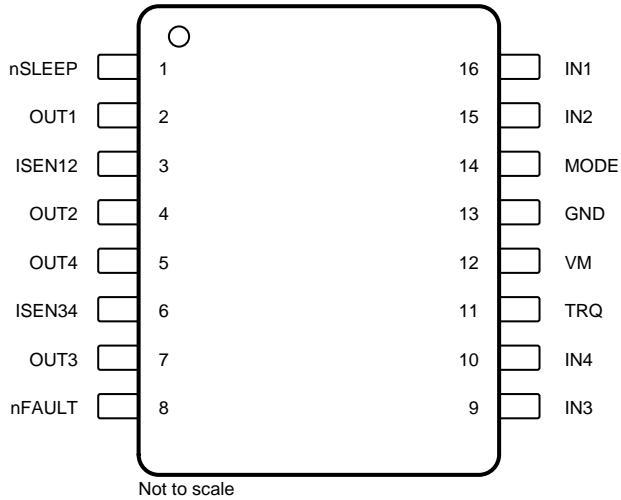
4 Revision History

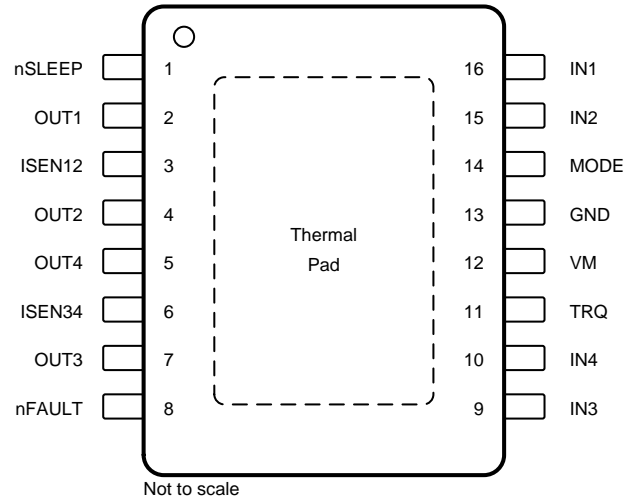NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2018	*	Initial release.

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5 Pin Configuration and Functions

DRV8847 PW Package
16-Pin TSSOP
Top View

	Pin		Pin	
nSLEEP	1		16	IN1
OUT1	2		15	IN2
ISEN12	3		14	MODE
OUT2	4		13	GND
OUT4	5		12	VM
ISEN34	6		11	TRQ
OUT3	7		10	IN4
nFAULT	8		9	IN3

Not to scale

DRV8847 PWP PowerPAD™ Package
16-Pin HTSSOP
Top View

	Pin		Pin	
nSLEEP	1		16	IN1
OUT1	2		15	IN2
ISEN12	3		14	MODE
OUT2	4	Thermal Pad	13	GND
OUT4	5		12	VM
ISEN34	6		11	TRQ
OUT3	7		10	IN4
nFAULT	8		9	IN3

Not to scale

DRV8847 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View

		OUT1	nSLEEP	IN1	IN2	
		16	15	14	13	
ISEN12	1				12	MODE
OUT2	2	Thermal Pad			11	GND
OUT4	3				10	VM
ISEN34	4				9	TRQ
		5	6	7	8	
		OUT3	nFAULT	IN3	IN4	

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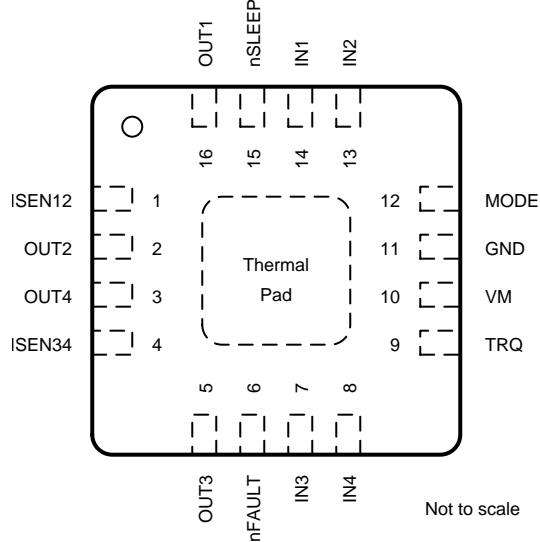
DRV8847S PW Package
16-Pin TSSOP
Top View

	Pin		Pin	
nSLEEP	1		16	IN1
OUT1	2		15	IN2
ISEN12	3		14	SDA
OUT2	4		13	GND
OUT4	5		12	VM
ISEN34	6		11	SCL
OUT3	7		10	IN4
nFAULT	8		9	IN3

Not to scale

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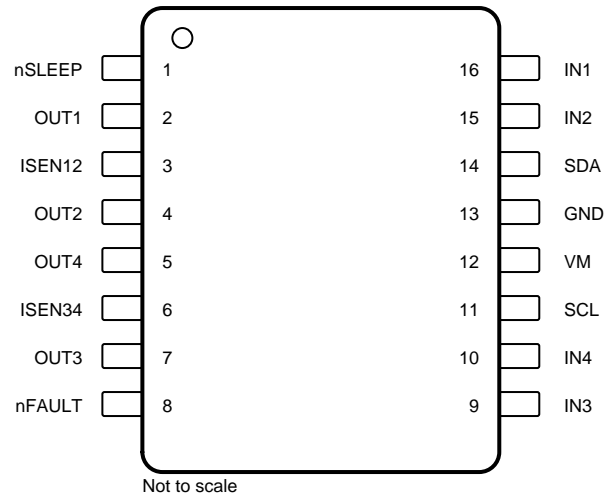
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Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	DRV8847		DRV8847S		
	TSSOP HTSSOP	WQFN	TSSOP		
GND	13	11	13	PWR	Device ground. Both the GND pin and device thermal pad (HTSSOP and WQFN packages) must be connected to ground
IN1	16	14	16	I	Half-bridge input 1
IN2	15	13	15	I	Half-bridge input 2
IN3	9	7	9	I	Half-bridge input 3
IN4	10	8	10	I	Half-bridge input 4
ISEN12	3	1	3	O	Full-bridge-12 sense. Connect this pin to the current sense resistor for full-bridge-12. Connect this pin to the GND pin if current regulation is not required.
ISEN34	6	4	6	O	Full-bridge-34 sense. Connect this pin to the to current sense resistor for full-bridge-34. Connect this pin to the GND pin if current regulation is not required.
MODE	14	12	—	I	Tri-state pin for selection of driver operating mode
nFAULT	8	6	8	OD	Fault indication pin. This pin is pulled logic low with a fault condition. This open-drain output requires an external pullup resistor.
nSLEEP	1	15	1	I	Sleep mode input. Set this pin to logic high to enable the device. Set this pin to logic low to go to low-power sleep mode
OUT1	2	16	2	O	Half-bridge output 1
OUT2	4	2	4	O	Half-bridge output 2
OUT3	7	5	7	O	Half-bridge output 3
OUT4	5	3	5	O	Half-bridge output 4
SCL	—	—	11	I	I^2C clock signal.
SDA	—	—	14	OD	I^2C data signal. The SDA pin requires a pullup resistor.
TRQ	11	9	—	I	Torque current scalar
VM	12	10	12	PWR	Power supply. Connect the VM pin to the motor power supply. Bypass this pin to ground with a VM-rated 0.1-µF and 10-µF (minimum) ceramic capacitor.

(1)   I = input, O = output, OD = open-drain output, PWR = power

Product Folder Links: *DRV8847*

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Power supply pin voltage (VM)	-0.3	20	V
Power supply voltage ramp rate (VM)	0	2	V/μs
Digital pin voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, nFAULT, SCL, SDA)	-0.3	5.5	V
Continuous phase node pin voltage (OUT1, OUT2, OUT3, OUT4)	-0.7	VM + 0.6	V
Continuous shunt amplifier input pin voltage (ISEN12, ISEN34)	-0.6	0.6	V
Peak drive current (OUT1, OUT2, OUT3, OUT4)	Internally Limited		A
Ambient temperature, T_A	-40	125	°C
Junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage (VM)	2.7		18[1]	V
V_{IN}	Logic input voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, SCL, SDA)	0		5	V
I_{RMS}	Motor RMS current per bridge (OUT1, OUT2, OUT3, OUT4)	0		1[2]	A
f_{PWM}	PWM frequency (IN1, IN2, IN3, IN4)	0		250[2]	kHz
V_{OD}	Open drain pullup voltage (nFAULT)	0		5	V
I_{OD}	Open drain output current (nFAULT)	0		5	mA
T_A	Operating Ambient Temperature	-40[3]		85	°C
T_J	Operating Junction Temperature	-40		150	°C

(1) **Errata:** The current silicon is functional from 2.7-V to 15-V
(2) Power dissipation and thermal limits must be observed
(3) **Errata:** The current silicon is functional from 0°C to 85°C (Ambient Temperature)

6.4 Thermal Information

THERMAL METRIC[1]		DRV8847, DRV8847S PW (TSSOP) 16 PINS	DRV8847 PWP (HTSSOP) 16 PINS	DRV8847 RTE (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	46.5	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.5	40.1	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	18.8	21.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.1	1.3	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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Thermal Information (continued)

THERMAL METRIC[(1)]		DRV8847, DRV8847S	DRV8847	DRV8847	UNIT
		PW (TSSOP)	PWP (HTSSOP)	RTE (QFN)	
		16 PINS	16 PINS	16 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	53.6	19.0	21.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5.9	6.1	°C/W

6.5 Electrical Characteristics

V_{VM} = 2.7 to 18 V over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
V_{VM}	VM operating voltage		2.7		18	V
I_{VM}	VM operating supply current	VM = 2.7 V; nSLEEP = 1; INX = 0		2	2.5	mA
		VM = 5 V; nSLEEP = 1; INX = 0		3	3.5	mA
		VM = 12 V; nSLEEP = 1; INX = 0		3	3.5	mA
I_{VMQ}	VM sleep mode current	VM = 2.7 V; nSLEEP = 0; TA = 25°C		0.5		µA
		VM = 2.7 V; nSLEEP = 0; TA = 85°C			1	µA
		VM = 5 V; nSLEEP = 0; TA = 25°C		1		µA
		VM = 5 V; nSLEEP = 0; TA = 85°C			1.5	µA
		VM = 12 V; nSLEEP = 0; TA = 25°C		3		µA
		VM = 12 V; nSLEEP = 0; TA = 85°C			3.5	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode		2		µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition			1.5	ms
t_{ON}	Turnon-time	VM > UVLO to output transition (nSLEEP = 1)			1.5	ms
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, NSLEEP, TRQ, SCL, SDA)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis	nSLEEP pin	40			mV
V_{HYS}	Input logic hysteresis	IN1, IN2, IN3, IN4, TRQ, SCL pins	100			mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	µA
I_{IH}	Input logic high current	IN1, IN2, IN3, IN4, TRQ, V_{IN} = 5 V	1		35	µA
		nSLEEP, V_{IN} = 5 V	1		25	µA
t_{PD}	Propagation Delay	INx edge to output	100	400	600	ns
TRI-LEVEL INPUTS (MODE)						
V_{IL}	Tri-level input logic low voltage		0		0.6	V
V_{IZ}	Tri-level input hi-Z voltage			1.2		V
V_{IH}	Tri-level input logic high voltage		1.6		5.5	V
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	1		35	µA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		35	µA
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.5	V
I_{OH}	Output logic high current	V_{OD} = 3.3 V	-1		1	µA
OPEN-DRAIN OUTPUTS (SDA)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.5	V
I_{OH}	Output logic high current	V_{OD} = 3.3 V	-1		1	µA
C_B	Capacitive load for each bus line				400	pF
DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						

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Product Folder Links: *DRV8847*

Electrical Characteristics (continued)

V_{VM} = 2.7 to 18 V over operating ambient temperature range (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)\_HS}$	High-side MOSFET on resistance	V_{VM} = 2.7 V; I_{OUT} = 0.5 A; T_A = 25°C		690	800	mΩ
		V_{VM} = 2.7 V; I_{OUT} = 0.5 A; T_A = 85°C			950	mΩ
		V_{VM} = 5 V; I_{OUT} = 0.5 A; T_A = 25°C		530	620	mΩ
		V_{VM} = 5 V; I_{OUT} = 0.5 A; T_A = 85°C			740	mΩ
		V_{VM} = 12 V; I_{OUT} = 0.5 A; T_A = 25°C		520	600	mΩ
		V_{VM} = 12 V; I_{OUT} = 0.5 A; T_A = 85°C			700	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance	V_{VM} = 2.7 V; I_{OUT} = 0.5 A; T_A = 25°C		570	670	mΩ
		V_{VM} = 2.7 V; I_{OUT} = 0.5 A; T_A = 85°C			900	mΩ
		V_{VM} = 5 V; I_{OUT} = 0.5 A; T_A = 25°C		460	520	mΩ
		V_{VM} = 5 V; I_{OUT} = 0.5 A; T_A = 85°C			690	mΩ
		V_{VM} = 12 V; I_{OUT} = 0.5 A; T_A = 25°C		450	520	mΩ
		V_{VM} = 12 V; I_{OUT} = 0.5 A; T_A = 85°C			680	mΩ
I_{OFF}	Off-state leakage current	V_{VM} = 5 V; T_J = 25 °C; V_{OUT} = 0 V	-1		1	µA
t_{RISE}	Output rise time	V_{VM} = 12 V; I_{OUT} = 0.5 A		150		ns
t_{FALL}	Output fall time	V_{VM} = 12 V, I_{OUT} = 0.5 A		150		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
V_{SD}	Body diode forward voltage	I_{OUT} = 0.5 A		1.1		V
PWM CURRENT CONTROL (ISEN12, SEN34)						
V_{TRIP}	ISENxx trip voltage	Torque at 100% (TRQ = 0)	135	150	165	mV
		Torque at 50% (TRQ = 1)	63.75	75	86.25	mV
t_{BLANK}	Current sense blanking time			1.8		µs
t_{OFF}	Current control constant off time			20		µs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout	Supply rising			2.7	V
		Supply falling	2.4			V
V_{UVLO_HYS}	Supply undervoltage hysteresis	Rising to falling theshold		50		mV
t_{UVLO}	Supply undervoltage deglitch time	VM falling; UVLO report		10		µs
I_{OCP}	Overcurrent protection trip point			2		A
t_{OCP}	Overcurrent protection deglitch time	V_{VM} = 12 V		3		µs
t_{RETRY}	Overcurrent protection retry time			1		ms
I_{OL}	Open load pull up and pull down current	< 15 nF on OUTx Pin		200		µA
V_{OL}	Open load detect threshold voltage			1		V
T_{TSD}	Thermal shutdown temperature		150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

6.6 I2C Timing Requirements

		MIN	NOM	MAX	UNIT
STANDARD MODE					
f_{SCL}	SCL Clock frequency	0		100	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU,STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0		3.45	µs
$t_{SU,DAT}$	Data set-up time	250			ns

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I2C Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
t_R	SDA and SCL rise time			1000	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST MODE					
f_{SCL}	SCL Clock frequency	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0		0.9	µs
$t_{SU,DAT}$	Data set-up time	250			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{SP}	Pulse width of spikes to be supressed by input noise filter		50		ns

Figure 1. Timing Diagram

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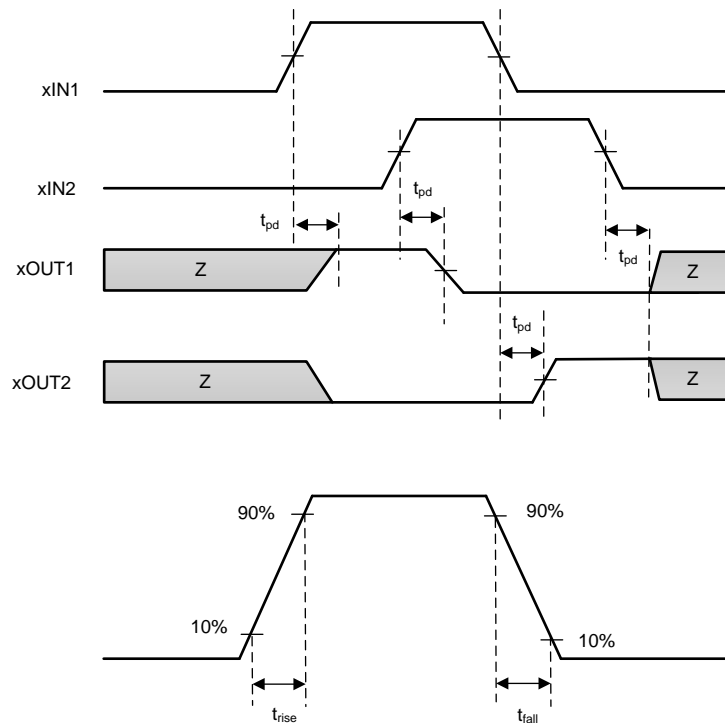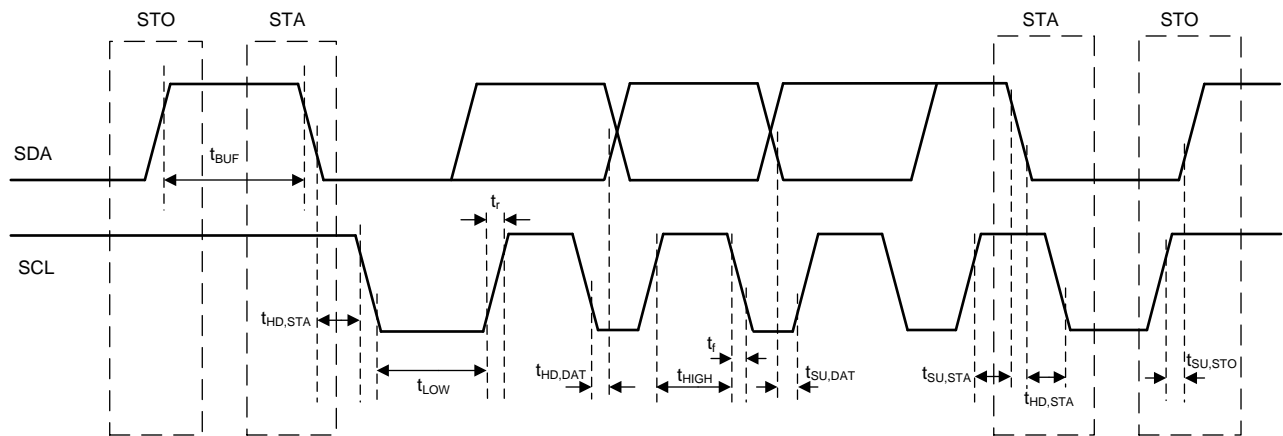
Figure 2. I²C Timing Diagram

7 Detailed Description

7.1 Overview

The DRV8847 device is an integrated 2.7- to 18-V dual motor driver for industrial brushed and stepper motor applications. This driver can drive two DC motors, a bipolar stepper motor, or the solenoid loads. The device integrates two H-bridges that use NMOS low-side and high-side drivers and current-sense regulation circuitry. The DRV8847 device supports a high output current of 1-A RMS per H-bridge using low-$R_{DS(ON)}$ integrated MOSFETs.

A simple PWM interface option allows easy interfacing to the H-bridge outputs. The interface options can be configured using the MODE and IN3 pins in the DRV8847 device. The interface options can be configured through a I^{2}C interface in the I^{2}C device variant (DRV8847S).

The current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The trip point for current regulation is controlled by the value of the sense resistor and fixed internal V_{TRIP} value.

A low-power sleep mode is included which lets the system save power when not driving the motor.

The DRV8847 device is available in three different packages:
- 16-pin TSSOP (no thermal pad)
- 16 pin HTSSOP (PowerPAD)
- 16 pin WQFN (thermal pad)

The I^{2}C variant of the DRV447 device is also available for a detailed diagnostics requirement and multi-slave operation with multi-slave operation control over I^{2}C bus.

The DRV8847S device variant is available in one package which is the 16-pin TSSOP (no thermal pad).

The DRV8847 device has a broad range of integrated protection features. These features include power-supply undervoltage lockout, open-load detection, overcurrent faults, and thermal shutdown.

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Product Folder Links: *DRV8847*

7.2 Functional Block Diagram
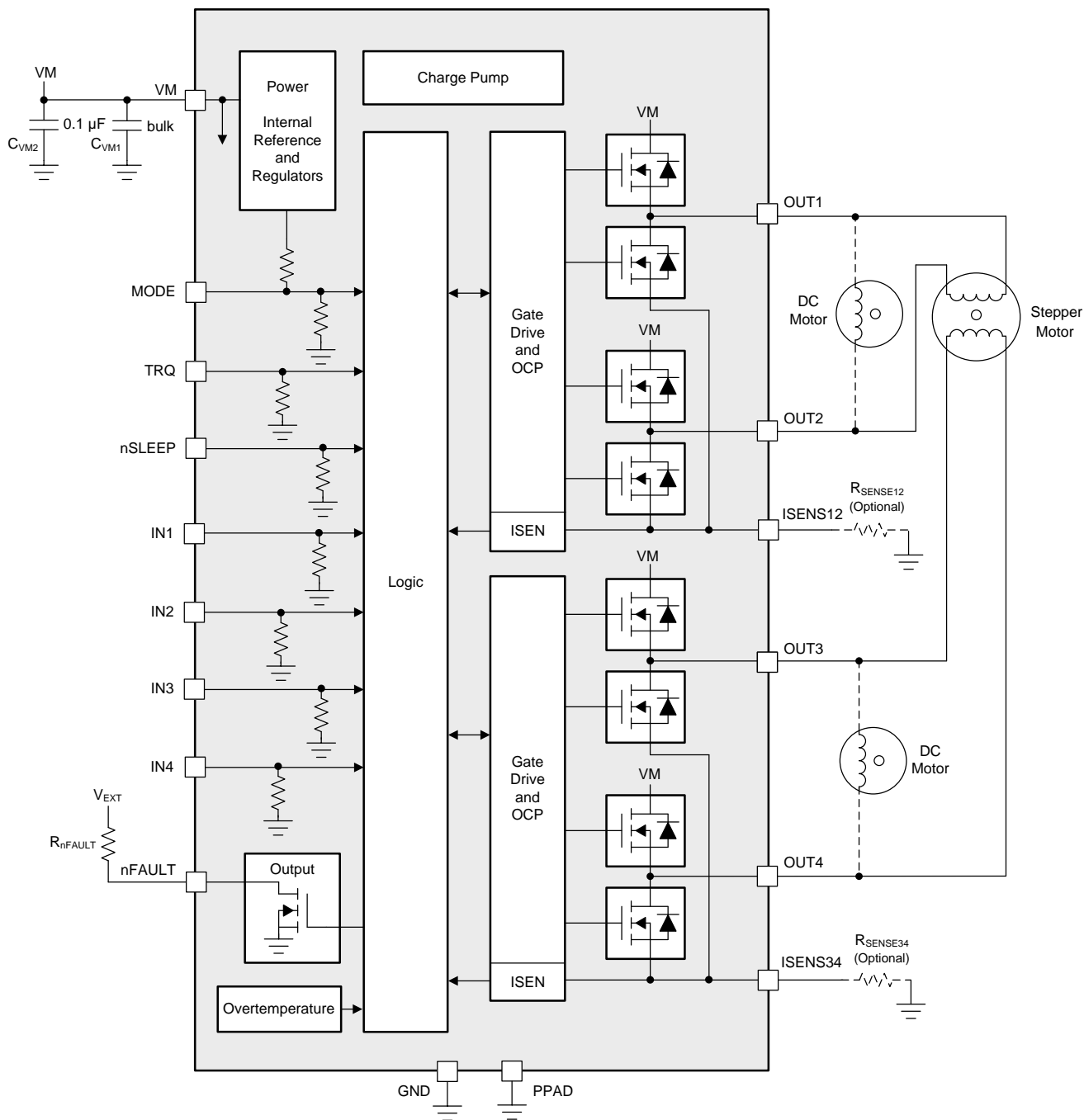
Figure 3. Block Diagram for DRV8847

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Functional Block Diagram (continued)

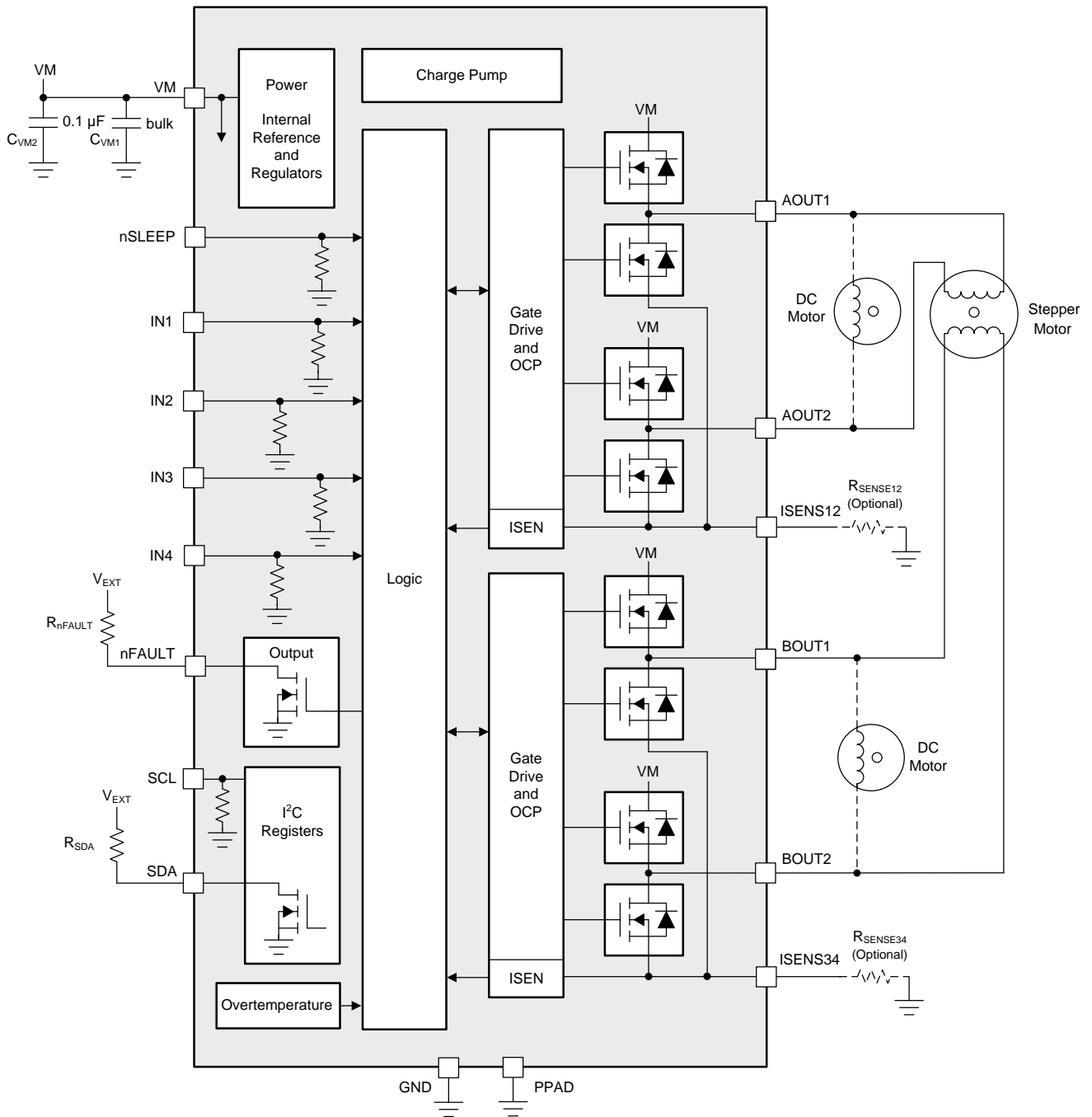**Figure 4. Block Diagram for DRV8847S**

Product Folder Links: *DRV8847*

7.3 Feature Description

Table 1 lists the recommended values of the external components for the gate driver.

Table 1. DRV8847 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	10-µF (minimum) VM-rated ceramic capacitor
C_{VM2}	VM	GND	0.1-µF VM-rated ceramic capacitor
R_{nFAULT}	VEXT[1]	nFAULT	>1 kΩ
R_{ISEN12}	ISEN12	GND	Sense resistor, see the *Typical Application* for sizing
R_{ISEN34}	ISEN34	GND	Sense resistor, see the *Typical Application* for sizing

(1) VEXT is not a pin on the DRV8847 device, but a pullup resistor on the VEXT external supply voltage is required for the open-drain output, nFAULT.

7.3.1 PWM Motor Drivers

The DRV8847 device has two identical H-bridge motor drivers with current-control PWM circuitry. Figure 5 shows a block diagram of the circuitry.

The two H-bridges can also be used as four independent half-bridges depending upon the interface option. The ISENxx pin can be only used together with two half-bridges.
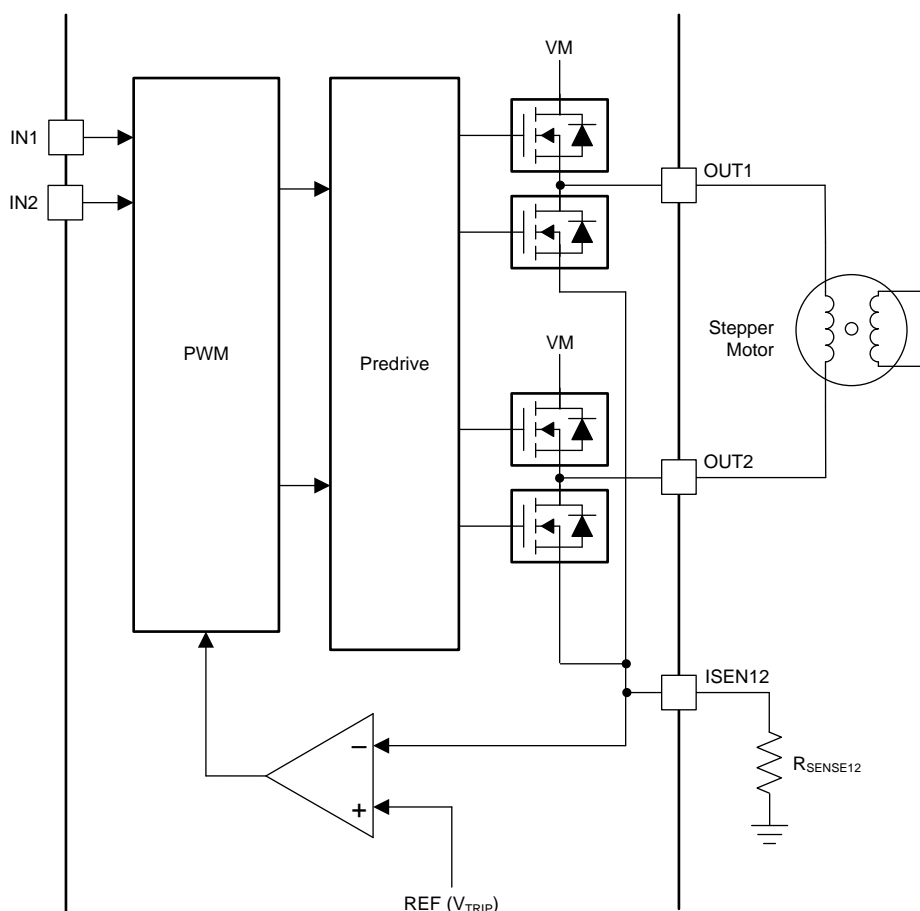
Figure 5. PWM Motor Driver Circuitry

7.3.2 Bridge Operation

The full-bridge can operate in four different operating modes: forward, reverse, coast (fast decay), and brake (slow decay) operation.

7.3.2.1 Forward Operation

This operating mode refers to the forward rotation of the motor such that the current flows from terminal A (OUT1 or OUT3) to terminal B (OUT2 or OUT4) as shown in Figure 6. In this mode, terminal A is connected to VM and terminal B is connected to ground.
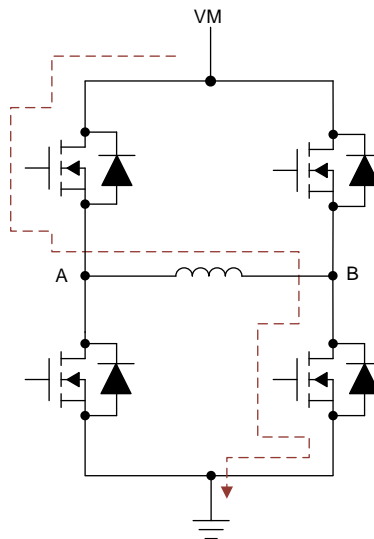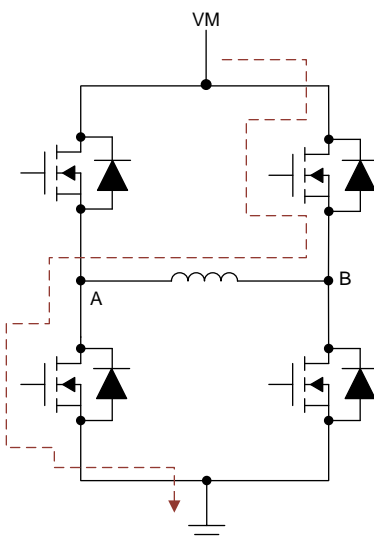

Figure 6. Forward Operation

7.3.2.2 Reverse Operation

This operating mode refers to the reverse rotation of the motor such that the current flows from terminal B (OUT2 or OUT4) to terminal A (OUT1 or OUT3) as shown in Figure 7. In this mode, terminal A is connected to ground and terminal B is connected to VM.

Figure 7. Reverse Operation

<div style="writing-mode: vertical-rl">ADVANCE INFORMATION</div>

7.3.2.3 Coast Operation (Fast Decay)

In this operating mode, all the FETs of the full-bridges are in the high impedance (Hi-Z) state. The motor also goes to the Hi-Z state, and the motor starts coasting. This operating mode also helps to decay the motor current faster and is therefore also referred to as a fast decay mode. If the motor was initially connected in forward operation (current flows from terminal A to terminal B) and if the coast operation is applied, then, because of the inductive nature of motor load, the current continues to flow in the same direction (A to B), and the anti-parallel diodes of the alternate FETs starts conducting as shown in Figure 8. This flow of current through anti-parallel diodes lets the current decrease rapidly because of the higher negative potential created by the supply voltage, VM.
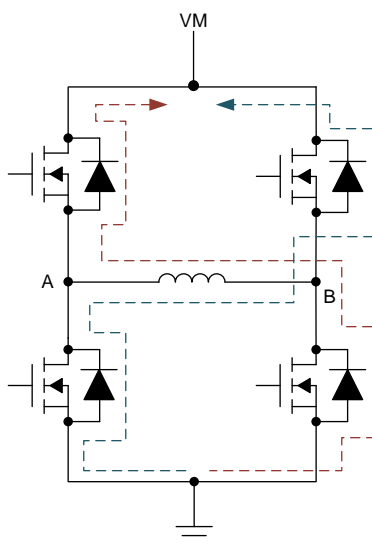
Figure 8. Coast Operation (Fast Decay)

7.3.2.4 Brake Operation (Slow Decay)

This operating mode is realized by switching on both of the low-side FETs of the full-bridge as shown in Figure 9. A current circulation path is provided when both low-side FETs are turned on. Due to this circulation path, the current decays to ground using the resistance of the motor and of the low-side FET. Because this current decay is less when compared to the coast operation because of the low potential difference, this mode is also referred to the slow decay mode.
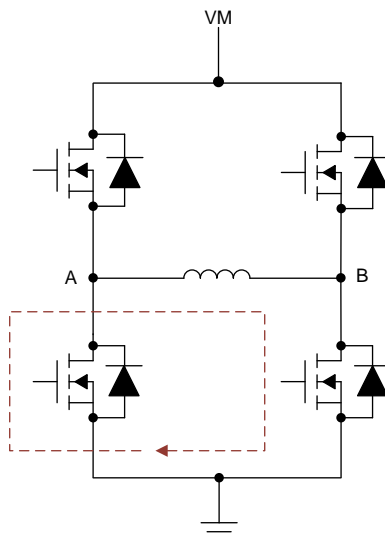
Figure 9. Brake Operation (Slow Decay)

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7.3.3 Bridge Control

The DRV8847 device can be configured in four different operating modes depending on user requirements. The MODE and IN3 pins are used to configure the DRV8847 in one of the four different interfaces: 4-pin interface, 2-pin interface, a parallel bridge interface, and the independent bridge interface. Mode selection is done using the I^{2}C registers in the DRV8847S device variant (see the *Programming* section). Table 2 lists the configurations to select the operating mode of the bridges.

Table 2. Bridge Mode Selection (DRV8847 Hardware Device Variant)

nSLEEP	MODE	IN3	INTERFACE
0	X	X	Sleep mode
1	0	X	4-pin interface
1	1	0	2-pin interface
1	1	1	Parallel bridge interface
1	Z	X	Independent bridge interface

NOTE

The MODE pin is not latched during driver operation. Therefore, TI does not recommend connecting this pin to a controller to use at any time.

7.3.3.1 4-Pin Interface

In the 4-pin interface, the DRV8847 device is configured to drive a stepper motor or two BDC motors with fully functional modes. To configure 4-pin interface operation, connect the MODE pin to ground and use the IN1, IN2, IN3, and IN4 pins to control the drivers. In this mode, the stepper or brushed DC motor can operate with all four modes (forward, reverse, coast, and brake mode) and the stepper motor can operate in either full-stepping mode or the non-circulating half-stepping mode. Sense resistors can be connected to the ISEN12 and ISEN34 pins for independent current regulation in bridge-12 and bridge-34 respectively.

Use this interface option for the following loads:

- Stepper motor in full-stepping mode (with or without current regulation)
- Stepper motor in half-stepping mode (with or without current regulation)
- Single or dual BDC motor (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)

Table 3 lists the configurations for 4-pin interface operation and Figure 10 shows the application diagram for 4-pin interface operation.

Table 3. 4-Pin Interface (MODE = 0)

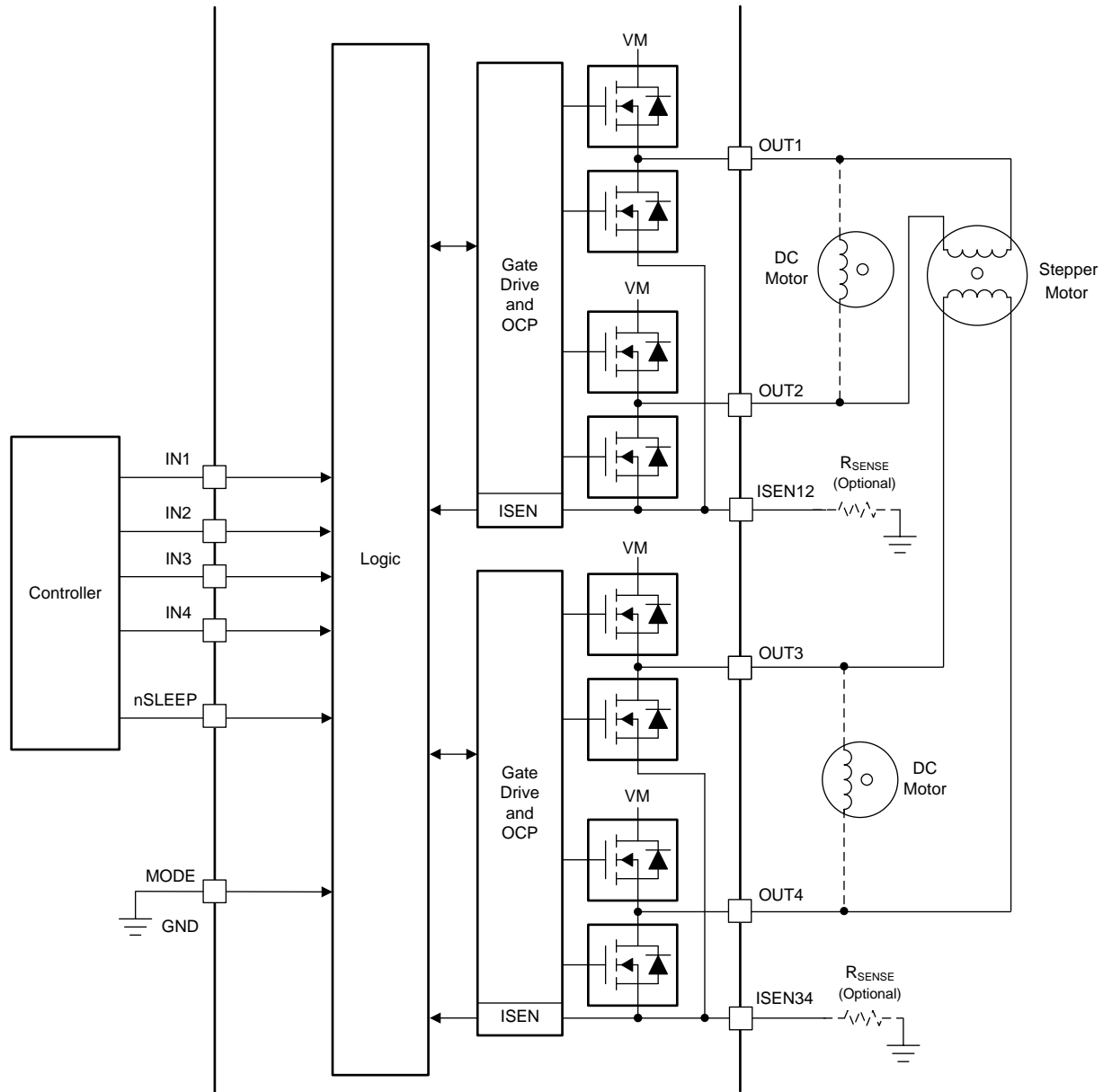| nSLEEP	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	FUNCTION (DC MOTOR)
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0	0			Z	Z			Motor coast (fast decay)
1	0	1			L	H			Reverse direction
1	1	0			H	L			Forward direction
1	1	1			L	L			Motor brake (slow decay)
1			0	0			Z	Z	Motor coast (fast decay)
1			0	1			L	H	Reverse direction
1			1	0			H	L	Forward direction
1			1	1			L	L	Motor brake (slow decay)

Figure 10. 4-Pin Interface Operation

7.3.3.2 2-Pin Interface

In the 2-pin interface, the DRV8847 device is configured to drive a stepper motor or two BDC motors with lower number of control inputs from micro-controller. To configure 2-pin interface operation, connect the MODE pin to the external supply (3.3 V or 5 V), connect the IN3 pin to ground, and use the IN1 and IN2 pins to control the driver. In this mode, the stepper or brushed DC motor operate in only two modes (forward mode and reverse mode) i.e. only full-step operation is supported for stepper motor. This 2-pin interface is very useful for low GPIO applications such as refrigerator dampers. Sense resistors can be connected to the ISEN12 and ISEN34 pins for current regulation.

Use this interface option for the following loads:

- Stepper motor in full stepping mode (with or without current regulation)
- Single or dual BDC motor (with or without current regulation) with reduced functional BDC modes (forward and reverse mode only)

Table 4 lists the configurations for 2-pin interface operation and Figure 11 shows the application diagram for 2-pin interface operation.

Table 4. 2-Pin Interface (MODE = 1, IN3 = 0)

| nSLEEP	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	FUNCTION (DC MOTOR)
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0		0	X	L	H			Reverse direction
1	1		0	X	H	L			Forward direction
1		0	0	X			L	H	Reverse direction
1		1	0	X			H	L	Forward direction
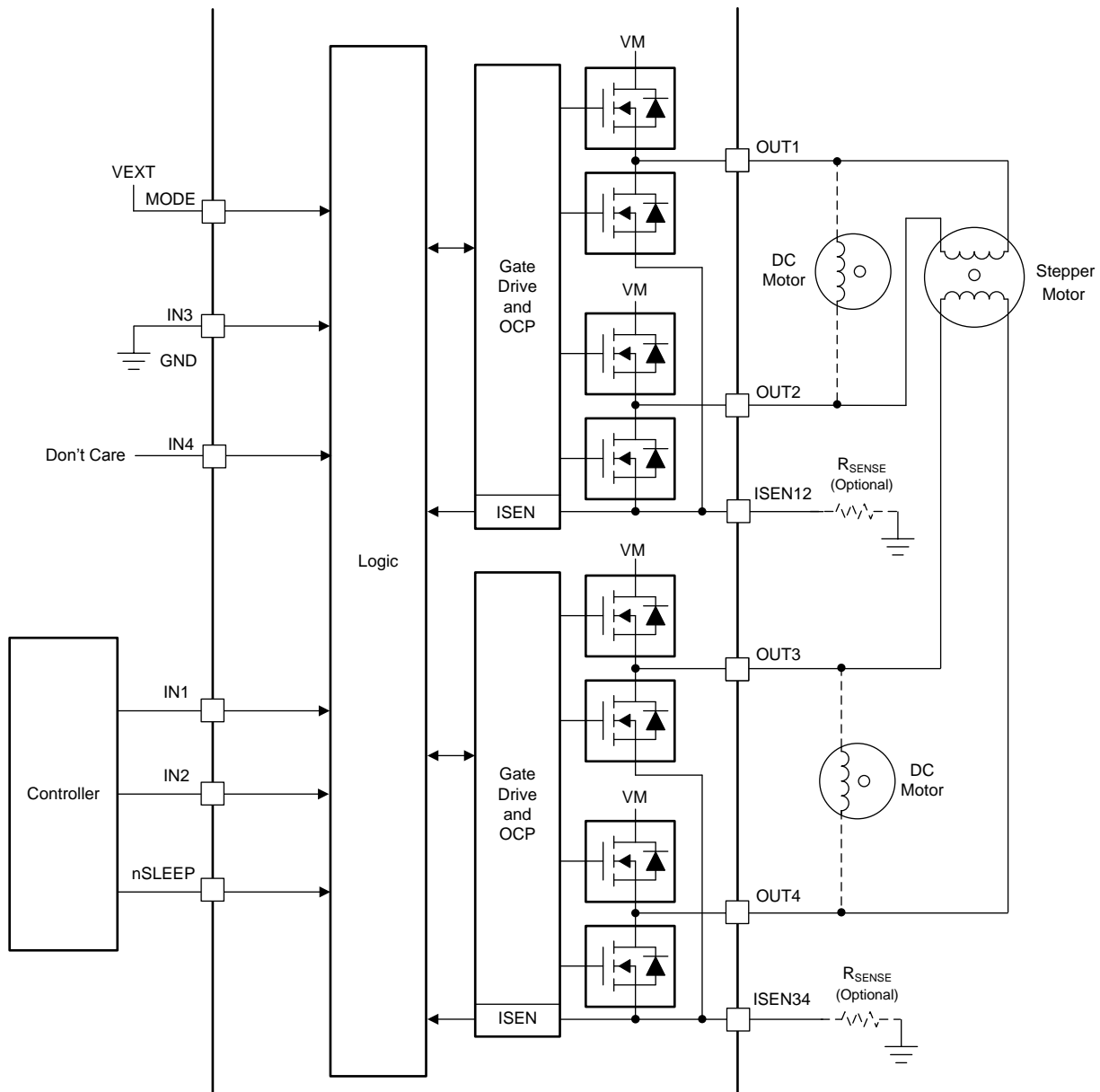
Figure 11. 2-Pin Interface Operation

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NOTE

In this mode, two of the OUTx pins are always 'ON' if the device is in non-sleep state (nSLEEP = HIGH). Therefore, to completely de-energize the motor-coils connected to OUTx pins, the user has to pull-down nSLEEP pin.

7.3.3.3 Parallel Bridge Interface

In the parallel bridge interface, the DRV8847 device is configured to drive a higher current BDC motor by using the driver in parallel to deliver twice the motor current. To go to parallel bridge interface operation, connect the MODE and IN3 pins to the external supply (3.3 V or 5 V) and use the IN1 and IN2 pins to control the driver. This mode can deliver the full functionality of the BDC motor control with all four modes (forward, reverse, coast, and brake mode).

Use this interface option for the following loads:

* One high current BDC motor (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)
* Two independent BDC motors operating together (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)

Table 5 lists the configurations for parallel bridge interface operation, and Figure 12 shows the application diagram for parallel bridge interface operation.

Table 5. Parallel Interface (MODE = 1, IN3 = 1)

nSLEEP	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	FUNCTION (DC MOTOR)
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0	0	1	X	Z	Z	Z	Z	Motor coast (fast decay)
1	0	1	1	X	L	H	L	H	Reverse direction
1	1	0	1	X	H	L	H	L	Forward direction
1	1	1	1	X	L	L	L	L	Motor brake (slow decay)

NOTE

Errata: Parallel bridge mode is not functional with the current regulation using RSENSE resistor and might see some over-currents on the OUTx nodes. This will be fixed in next silicon revision.

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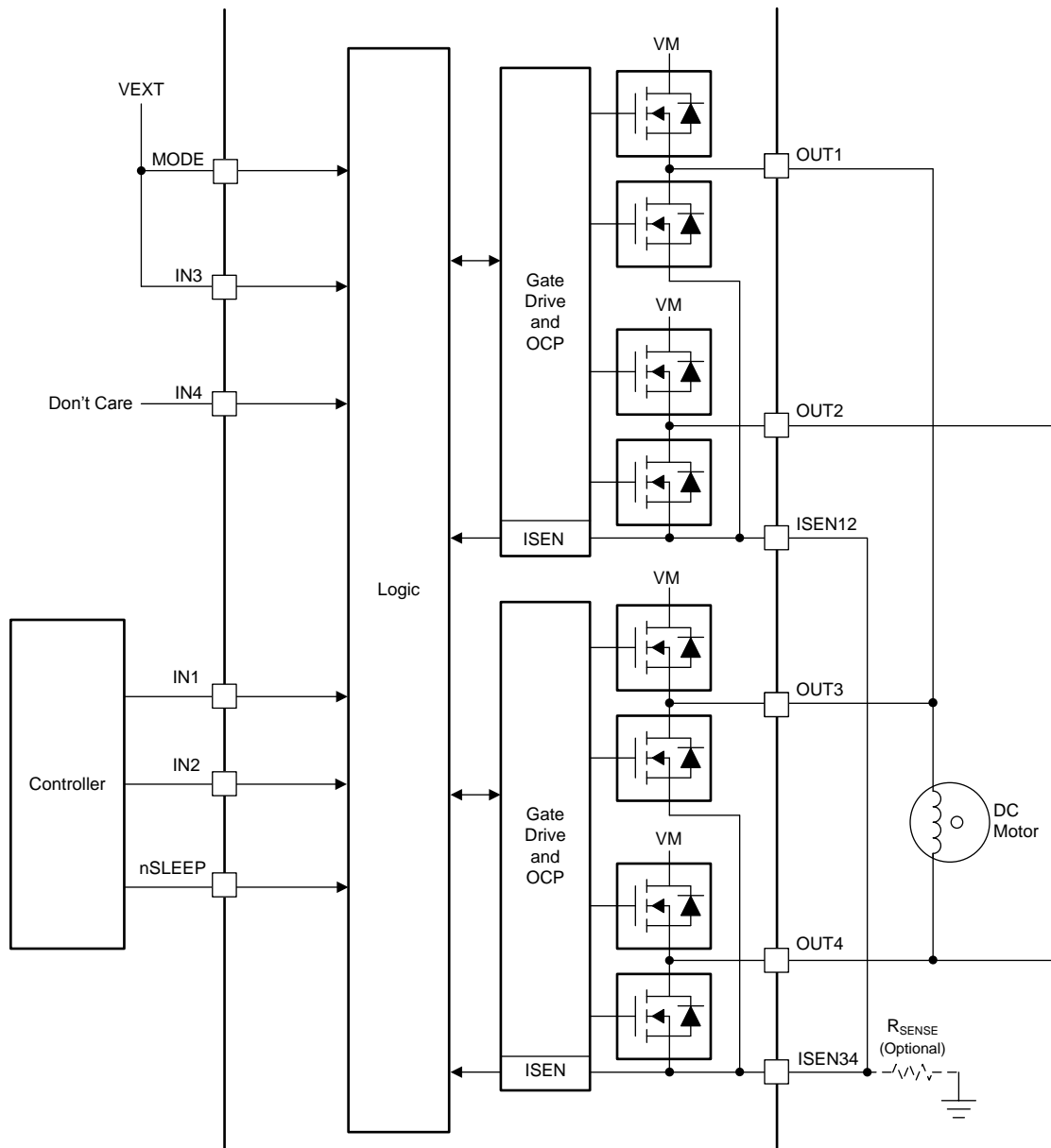
Figure 12. Parallel Mode Operation

7.3.3.4 *Independent Bridge Interface*

In the independent bridge interface, the DRV8847 device is configured for independent half-bridge operation. To configure independent bridge interface operation, leave the MODE pin unconnected (Hi-Z state) and use the IN1, IN2, IN3, and IN4 pins to independently control the OUT1, OUT2, OUT3, and OUT4 pins respectively. Only two output states of the OUTx pin can be controlled (either connected to VM or connected to GND). This mode is used to drive independent loads such as relays and solenoids.

Use this interface option for the following loads:
*   Relay or solenoid coils connected to the VM pin or ground
*   Single or dual BDC motor (with or without current regulation) with three functional BDC modes (forward, reverse, and braking mode only)
*   Stepper motor in full-stepping mode (with or without current regulation)
*   Stepper motor in half-stepping mode (with or without current regulation) using brake mode

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Table 6 lists the configurations for independent bridge interface operation and Figure 13 shows the application diagram for independent bridge interface operation.

Table 6. Independent Bridge Interface (MODE = Hi-Z)

nSLEEP	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	FUNCTION (DC MOTOR)
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0				L				OUT1 connected to GND
1	1				H				OUT1 connected to VM
1		0				L			OUT2 connected to GND
1		1				H			OUT2 connected to VM
1			0				L		OUT3 connected to GND
1			1				H		OUT3 connected to VM
1				0				L	OUT4 connected to GND
1				1				H	OUT4 connected to VM

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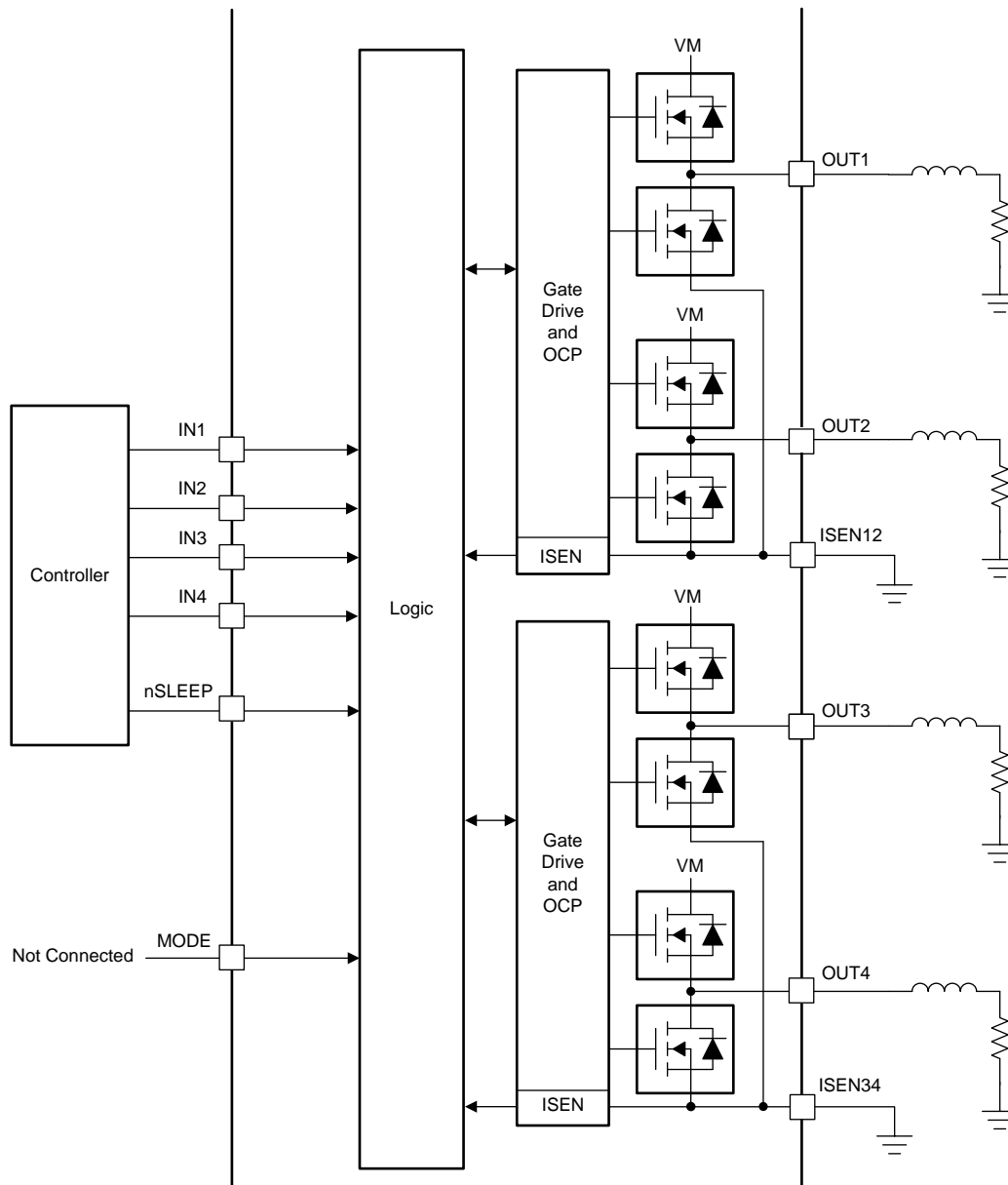
Figure 13. Independent Bridge Interface

7.3.4 Current Regulation

The current through the motor windings is regulated by a fixed off-time PWM current regulation circuit. With brushed DC motors, current regulation can be used to limit the stall current (which is also the start-up current) of the motor.

Current regulation works as follows: When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current trip threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle.

NOTE

Immediately after the current is enabled, the voltage on the ISENxx pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

The PWM trip current is set by a comparator which compares the voltage across a current sense resistor connected to the ISENxx pin with a reference voltage. This reference voltage (V_{TRIP}) is generated on-chip and decides the current trip level.

The full-scale trip current in a winding is calculated as shown in Equation 1.

$$I_{TRIP} = Torque \frac{V_{TRIP}}{R_{SENSExx}}$$

where

- I_{TRIP} is the regulated current.
- V_{TRIP} is the internally generated trip voltage.
- $R_{SENSExx}$ is the resistance of the sense resistor.
- Torque is the torque scalar, the value of which depends on the input on TRQ pin. TRQ = 100% for TRQ pin connected to GND (DRV8847) or TRQ bit set to 0 (DRV8847S) and TRQ = 50% connected to V_{EXT} (DRV8847) or TRQ bit set to 1 (DRV8847S).   (1)

For example, if the V_{TRIP} voltage is 150 mV and the value of the sense resistor is 150 mΩ, the full-scale trip current is 1 A (150 mV / (150 mΩ) = 1 A).

NOTE

If current control is not needed, connect the ISENxx pins directly to ground.

7.3.5 Current Recirculation and Decay Modes

During PWM current trip operation, the H-bridge is enabled to drive current through the motor winding until the trip threshold of the current regulation is reached. After the trip current threshold is reached, the drive current is interrupted, but, because of the inductive nature of the motor, current must continue to flow for some time. This continuous flow of current is called recirculation current. A mixed decay allows a better current regulation by optimizing the current ripple by using fast and slow decay.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the anti-parallel diodes of the opposite FETs are conducting on to let the current decay faster as shown in Figure 14 (see case 2). In slow decay mode, winding current is recirculated by enabling both low-side FETs in the bridge (see case 3 in Figure 14). Mixed decay starts with fast decay, then goes to slow decay. In the DRV8847 device, the mixed decay ratio is 25% fast decay and 75% slow decay as shown in Figure 15.
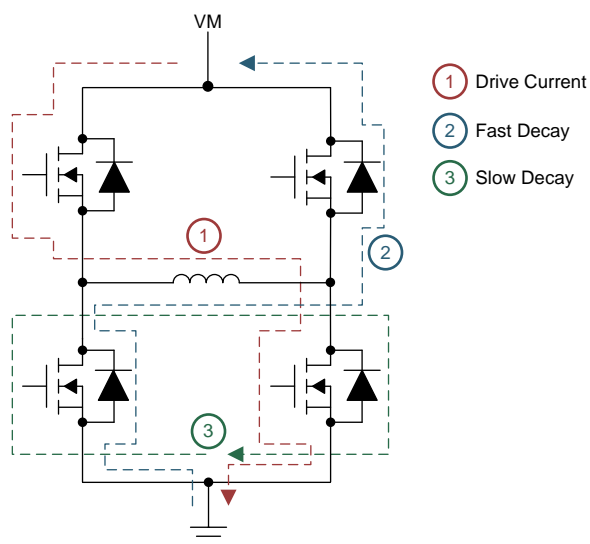
Figure 14. Decay Modes

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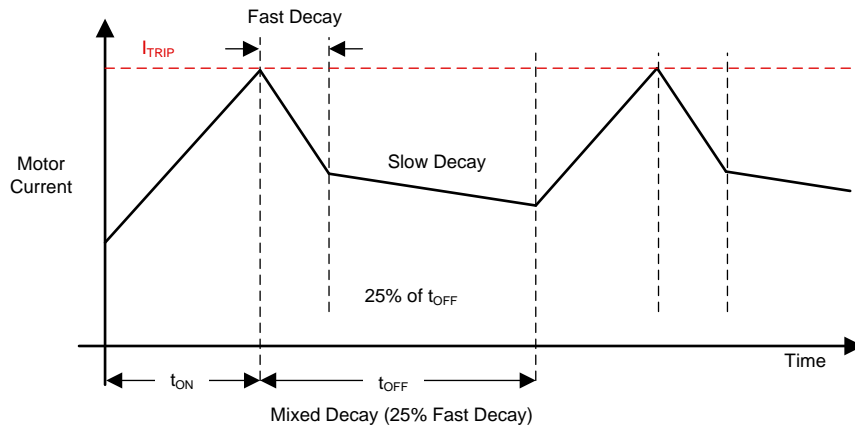
Figure 15. Mixed Decay

7.3.6 Torque Scalar

The torque scalar is used to dynamically adjust the output current through a digital input pin, TRQ. This torque scalar decreases the trip reference value of the output current to 50% (whenever the TRQ pin is pulled high). Torque scalar can be used to scale the holding torque of the stepper motor. For the I²C device variant (DRV8847S), this feature is implemented through an I²C register.

When the TRQ pin is pulled-low (or the TRQ bit is reset in the DRV8847S device variant), then trip current is calculated using Equation 2.

$$I_{TRIP} = \frac{Torque \times V_{TRIP}}{R_{SENSExx}}$$

(2)

When the TRQ pin is pulled-high (or the TRQ bit is set in the DRV8847S device variant), then trip current is calculated using Equation 3.

$$I_{TRIP} = 0.5\frac{V_{TRIP}}{R_{SENSExx}}$$

(3)

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7.3.7 Stepping Modes

The DRV8847 device is used to drive a stepper motor in full-stepping mode or non-circulating half-stepping mode using the following bridge configurations:

- Full-stepping mode (with or without current regulation)
  - Using 4-pin interface configuration
  - Using 2-pin interface configuration
- Half-stepping mode (with or without current regulation)
  - Using 4-pin interface configuration

7.3.7.1 *Full-Stepping Mode (4-Pin Interface)*

In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings.

In 4-pin interface, the PWM input is applied to the IN1, IN2, IN3, and IN4 pins as shown in Figure 16 and the driver operates only in forward (FRW) and reverse (REV) mode.
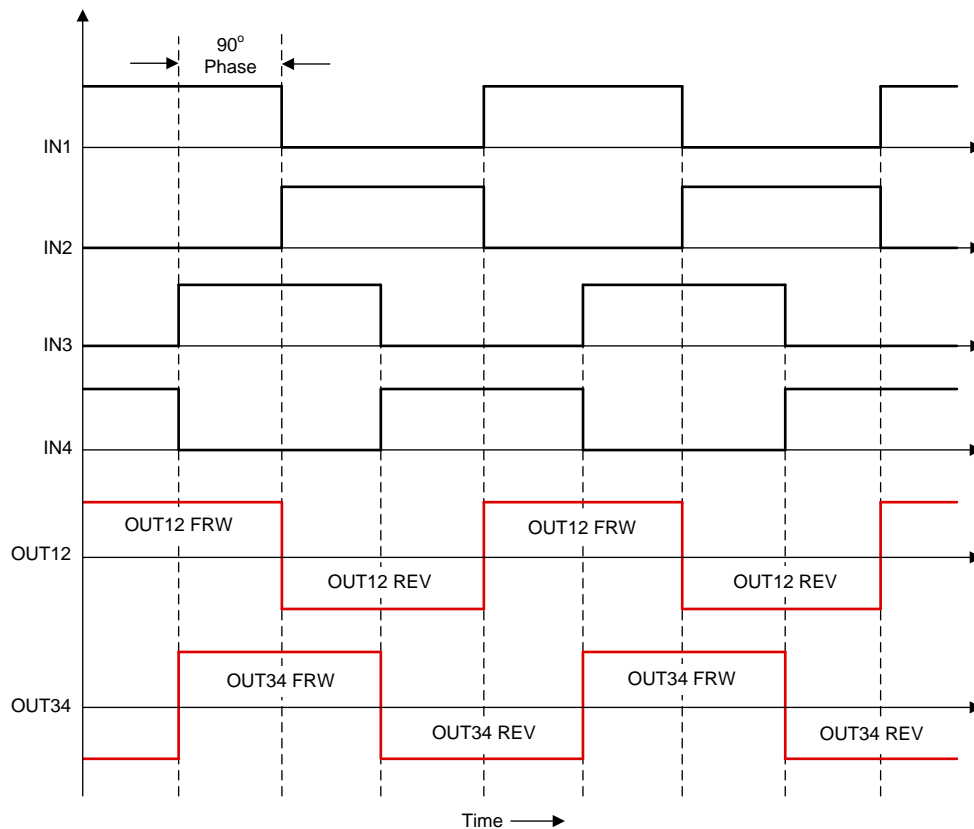
Figure 16. Full-Stepping Mode Using 4-Pin Interface

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7.3.7.2 *Full-Stepping Mode (2-Pin Interface)*

In full-stepping using the 2-pin interface, the PWM input is only applied to the IN1 and IN2 pins, and the IN3 is connected to ground (see the *Figure 11* section). Figure 17 shows the full-stepping mode of stepper motor using the 2-pin interface
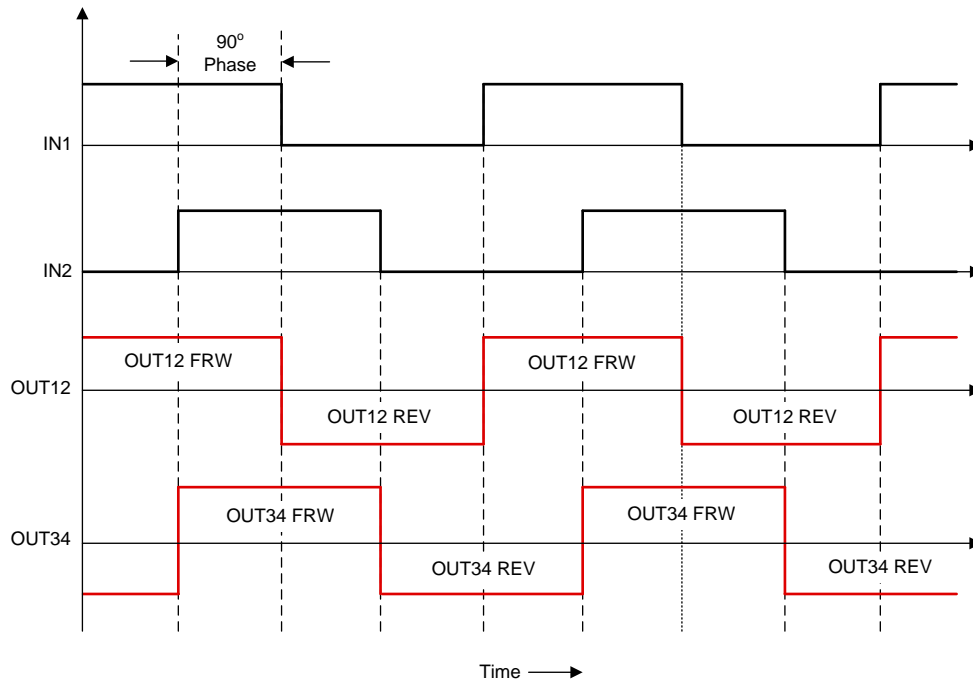
Figure 17. Full-Stepping Mode Using 2-Pin Interface

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7.3.7.3 Half-Stepping Mode

In half-stepping mode, the full-bridge operates in one of the three modes (forward, reverse, or coast mode) with a phase shift of 45° between the two windings.

In 4-pin interface, the PWM input is connected to the IN1, IN2, IN3, and IN4 pins as shown in Figure 18, and the driver operates in forward, reverse, and coast mode.
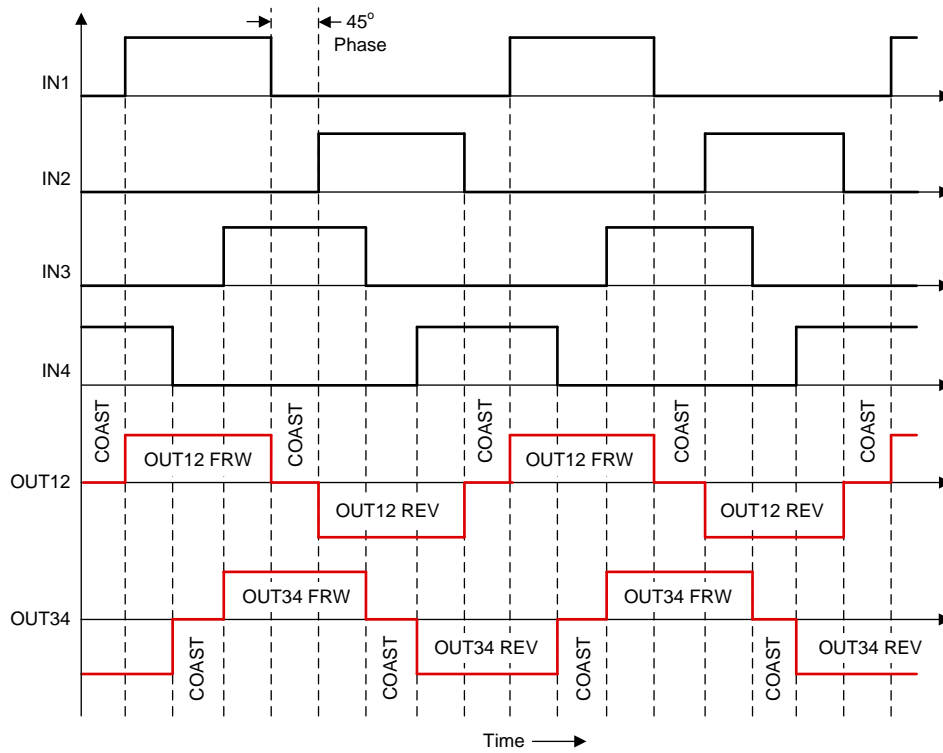
Figure 18. Half-Stepping Mode Using 4-Pin Interface

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7.3.8 Motor Driver Protection Circuits

The DRV8847 device is protected against VM undervoltage, overcurrent, open load, and over temperature events.

7.3.8.1 Overcurrent Protection (OCP)

The DRV8847 is protected against overcurrent by overcurrent protection trip. The OCP circuit on each FET disables the current flow through the FET by removing the gate drive. If this overcurrent detection continues for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge (or half-bridge in the independent interface) are disabled and the nFAULT pin is driven low. The DRV8847 device stays disabled until the retry time t_{RETRY} occurs whereas the DRV8847S device has a programmable option for auto-retry or the latch mode.

7.3.8.1.1 OCP Automatic Retry (Hardware Device and Software Device (OCPR = 0b))

After an OCP event in this mode, the corresponding half-bridges, full-bridge, or both bridges (depending on the MODE bits) are disabled and the nFAULT pin is driven low (see Table 10 and Table 11). The OCP and corresponding OCPx bits are latched high in the I^{2}C registers (see the *Register Map* section). Normal operation resumes automatically (motor driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses as shown in Figure 19. The OCP and OCPx bits remain latched until the t_{RETRY} period expires.
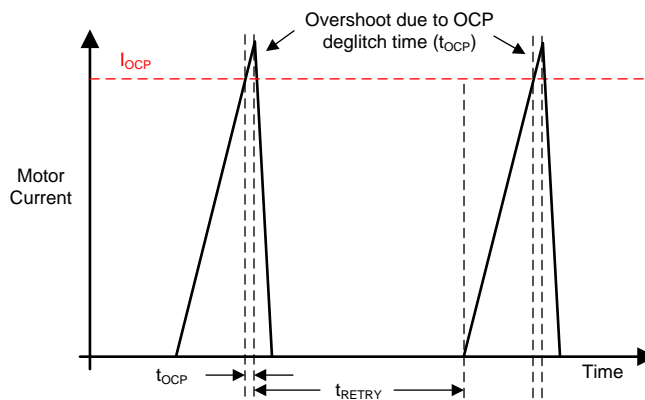
Figure 19. OCP Operation

7.3.8.1.2 OCP Latch Mode (Software Device (OCPR = 1b))

OCP latch mode is only available in the DRV8847S device. After an OCP event, the corresponding half-bridges, full-bridge, or both bridges (depending on the MODE bits) are disabled and the nFAULT pin is driven low. The OCP and corresponding OCPx bits are latched high in the I^{2}C registers (see the *Register Map* section). Normal operation continues (motor driver operation and the nFAULT pin is released) when the OCP condition is removed and a clear faults command is issued through the CLR_FLT bit.

7.3.8.2 Thermal Shutdown (TSD)

If the die temperature exceeds thermal shutdown limits (T_{TSD}), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature decreases to a value within the specified limits, normal operation resumes automatically. The nFAULT pin is released after operation starts again.

7.3.8.3 VM Undervoltage Lockout (VM_UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold as shown in Figure 20. The nFAULT pin is driven low during an undervoltage condition and is released after operation starts again.
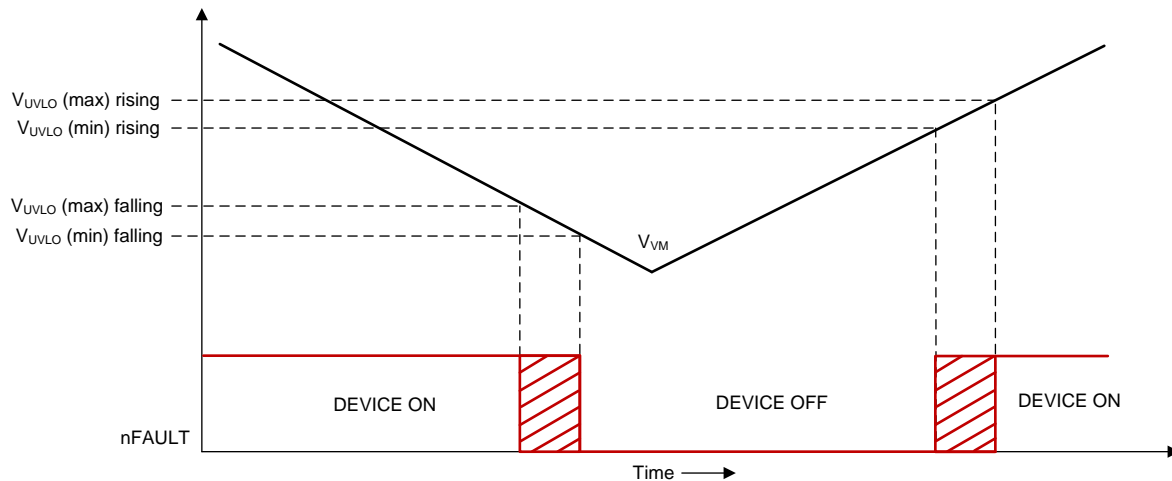
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Figure 20. VM UVLO Operation

7.3.8.4 Open Load Detection (OLD)

An open load detection feature is also implemented in this device. This diagnostic test runs at device power up or when the DRV8847 device comes out from sleep mode (rising edge on the nSLEEP pin). The OLD diagnostic test can run any time in the I²C variant device (DRV8847S) using the OLDOD (OLD On Demand) bit.

The OLD implementation is done on the full-bridge and the half-bridge. In the DRV8847 device, during an open-load condition, the half-bridges, full-bridge, or both bridges (depending on the MODE pin) are always operating and the nFAULT pin is pulled low. The user must reset the power to release the nFAULT pin by doing the OLD sequence again. Table 7 lists the different OLD scenarios for the DRV8847 device.

In the DRV8847S device, the user can program the full-bridge or half-bridge to be in the operating mode or the Hi-Z state, whenever an open-load condition is detected by using the OLDBO (OLD Bridge Operation) bit. Moreover, the nFAULT signaling on the OLD bit can be disabled using the OLDFD (OLD Fault Disable) bit. For detailed I²C register settings, see the *Register Map* section. Table 8 lists the different OLD scenarios for the DRV8847S device.

> **NOTE**
> For accurate OLD operation, the user must ensure that the motor is stationary (or current in connected load becomes zero) before the open load on-demand command is executed.

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Table 7. Open Load Detection in DRV8847

INTERFACE	LOAD TYPE	OLD	BRIDGE OPERATION	nFAULT
4-pin 2-pin	Full-Bridge Connected	NO	YES	NO
	Half-Bridge Connected	NO	YES	NO
	Bridge Open	YES	YES	YES
	One Half-Bridge Open	YES	YES	YES
Parallel bridge	Full-Bridge Connected	NO	YES	NO
	Half-Bridge Connected	NO	YES	NO
	Bridge Open	YES	YES	YES
	One Half-Bridge Open	YES	YES	YES
Independent bridge	Full-Bridge Connected	NO	YES	NO
	Half-Bridge Connected	NO	YES	NO
	Bridge Open	YES	YES	YES
	One Half-Bridge Open	YES	YES	YES

Table 8. Open Load Detection in DRV8847S (Full-bridge-12)

INTERFACE	LOAD TYPE	OLD	BRIDGE OPERATION[1]		nFAULT	OLD BITS			
			OLDBO = 0b	OLDBO = 1b		OLD1	OLD2	OLD3	OLD4
4-pin 2-pin	Full-bridge connected	NO	YES	YES	NO	0b	0b	X	X
	Half-bridge connected	NO	YES	YES	NO	0b	0b	X	X
	Bridge open	YES	YES	NO	YES	1b	1b	X	X
	One half-bridge open	YES	YES	NO	YES	1b or 0b [2]	0b or 1b	X	X
Parallel bridge	Full-bridge connected	NO	YES	YES	NO	0b	0b	X	X
	Half-bridge connected	NO	YES	YES	NO	0b	0b	X	X
	Bridge open	YES	YES	NO	YES	1b	1b	X	X
	One half-Bridge Open	YES	YES	NO	YES	1b or 0b	0b or 1b	X	X
Independent bridge	Full-Bridge Connected	NO	YES	YES	NO	0b	0b	X	X
	Half-Bridge Connected	NO	YES	YES	NO	0b	0b	X	X
	Bridge Open	YES	YES	NO	YES	1b	1b	X	X
	One Half-Bridge Open	YES	YES	NO	YES	1b or 0b	0b or 1b	X	X

(1)   The operation of the bridge is subjected to the selected mode type:
    (a) In 4-pin or 2-pin interface, the corresponding bridge is in the operating or Hi-Z state.
    (b) In parallel bridge (BDC) interface, both bridges are in the operating or Hi-Z state.
    (c) In independent bridge interface, the corresponding half-bridge is in the operating or Hi-Z state.
(2)   Depending on which half-bridge is open, the corresponding bit in the I^{2}C register is set.

As shown in Figure 21, during device wakeup, a constant current source pulls the OUT1 pin to the VDD voltage. If the voltage on the OUT2 pin is sensed to be less than the logic-low output voltage (V_{OL}), then an open-load condition is reported by pulling the nFAULT pin low. This test executes before the t_{WAKE} or t_{ON} time has elapsed. When an open load is detected, the nFAULT pin is latched low until the device is power cycled. A similar implementation is done for the OUT3 and OUT4 pins.

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Figure 21. Open Load Detect Circuit

7.4 Device Functional Modes

The DRV8847 device is active until the nSLEEP pin is pulled logic low. In sleep mode, the internal circuitry (charge pump and regulators) is disabled and all internal FETs are disabled (Hi-Z state).

NOTE

The t_{SLEEP} time must elapse before the device goes to sleep mode.

The device goes to operating mode automatically if the nSLEEP pin is pulled logic high. t_{WAKE} must elapse before the device is ready for inputs. Various functional modes are described in Table 9.

The DRV8847 device goes to a fault mode in the event of VM undervoltage (UVLO), overcurrent (OCP), open-load detection (OLD), and thermal shutdown (TSD). The functionality of each fault depends on the type of fault listed in Table 10 for the DRV8847 device and Table 11 for the DRV8847S device.

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Table 9. Functional Modes

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	2.7 V < V_{VM} < 18 V nSLEEP pin = 1	Operating	Operating
Sleep	2.7 V < V_{VM} < 18 V nSLEEP pin = 0	Disabled	Disabled
Fault	Any fault condition met	Depends on fault	Depends on fault

Table 10. Fault Support for DRV8847

FAULT	INTERFACE	CONDITION	REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (VM_UVLO)	All interfaces	VM < V_{UVLO}	nFAULT	Both H-bridges in Hi-Z state	Shutdown	**Automatic:** VM > V_{UVLO}
Overcurrent (OCP)	4-pin 2-pin	I > I_{OCP}	nFAULT	Corresponding H-bridges in Hi-Z state	Operating	**Automatic:** t_{RETRY}
	Parallel bridge			Both H-bridges in Hi-Z state		
	Independent bridge			Corresponding half-bridges in Hi-Z state		
Open load detect (OLD)	4-pin	Full-bridge open	nFAULT	H-bridge in operating mode	Operating	**Power cycle /RESET:** OUTx Connected
	2-pin Parallel bridge	Full-bridges open	nFAULT	Both H-bridges in operating mode		
	Independent bridge	Half-bridge open	nFAULT	Half-bridge in operating mode		
Thermal shutdown (TSD)	All interfaces	T_J > T_{TSD} (min 150°C)	nFAULT	Both H-bridges in Hi-Z state	Operating	T_J < T_{TSD} (T_{HYS} typ 40°C)

Table 11. Fault Support for DRV8847S

FAULT	MODE	CONDITION	REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (VM_UVLO)	All interfaces	VM < V_{UVLO}	nFAULT	Both H-bridges in Hi-Z state	Shutdown	**Automatic:** VM > V_{UVLO}
Overcurrent (OCP)	4-pin 2-pin	I > I_{OCP}	nFAULT	Corresponding H-bridges in Hi-Z state	Operating	**Automatic:** t_{RETRY}
	Parallel bridge			Both H-bridges in Hi-Z state		
	Independent bridge Interface			Corresponding half-bridges in Hi-Z state		
Open load detect (OLD)	4-pin	Full-bridge open	nFAULT	H-bridge in operating or Hi-Z state[1]	Operating	**Power cycle / RESET:** OUTx Connected
	2-pin Parallel bridge	Full-bridges open	nFAULT	Both H-bridges in operating or Hi-Z state		
	Independent bridge	Half-bridge open	nFAULT	Half-bridge in operating or Hi-Z state		
Thermal shutdown (TSD)	All interfaces	T_J > T_{TSD} (min 150°C)	nFAULT	Both H-bridges in Hi-Z state	Operating	T_J < T_{TSD} (T_{HYS} typ 40°C)

(1)   The state of the bridge in OLD is dependent on the OLDBO bit as listed in Table 16.

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7.5 Programming

This section applies only to the DRV88847S device (I²C variant).

7.5.1 I²C Communication

7.5.1.1 I²C Write

To write on the I2C bus, the master device sends a START condition on the bus with the address of the 7-bit slave device. Also, the last bit (the R/W bit) is set to 0b, which signifies a write. After the slave sends the acknowledge bit, the master device then sends the register address of the register to be written. The slave device sends an acknowledge (ACK) signal again which notifies the master device that the slave device is ready. After this process, the master device sends 8-bit write data and terminates the transmission with a STOP condition.
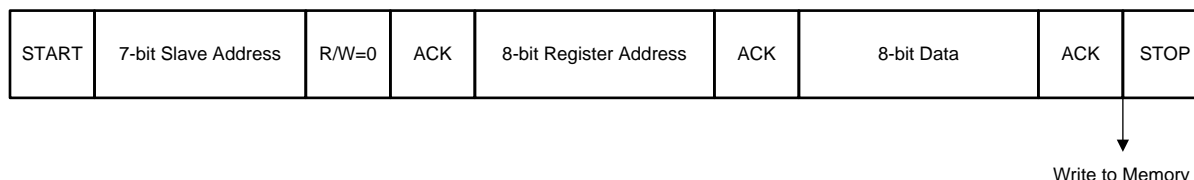
Figure 22. I²C Write Sequence

7.5.1.2 I²C Read

To read from a slave device, the master device must first communicate to the slave device which register will be read from. This communication is done by the master starting the transmission similarly to the write process which is by setting the address with the R/W bit equal to 0b (signifying a write). The master device then sends the register address of the register to be read from. When the slave device acknowledges this register address, the master device sends a START condition again, followed by the slave address with the R/W bit set to 1b (signifying a read). After this process, the slave device acknowledges the read request and the master device releases the SDA bus, but continues supplying the clock to the slave device.

During this part of the transaction, the master device becomes the master-receiver, and the slave device becomes the slave-transmitter. The master device continues sending out the clock pulses, but releases the SDA line so that the slave device can transmit data. At the end of the byte, the master device send a negative-acknowledge (NACK) signal, signaling to the slave device to stop communications and release the bus. The master device then sends a STOP condition.
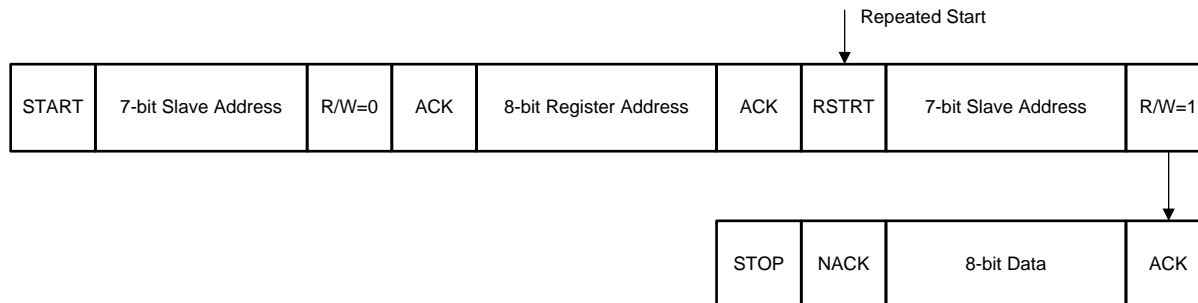
Figure 23. I²C Read Sequence

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Programming (continued)

7.5.2 Multi-Slave Operation

Multi-slave operation is used to control multiple DRV8847S devices through one I²C line as shown in Figure 24. The default device address of the DRV8847 device is 0x60 (7-bit address). Therefore, any DRV8847S device can be accessed using this address. The steps for multi-slave configuration for programming device-1 out of 4 connected devices (as shown in Figure 24) are as follows:
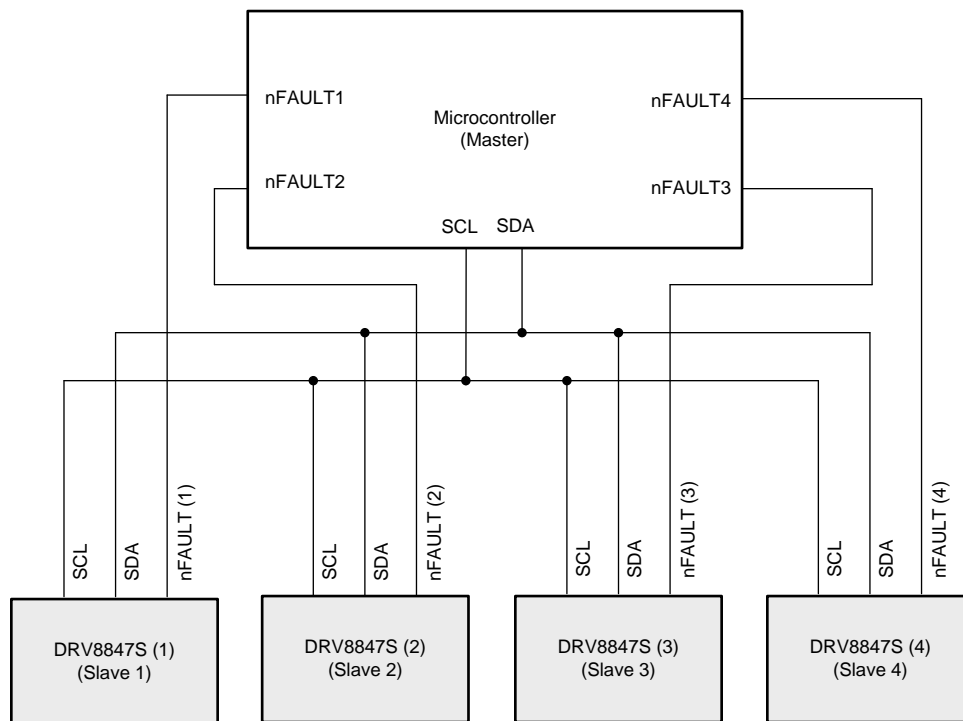
Figure 24. Multi-Slave Operation of DRV8847S

- The DRV8847S device variant is configured for multi-slave operation by writing the DISFLT bit (IC2_CON register) of all connected devices to 1b. This step will disable the nFAULT output pin of all DRV8847S, to avoid any race condition between master and slave I²C device.
- Pull the nFAULT pins (nFAULT2, nAFULT3, and nFAULT4 pins) of three devices (2, 3, and 4) to low to release the I²C buses of the slave device (device-2, device-3 and device-4). Now only device-1 is connected to master.
- Since, only one device, DRV8847S (1), is connected to the controller, and, therefore, its slave address can be reprogrammed from default 0x60 (7-bit address) to another unique address.
- Similarly, the slave address (SLAVE_ADDR) of the other three devices (device-2, device-3 and device-4) can be reprogrammed sequentially to unique addresses by a combination of nFAULT pins.
- When all slave addresses are reprogrammed, resume the DISFLT bit to 0b (IC2_CON register). This will enable the nFAULT output pin for fault flagging.
- All the nFAULT pins are released and a multi-slave setup is complete. Now all connected slave devices can be accessed using the newly reprogrammed address.
- The above steps should be repeated for any device in case of a power reset (nSLEEP). .

7.6 Register Map

Table 12 lists the memory-mapped I^{2}c registers for the DRV8847 device. The I^{2}C registers are used to configure the DRV8847S device and for device diagnostics.

NOTE

Do not modify reserved registers or addresses not listed in the register map (Table 12). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0b.

Table 12. I^{2}C Registers

Address	Acronym	Register Name	7	6	5	4	3	2	1	0	Access	Section
0x00	SLAVE_ADDR	Slave Address	RSVD	SLAVE_ADDR							RW	Go
0x01	IC1_CON	IC1 Control	TRQ	IN4	IN3	IN2	IN1	I2CBC	MODE		RW	Go
0x02	IC2_CON	IC2 Control	CLRFLT	DISFLT	RSVD	DECAY	OCPR	OLDOD	OLDFD	OLDBO	RW	Go
0x03	SLR_STATUS1	Slew Rate and Fault Status-1	RSVD	SLR	RSVD	nFAULT	OCP	OLD	TSDF	UVLOF	RW	Go
0x04	STATUS2	Fault Status-2	OLD4	OLD3	OLD2	OLD1	OCP4	OCP3	OCP2	OCP1	R	Go

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Complex bit access types are encoded to fit into small table cells. Table 13 shows the codes that are used for access types in this section.

Table 13. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.6.1 Slave Address Register (Address = 0x00) [reset = 0x60]

Slave Address is shown in Figure 25 and described in Table 14.

Figure 25. Slave Address Register

7	6	5	4	3	2	1	0
RSVD	SLAVE_ADDR						
R-0b	R/W-1100000b						

Table 14. Slave Address Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6-0	SLAVE_ADDR	R/W	1100000b	Slave address (8 bit) The default value is 0x60

7.6.2 IC1 Control Register (Address = 0x01) [reset = 0x00]

IC1 Control is shown in Figure 26 and described in Table 15.

Figure 26. IC1 Control Register

7	6	5	4	3	2	1	0
TRQ	IN4	IN3	IN2	IN1	I2CBC	MODE	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

Table 15. IC1 Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRQ	R/W	0b	0b = Torque scalar set to 100% 1b = Torque scalar set to 50%
6	IN4	R/W	0b	The INx bits are used to control the bridge operation.
5	IN3	R/W	0b	The INx bits are used to control the bridge operation.
4	IN2	R/W	0b	The INx bits are used to control the bridge operation.
3	IN1	R/W	0b	The INx bits are used to control the bridge operation.
2	I2CBC	R/W	0b	0b = Bridge control configured by using the INx pins 1b = Bridge control configured by using the INx bits
1-0	MODE	R/W	00b	00b = 4-pin interface 01b = 2-pin interface 10b = Parallel interface 11b = Independent mode

7.6.3 IC2 Control Register (Address = 0x02) [reset = 0x00]

IC2 Control is shown in Figure 27 and described in Table 16.

Figure 27. IC2 Control Register

7	6	5	4	3	2	1	0
CLRFLT	DISFLT	RSVD	DECAY	OCPR	OLDOD	OLDFD	OLDBO
R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 16. IC2 Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLRFLT	R/W	0b	Set this bit to issue a clear FAULT command. This command clears all FAULT bits other than the OLD and OLDx bits. This bit reset to 0b after clearing all the faults. 0b = No clear FAULT command issued 1b = Clear FAULT command issued
6	DISFLT	R/W	0b	0b = nFAULT pin not disable 1b = nFAULT pin is disabled
5	RSVD	R	0b	Reserved
4	DECAY	R/W	0b	0b = 25% fast decay 1b = 100% slow decay
3	OCPR	R/W	0b	0b = OCP auto retry mode 1b = OCP latch mode
2	OLDOD	R/W	0b	0b = Idle 1b = OLD on-demand is activated
1	OLDFD	R/W	0b	0b = Fault signaling on OLD 1b = No fault signaling on OLD
0	OLDBO	R/W	0b	0b = Bridge operating on OLD 1b = Bridge Hi-Z on OLD

NOTE

Errata: In current silicon, the CLR_FLT does not reset to 0b after clearing all the faults. This will be fixed in next revision.

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7.6.4 Slew-Rate and Fault Status-1 Register (Address = 0x03) [reset = 0x40]

Fault Status-1 is shown in Figure 28 and described in Table 17.

Figure 28. Fault Status-1 Register

7	6	5	4	3	2	1	0
RSVD	SLR	RSVD	nFAULT	OCP	OLD	TSDF	UVLOF
R-0b	R/W-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 17. Fault Status-1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	SLR	R/W	0b	0b = 150 ns 1b = 300 ns
5	RSVD	R	0b	Reserved
4	nFAULT	R	0b	0b = No FAULT detected (mirrors the nFAULT pin) 1b = FAULT detected
3	OCP	R	0b	0b = No OCP detected 1b = OCP detected
2	OLD	R	0b	0b = No open load detected 1b = Open load detected
1	TSDF	R	0b	0b = No TSD fault detected 1b = TSD fault detected
0	UVLOF	R	0b	0b = No UVLO fault detected 1b = UVLO fault detected

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Product Folder Links: *DRV8847*

7.6.5 Fault Status-2 Register (Address = 0x04) [reset = 0x00]

Fault Status-2 is shown in Figure 29 and described in Table 18.

Figure 29. Fault Status-2 Register

7	6	5	4	3	2	1	0
OLD4	OLD3	OLD2	OLD1	OCP4	OCP3	OCP2	OCP1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 18. Fault Status-2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OLD4	R	0b	0b = No open load detected on OUT4 1b = Open load detected on OUT4
6	OLD3	R	0b	0b = No open load detected on OUT3 1b = Open load detected on OUT3
5	OLD2	R	0b	0b = No open load detected on OUT2 1b = Open load detected on OUT2
4	OLD1	R	0b	0b = No open load detected on OUT1 1b = Open load detected on OUT1
3	OCP4	R	0b	0b = No OCP detected on OUT4 1b = OCP detected on OUT4
2	OCP3	R	0b	0b = No OCP detected on OUT3 1b = OCP detected on OUT3
1	OCP2	R	0b	0b = No OCP detected on OUT2 1b = OCP detected on OUT2
0	OCP1	R	0b	0b = No OCP detected on OUT1 1b = OCP detected on OUT1

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Product Folder Links: *DRV8847*

8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8847 device is used in applications for stepper or brushed DC motor control.

8.2 Typical Application

The user can configure the DRV8847 for stepper motor and dual BDC motor applications as described in this section.

8.2.1 Stepper Motor Application

Figure 30 shows the typical application of the DRV8847 device to drive a stepper motor.
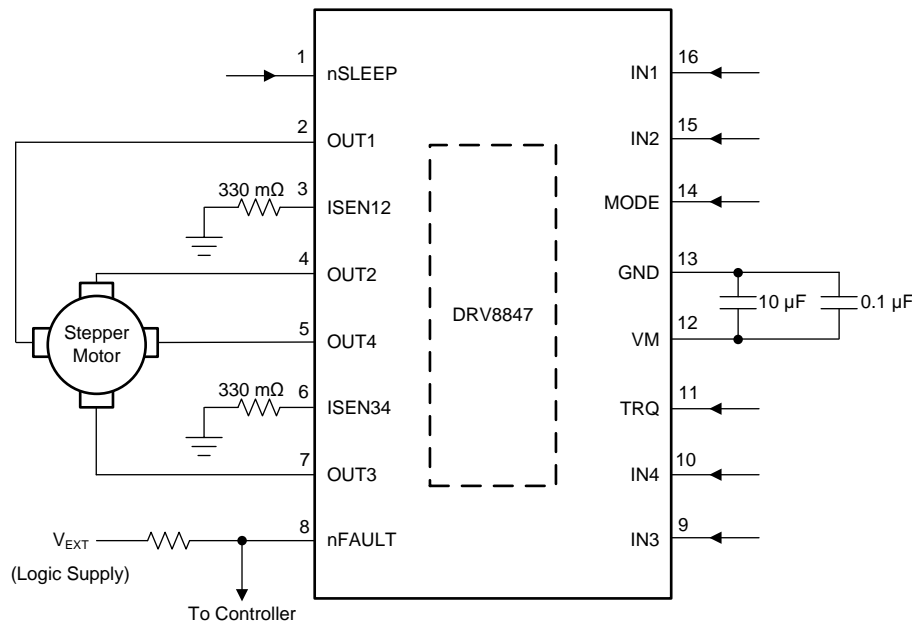
Figure 30. Typical Application Schematic of Device Driving Stepper Motor

8.2.1.1 Design Requirements

Table 19 lists design input parameters for system design.

Table 19. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	12 V
Motor winding resistance	R_L	34 Ω/phase
Motor winding inductance	L_L	33 mH/phase
Motor RMS current	I_{RMS}	350 mA
Target trip current	I_{TRIP}	350 mA
Trip current reference voltage (internal voltage)	V_{TRIP}	150 mV

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Current Regulation

The trip current (I_{TRIP}) is the maximum current driven through either winding. The amount of this current depends on the sense resistor value ($R_{SENSExx}$) as shown in Equation 4 (Considering torque setting (TRQ) as 100%).

$$I_{TRIP} = \frac{Torque \times V_{TRIP}}{R_{SENSExx}}$$

(4)

The I_{TRIP} current is set by a comparator which compares the voltage across the $R_{SENSExx}$ resistor to a reference voltage. To avoid saturation of the motor, the I_{TRIP} current must be calculated as shown in Equation 5.

$$I_{TRIP} = \frac{V_{VM}}{R_L\ (\Omega) + R_{DS(ON)\_HS}\ (\Omega) + R_{DS(ON)\_LS}\ (\Omega) + R_{SENSExx}\ (\Omega)}$$

where

- V_{VM} is the motor supply voltage.
- R_L is the motor winding resistance.
- $R_{DS(ON)\_HS}$ and $R_{DS(ON)\_LS}$ are the high-side and low-side on-state resistance of the FET. (5)

For an I_{TRIP} value of 350 mA, the value of the sense resistor ($R_{SENSExx}$) is calculated as shown in Equation 6.

$$R_{SENSE12} = R_{SENSE34} = \frac{V_{TRIP}}{I_{TRIP}} = \frac{150\ mV}{350\ mA} = 428.6\ m\Omega$$

(6)

Select the closest available value of 440 mΩ for the sense resistors. Selecting this value will effect the current accuracy by 2.8%.

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8.2.2 Dual BDC Motor Application

Figure 31 shows the typical application of DRV8847 device to drive dual BDC motors.
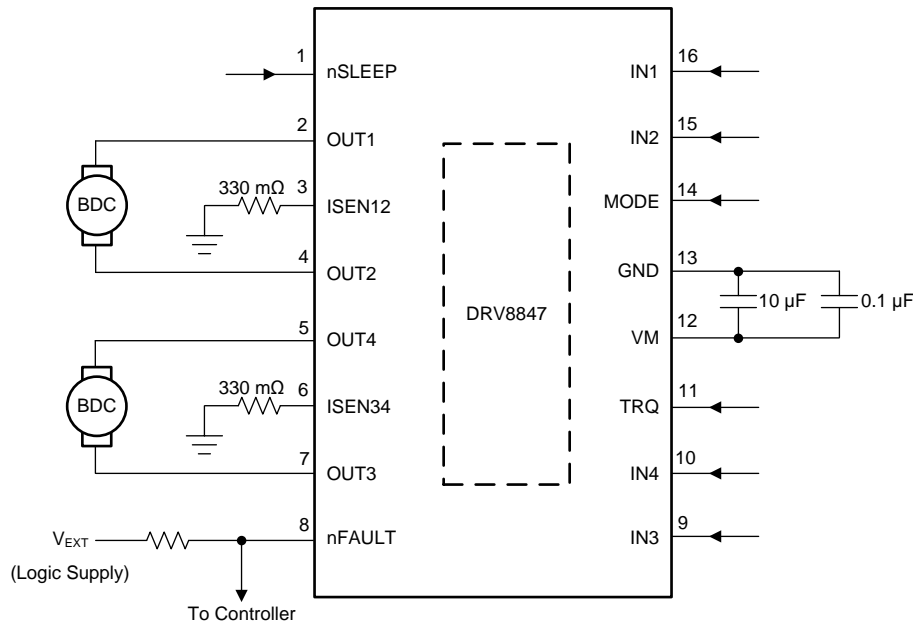
Figure 31. Typical Application Schematic of Device Driving Two BDC Motors

8.2.2.1 Design Requirements

Table 20 lists the design input parameters for system design.

Table 20. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	12 V
Motor winding resistance	R_L	13.2 Ω
Motor winding inductance	L_L	500 µH
Motor RMS current	I_{RMS}	490 mA
Motor start-up current	I_{START}	900 mA
Target trip current	I_{TRIP}	1.2 A
Trip current reference voltage (internal voltage)	V_{TRIP}	150 mV

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Motor Voltage

The motor voltage used in an application depends on the rating of the selected motor and the desired revolutions per minute (RPM). A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2.2 Current Regulation

The trip current (I_{TRIP}) is the maximum current driven through either winding. Because the peak current (start current) of the motor is 900 mA, the I_{TRIP} current level is selected to be just greater than the peak current. The selected I_{TRIP} value for this example is 1.2 A. Therefore, use Equation 7 to select the value of the sense resistors ($R_{SENSE12}$ and $R_{SENSE34}$) connected to the ISEN12 and ISEN34 pins.

$$R_{SENSE12} = R_{SENSE34} = \frac{V_{TRIP}}{I_{TRIP}} = \frac{150\ mV}{1.2\ A} = 125\ m\Omega$$

(7)

8.2.2.2.3 Sense Resistor

For optimal performance, the sense resistor must:
- Be a surface mount component
- Have low inductance
- Be rated for high enough power
- Be placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. In this example, the peak current is 900 mA, the RMS motor current is 490 mA, and the sense resistor value is 125 mΩ. Therefore, the sense resistors ($R_{SENSE12}$ and $R_{SENSE34}$) dissipate 30 mW (490 mA^2 × 125 mΩ = 30 mW). The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a printed circuit board (PCB) is shared with other components generating heat, margin should be added. For best practice, measure the actual sense resistor temperature in a final system, along with the power MOSFETs, because those components are often the hottest.

Because power resistors are larger and more expensive than standard resistors, the common practice is to use multiple standard resistors in parallel, between the sense node and ground. This practice distributes the current and heat dissipation.

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9 Power Supply Recommendations

The DRV8847 device is designed to operate from an input voltage supply (V_{VM}) range from 2.7 V to 18 V. Place a 0.1-µF ceramic capacitor rated for VM as close to the DRV8847 device as possible. In addition, a bulk capacitor with a value of at least 10 µF must be included on the VM pin.

9.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. The amount of bulk capacitance depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor start-up current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.
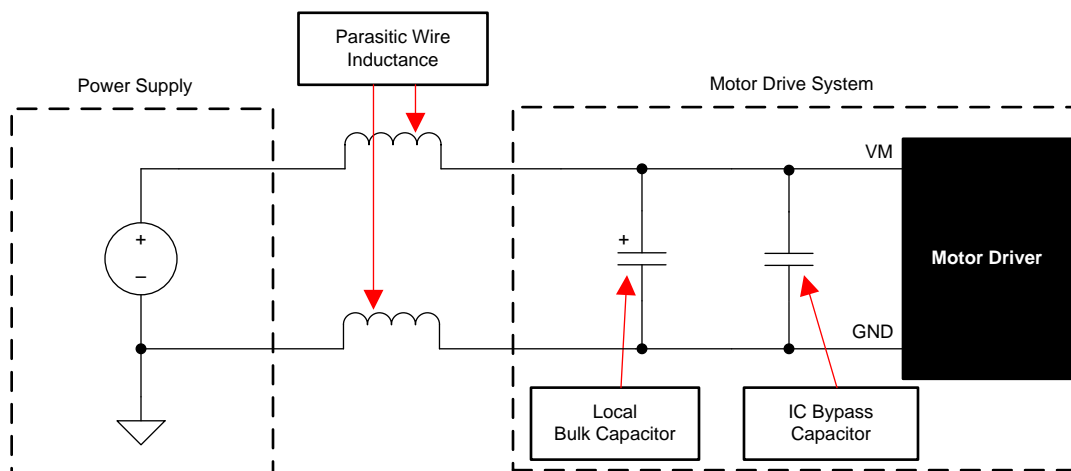
Figure 32. Setup of Motor Drive System With External Power Supply

Product Folder Links: *DRV8847*

10 Layout

10.1 Layout Guidelines

Bypass the VM pin to ground using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF and rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

10.2 Layout Example
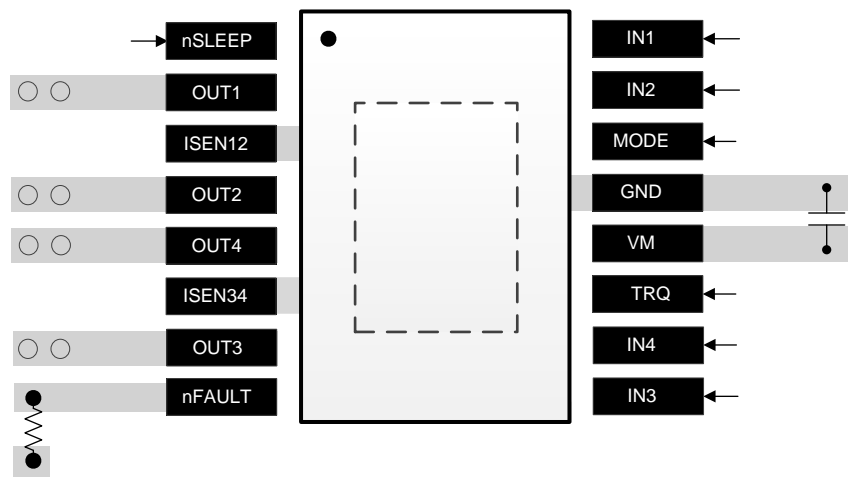
Figure 33. Layout Recommendation of 16-Pin TSSOP Package for Single-Layer Board
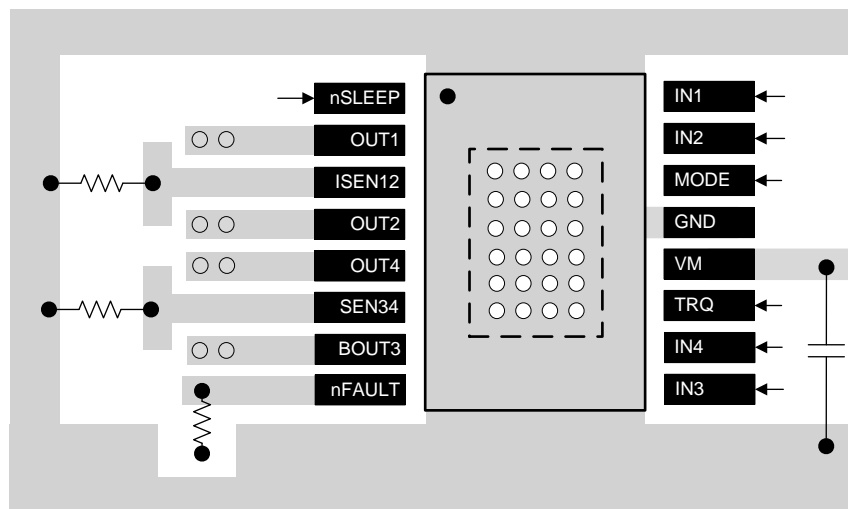
Figure 34. Layout Recommendation of 16-Pin HTSSOP Package for Double-Layer Board

ADVANCE INFORMATION

10.3 Thermal Considerations

10.3.1 Maximum Output Current

In actual operation, the maximum output current that is achievable with a motor driver is a function of the die temperature. This die temperature is greatly affected by ambient temperature and PCB design. Essentially, the maximum motor current is the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to avoid thermal shutdown.

The dissipation ratings given in the data sheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected without putting the device in thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed through measurement or thermal simulation.

10.3.2 Thermal Protection

The DRV8847 device has thermal shutdown (TSD) as described in the *Maximum Output Current* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature deceases 40°C.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heat-sinking, or too high an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8847 device is dominated by the DC power dissipated in the output FET resistance ($R_{DS(ON)\_HS}$ and $R_{DS(ON)\_LS}$). Additional power is dissipated because of PWM switching losses. These losses are dependent on the PWM frequency, rise and fall times, and VM supply voltages. These switching losses are typically on the order of 10% to 30% of the DC power dissipation.

Use Equation 8 to estimate the DC power dissipation of one H-bridge.

$$P_{TOT} = R_{DS(ON)\_LS} \times I_{OUT(RMS)}{}^2 + R_{DS(ON)\_HS} \times I_{OUT(rms)}{}^2$$

where

- P_{TOT} is the total power dissipation
- $I_{OUT(RMS)}$ is the RMS output current being applied to motor
- $R_{DS(ON)\_HS}$ and $R_{DS(ON)\_LS}$ are the high-side and low-side on-state resistance of the FET (8)

NOTE

The value of $R_{DS(ON)\_HS}$ and $R_{DS(ON)\_LS}$ increases with temperature. Therefore, as the device heats, the power dissipation increases. This relationship must be considered when sizing the heat-sink.

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Product Folder Links: *DRV8847*

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *DRV8847EVM User's Guide*
- Texas Instruments, *DRV8847EVM and DRV8847SEVM Software User's Guide*
- Texas Instruments, *Small Motors in Large Appliances* TI TechNote

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8847PWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV8847PWPR	ACTIVE	HTSSOP	PWP	16	1	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RTE (S−PWQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

PIN 1 INDEX AREA
TOP AND BOTTOM

SEATING PLANE

0,20 REF.

0,80 / 0,70

0,08

0,05 / 0,00

16X 0,50 / 0,30

EXPOSED THERMAL PAD

16X 0,30 / 0,18

0,50

3,15 / 2,85

3,15 / 2,85
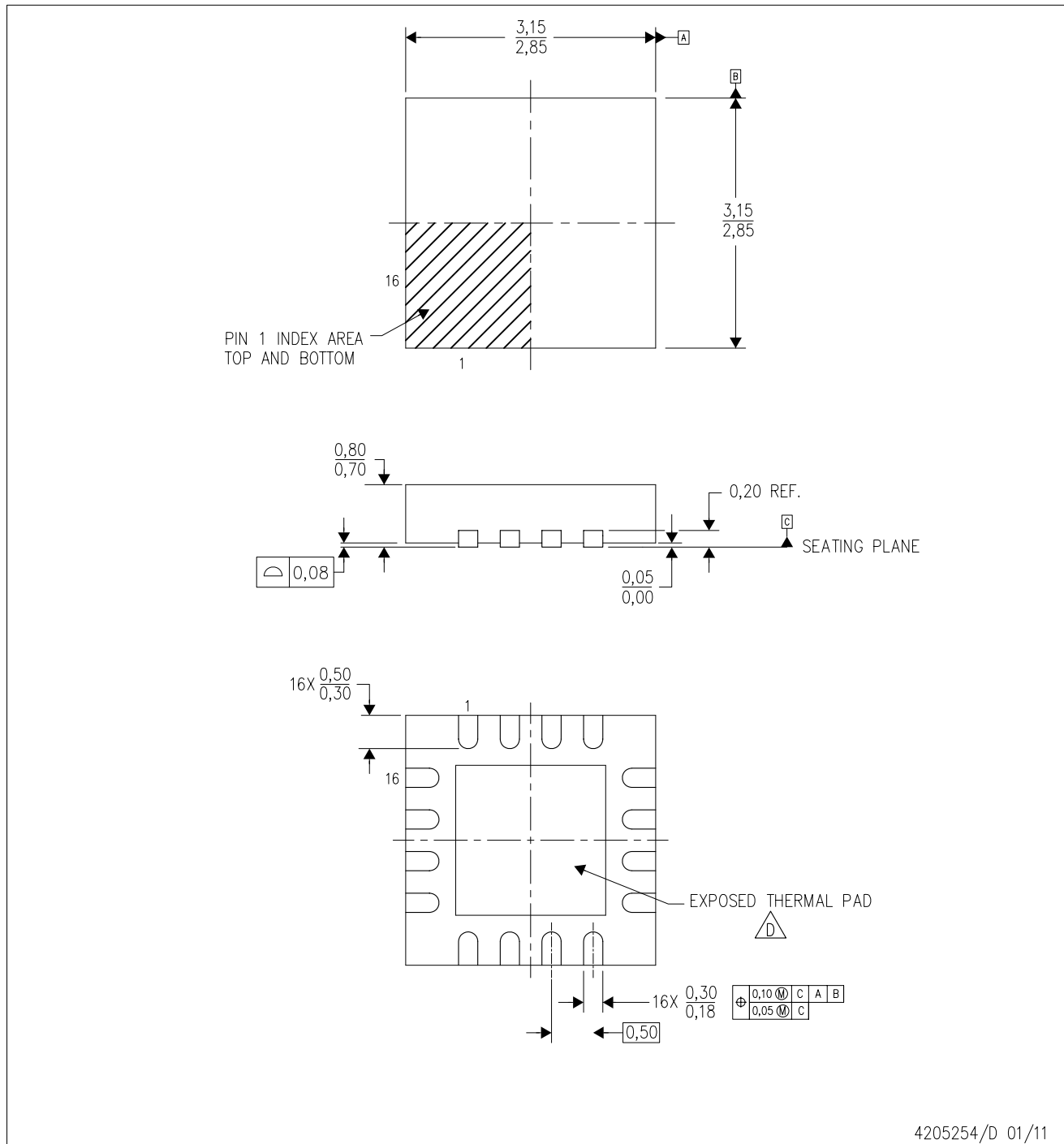
4205254/D 01/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−220.

TEXAS INSTRUMENTS
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PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE
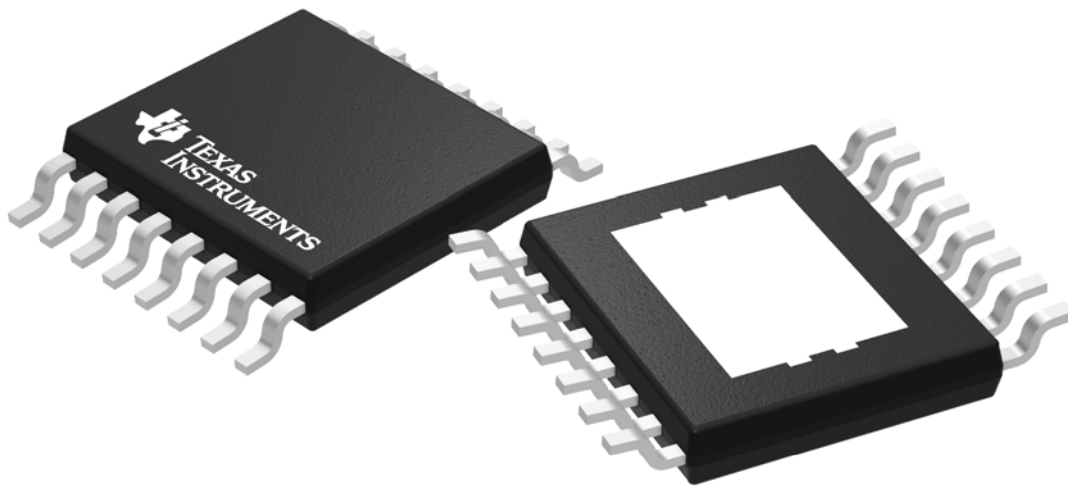
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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IMPORTANT NOTICE