

PGA970 LVDT Sensor Signal Conditioner

1 Features

- Analog Features
 - Analog Front End for LVDT Sensors
 - On-Chip Temperature Sensor
 - Programmable Gain
 - Two 24-Bit Digital Demodulators
 - 24-Bit Auxiliary Analog-to-Digital Converter
 - 14-Bit Output DAC
- Digital Features
 - Microcontroller Core
 - ARM Cortex-M0 at 8 MHz
 - On-Chip Oscillator
 - Memory
 - 8 KBytes FRAM for Program and Configuration Data
 - 2 KBytes RAM for Variables
 - 512 Bytes of RAM for Waveform Generator
- Peripheral Features
 - Serial Peripheral Interface (SPI)
 - One-Wire Interface
 - Ratiometric and Absolute Voltage Output
 - 4- to 20-mA Current Loop Interface (with external components)
 - Power Management Control
 - Analog Low-Voltage Detect

- Industrial Temperature Range: -40°C to 125°C
- Power Supply:
 - Depletion MOSFET Gate Controller
 - ABSMAX: -0.3 to 33 V
 - Operational: 3.5 to 30 V
- Package Option: QFP-48

2 Applications

- LVDT Sensor Signal Conditioning
- RVDT Sensor Signal Conditioning
- Resolver Signal Conditioning
- Conductivity Measurement

3 Description

The PGA970 is an interface device for LVDT sensors. The device incorporates analog front end that directly connects to the sense element and has voltage regulators and oscillator. The device also includes analog-to-digital converters, ARM Cortex-M0 microprocessor and FRAM memory. Sensor compensation algorithms can be implemented in software. The PGA970 includes multiple output interfaces.

Device Information⁽¹⁾

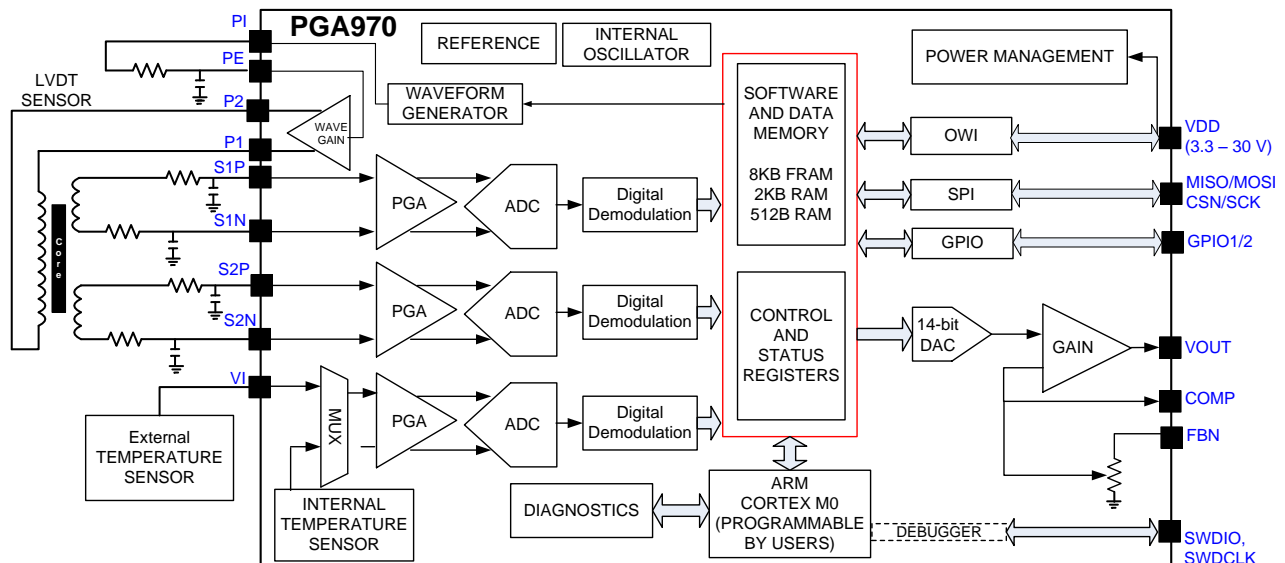
ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
PGA970QPHPR	QFP (48)	9.00 mm x 9.00 mm
PGA970QPHPT		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

General Features

PRODUCT PREVIEW

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

4 Device and Documentation Support

4.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.2 Trademarks

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4.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA970QPHPR	PREVIEW	HTQFP	PHP	48	1000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MS-026

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