

# □ MN101E46 Series

| Type                               | MN101E46G   | MN101E46N | MN101E46R | MN101EF46R      |
|------------------------------------|---|-----------|-----------|-----------------|
| Internal ROM type                  | Mask ROM  |           |           | FLASH           |
| ROM (byte)                         | 128K  | 508K      | 928K      |                 |
| RAM (byte)                         | 4K  |           | 6K        | 8K              |
| Package (Lead-free)                | TQFP128-P-1414C   |           |           | TQFP128-P-1414A |
| Minimum Instruction Execution Time | 0.1 $\mu$ s (at 2.2 V to 3.6 V, 10 MHz)<br>0.125 $\mu$ s (at 1.8 V to 3.6 V, 8 MHz)<br>61 $\mu$ s (at 1.8 V to 3.6 V, 32.768 kHz) |           |           |                 |

## ■ Interrupts

RESET. Watchdog. External 0 to 3. Timer 0 to 3. Timer 6. Timer 7 (2 systems). Timer 8 (2 systems). Time base. Serial 0. Serial 1 (2 systems). A/D conversion finish. Automatic transfer finish. LCD frame finish

## ■ Timer Counter

8-bit timer  $\times$  5

Timer 0 .....Square-wave/8-bit PWM output. Event count. Remote control carrier output. Simple pulse width measurement

Timer 1 .....Square-wave output. Event count. Serial transfer clock output

Timer 2 .....Square-wave/8-bit PWM output. Serial transfer clock output. Event count. Simple pulse width measurement

Timer 3 .....Square-wave output. Event count. Serial transfer clock output

Timer 6 .....8-bit freerun timer

Timer 0, 1 can be cascade-connected

Timer 2, 3 can be cascade-connected

16-bit timer  $\times$  2

Timer 7, 8 .....Square-wave output. 16-bit PWM output (cycle/duty continuous variable). Event count. Pulse width measurement.

Input capture

Time base timer: One-minute count setting

Watchdog timer  $\times$  1

## ■ Serial interface

Synchronous type/Single-master I<sup>2</sup>C  $\times$  1: Serial 0

Synchronous type/UART (full-duplex)  $\times$  1: Serial 1

## ■ DMA controller

Maximum transfer cycles: 255

Starting factor: External request. Various types of interrupt. Software

Transfer mode: 1-byte transfer. Word transfer. Burst transfer

## ■ I/O Pins

I/O 67 : Common use

Output 40 : LCD drive output exclusive use

## ■ A/D converter

10-bit  $\times$  3 channels (External input 2 channels, Internal 1.8 V input 1 channel)

## ■ Display control function

Dot Matrix type LCD control function

Display size up to 2048 pixels (32 COM  $\times$  64 SEG)

LCD drivers: COM output maximum 32 pins / SEG output maximum 67 pins (3 pins has dual function for COM/SEG)

1/8, 1/16, 1/24, 1/32 duty

1/5, 1/6 bias

LCD panel drive voltage maximum 5.5 V

Built-in LCD voltage booster and LCD voltage dividing resistor

16-level contrast control

Bright and dark 2-step level display function

Monochrome inversion function

## ■ Special Ports

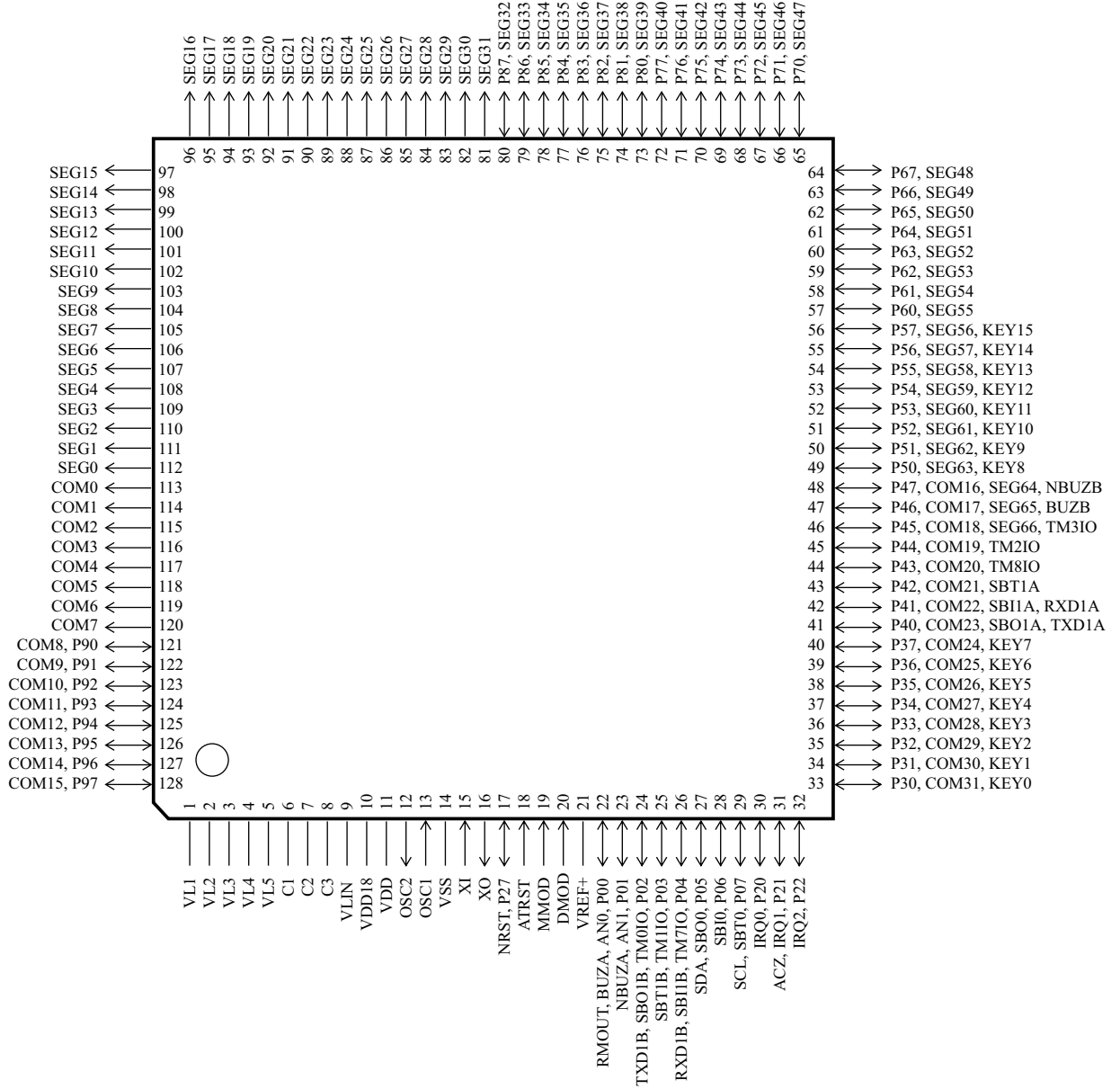
Buzzer output. Remote control carrier output

■ ROM Correction

Correcting address designation: Up to 7 addresses possible

■ Pin Assignment

TQFP128-P-1414A, TQFP128-P-1414C



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