ISL91117

High Efficiency Synchronous Boost Converter with 4.2A Switches and Output Disconnect

FN8569
Rev 3.00
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The ISL91117 is a highly-integrated boost switching regulator for battery powered applications. The device provides a power supply solution for products using dual-cell or three-cell alkaline, NiCd or NiMH, or one-cell Li-ion or Li-polymer battery.

This device is capable of delivering an output current of 1.5A with PVIN = 3.3V and VOUT = 5V. The use of a synchronous rectifier maximizes efficiency at high loads. No-load quiescent current of only 35µA optimizes efficiency under light-load conditions. Forced PWM and/or synchronization to an external clock may also be selected for noise sensitive applications.

The ISL91117 is designed for standalone applications and supports 5V fixed output voltage or variable output voltages with an external resistor divider. Power supply solution size is minimized by a 2.34mm x 1.72mm WLCSP and a 2.6MHz switching frequency, which allows for the use of tiny, low-profile inductors and ceramic capacitors to minimize the size of the solution.

Related Literature

- AN1918, ISL91117II7-EVZ, ISL91117IIA-EVZ Evaluation Boards

Features

- Input voltage range: 1.8V to 4.8V
- Fixed 5V or adjustable output
- Output current: up to 1.5A (PVIN = 3.3V, VOUT = 5V)
- High efficiency: up to 96%
- 35µA quiescent current maximizes light-load efficiency
- True input-output disconnect when disabled
- 2.6MHz switching frequency minimizes external component size
- Selectable forced-PWM mode and external synchronization
- Fully protected for short-circuit, over-temperature and undervoltage
- Small 2.34mm x 1.72mm WLCSP

Applications

- Smart phones and tablets
- Wireless communication devices
- Products including portable HDMI and USB-OTG

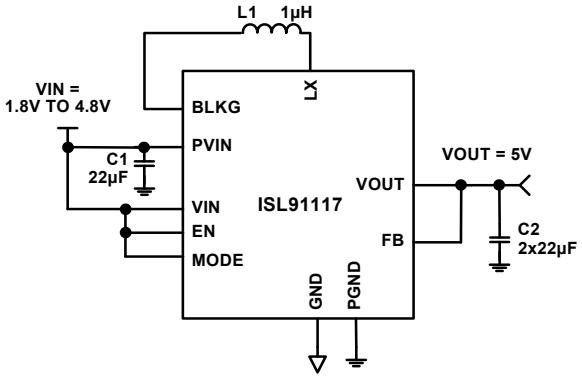


FIGURE 1. TYPICAL FIXED OUTPUT APPLICATION

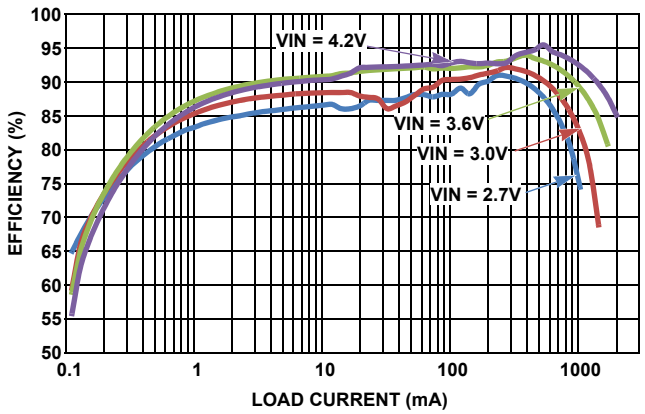
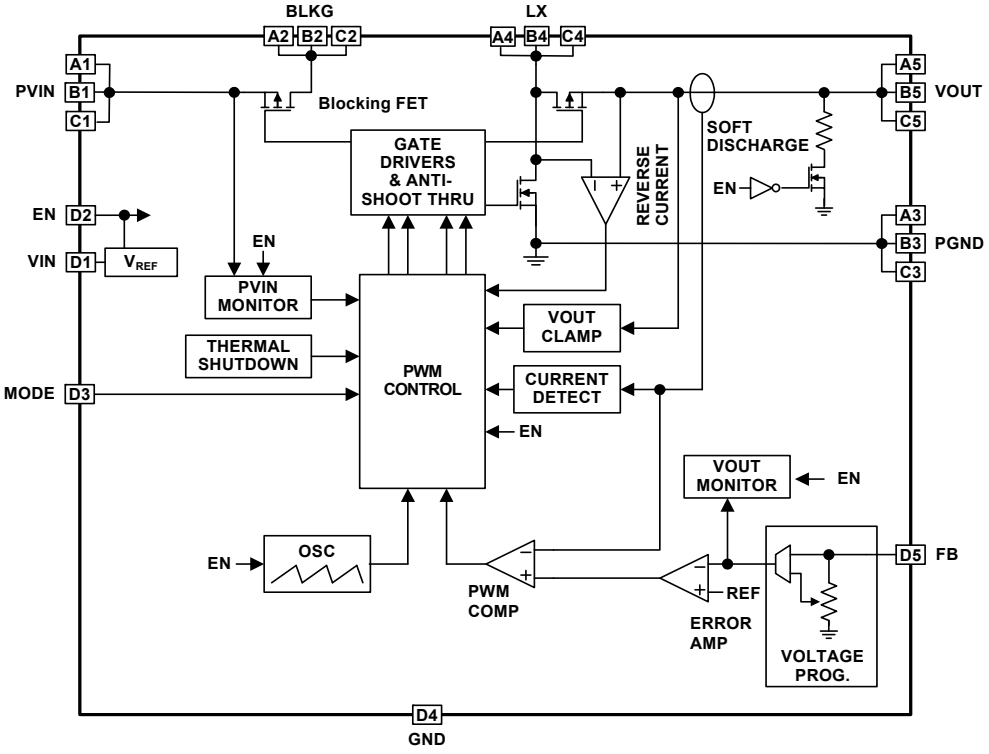


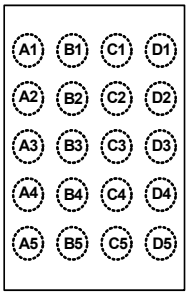
FIGURE 2. EFFICIENCY vs LOAD CURRENT (VOUT = 5V)

Block Diagram



Pin Configuration

ISL91117
(4x5 WLCSP)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A5, B5, C5	VOUT	Boost output. Connect 2x22µF capacitor to PGND.
A4, B4, C4	LX	Switching node of the boost converter.
A3, B3, C3	PGND	Power ground for high switching current.
A2, B2, C2	BLKG	Blocking FET terminal. Connect the input side of the inductor.
A1, B1, C1	PVIN	Power input. Range: 1.8V to 4.8V. Connect a 22µF capacitor to PGND.
D1	VIN	Supply input. Range: 1.8V to 4.8V.
D2	EN	Logic input, drive HIGH to enable device.
D3	MODE	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation. Also, this pin can be used with an external clock sync input. Range: 2.75MHz to 3.25MHz. Maximum voltage on this pin should be limited to VIN.
D4	GND	Analog ground pin.
D5	FB	Voltage feedback pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL91117II7Z-T (Note 4)	GAXC	5	-40 to +85	20 Ball WLCSP	W4x5.20F
ISL91117II7Z-T7A (Note 4)	GAXC	5	-40 to +85	20 Ball WLCSP	W4x5.20F
ISL91117IIAZ-T	GAXB	ADJ.	-40 to +85	20 Ball WLCSP	W4x5.20F
ISL91117IIAZ-T7A	GAXB	ADJ.	-40 to +85	20 Ball WLCSP	W4x5.20F
ISL91117II7-EVZ (Note 4)	Evaluation Board for ISL91117II7Z				
ISL91117IIA-EVZ	Evaluation Board for ISL91117IIAZ				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL91117 For more information on MSL please see techbrief TB363.
4. Contact Intersil for Availability.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX (Note 7). . . . . -0.3V to 6.5V
FB (ISL91117IIAZ) . . . . . -0.3V to 2.7V
FB (ISL91117II7Z) . . . . . -0.3V to 6.5V
MODE/SYNC . . . . . -0.3V to VIN+0.3V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2.5kV
Machine Model (Tested per JESD22-A115-A). 200V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ball WLCSP (Notes 5, 6).	66	1.0

Maximum Junction Temperature (Plastic Package) . . . . . .+125°C
Storage Temperature Range. . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range . . . . . 1.8V to 4.8V
Load Current Range (DC). . . . . 0A to 1.5A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
6. For θ_{JC}, the “case temp” location is taken at the package top center.
7. LX pin can withstand switching transients of -1.5V for 100ns, and 7V for 20ms.

Analog Specifications

VIN = PVIN = EN = 3.6V, VOUT = 5V, L1 = 1µH, C1 = 22µF, C2 = 2 x 22µF, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 4.8V).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SUPPLY						
VIN	Input Voltage Range		**1.8**		**4.8**	V
V_{UVLO}	VIN Undervoltage Lockout Threshold	Rising		1.725	**1.775**	V
		Falling	**1.550**	1.650		V
I_{VIN}	VIN Supply Current	PFM mode, no external load on VOUT (Note 9)		27.5	**60**	µA
I_{SD}	VIN Supply Current, Shutdown	EN = GND, VIN = 3.6V		0.4	**1.0**	µA
OUTPUT VOLTAGE REGULATION						
	Output Voltage Accuracy	I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
V_{FB}	FB Pin Voltage Regulation	For adjustable output version (ISL91117IIAZ)	**0.788**	0.80	**0.812**	V
I_{FB}	FB Pin Bias Current	For adjustable output version (ISL91117IIAZ)			**0.2**	µA
ΔVOUT/ ΔVIN	Line Regulation, PWM Mode	I_{OUT} = 500mA, MODE = GND, VIN step from 2.3V to 4.8V		±0.005		mV/mV
ΔVOUT/ ΔI_{OUT}	Load Regulation, PWM Mode	VIN = 3.7V, MODE = GND, IOUT step from 0mA to 500mA		±0.005		mV/mA
ΔVOUT/ ΔVIN	Line Regulation, PFM Mode	I_{OUT} = 100mA, MODE = VIN, VIN step from 2.3V to 4.8V		±12.5		mV/V
ΔVOUT/ ΔI_{OUT}	Load Regulation, PFM Mode	VIN = 3.7V, MODE = VIN, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
V_{CLAMP}	Output Voltage Clamp	Rising	**5.25**		**5.95**	V
	Output Voltage Clamp Hysteresis			400		mV
DC/DC SWITCHING SPECIFICATIONS						
f_{SW}	Oscillator Frequency		**2.4**	2.6	**2.9**	MHz
t_{ONMIN}	Minimum On Time			80		ns
$I_{NFETLEAK}$	LX Pin Leakage Current		**-0.5**		**+0.5**	µA

Analog Specifications VIN = PVIN = EN = 3.6V, VOUT = 5V, L1 = 1µH, C1 = 22µF, C2 = 2 x 22µF, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 4.8V). (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SOFT-START and SOFT DISCHARGE						
t_{SS}	Soft-start Time	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value. VIN = 2V, I_{OUT} = 200mA		2		ms
R_{DISCHG}	VOUT Soft-Discharge ON-Resistance	EN < VIL		120		Ω
POWER MOSFET						
R_{DSON_P}	P-Channel MOSFET ON-Resistance	I_{OUT} = 200mA		90		mΩ
R_{DSON_N}	N-Channel MOSFET ON-Resistance	I_{OUT} = 200mA		75		mΩ
I_{PK_LMT}	P-Channel MOSFET Peak Current Limit		**3.7**	4.2	**4.7**	A
PFM/PWM TRANSITION						
	Load Current Threshold, PFM to PWM			200		mA
	Load Current Threshold, PWM to PFM			75		mA
	External Synchronization Frequency Range		**2.75**		**3.25**	MHz
	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			35		°C
LOGIC INPUTS						
I_{LEAK}	Input Leakage			0.03	**0.5**	µA
V_{IH}	Input HIGH Voltage		**1.4**			V
V_{IL}	Input LOW Voltage				**0.4**	V

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

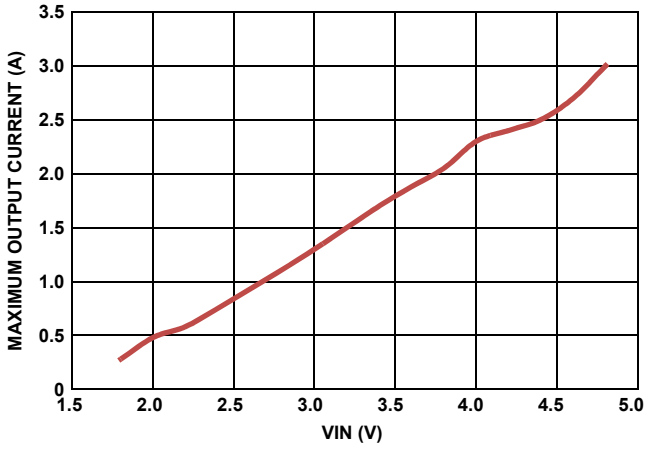


FIGURE 3. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE (V_{OUT} = 5V)

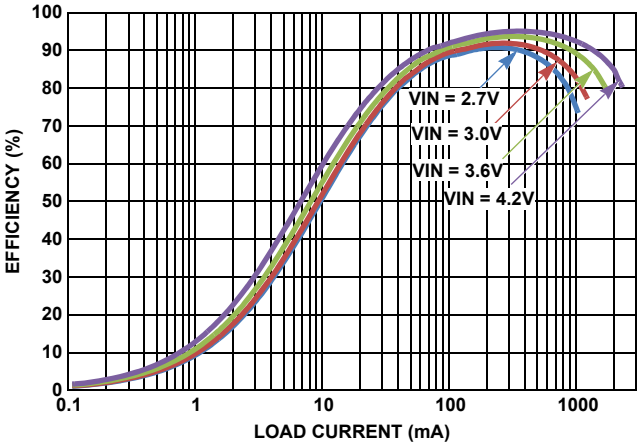


FIGURE 4. EFFICIENCY vs LOAD CURRENT (VOUT = 5V, MODE = LOW, T_A = +25°C)

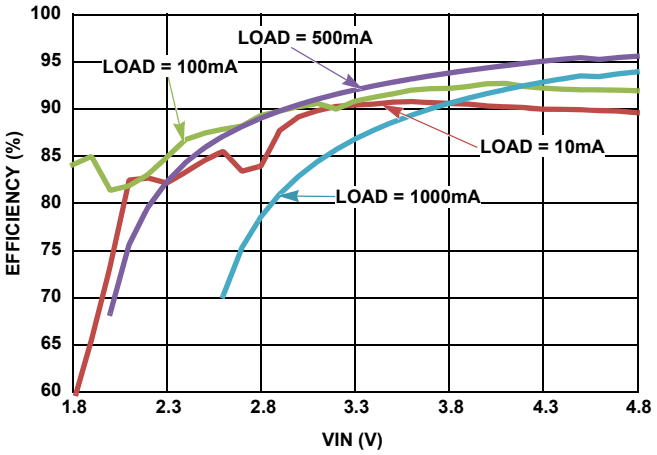


FIGURE 5. EFFICIENCY vs INPUT VOLTAGE (MODE = HIGH, T_A = +25°C)

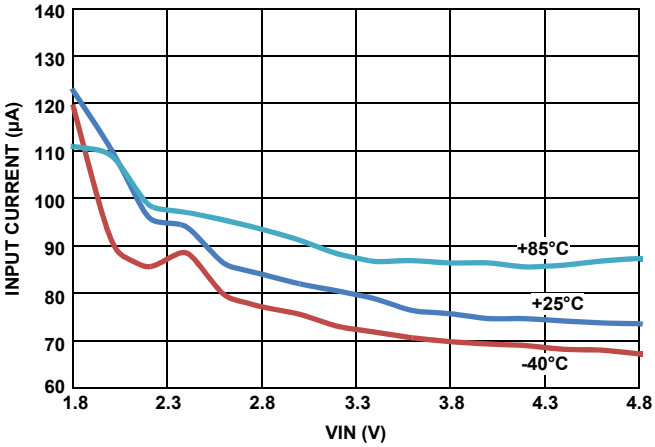


FIGURE 6. INPUT CURRENT vs INPUT VOLTAGE (MODE = HIGH)

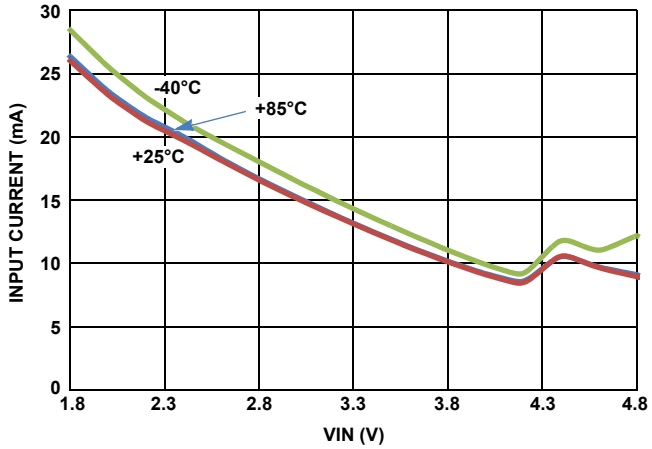


FIGURE 7. INPUT CURRENT vs INPUT VOLTAGE (MODE = LOW)

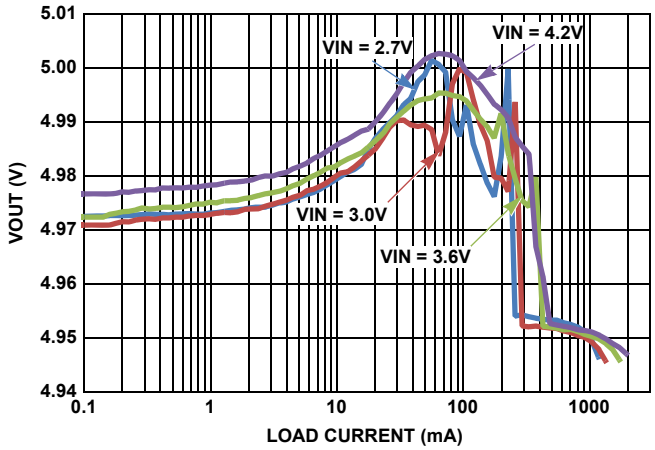


FIGURE 8. OUTPUT VOLTAGE vs LOAD CURRENT (MODE = HIGH, T_A = +25°C)

Typical Performance Curves (Continued)

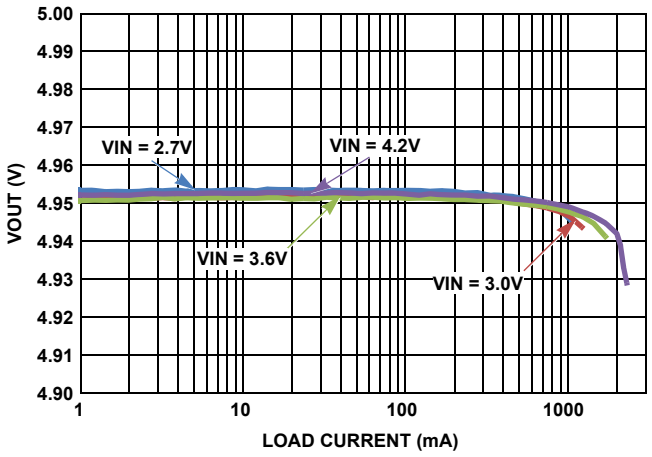


FIGURE 9. OUTPUT VOLTAGE vs LOAD CURRENT (MODE = LOW, T_A = +25°C)

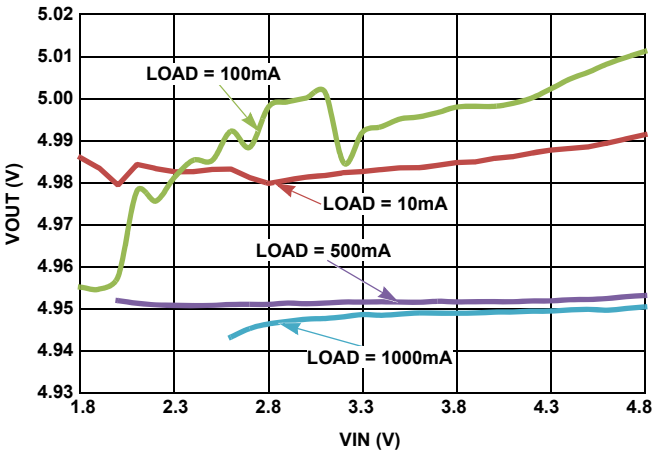


FIGURE 10. OUTPUT VOLTAGE vs INPUT VOLTAGE (MODE = HIGH, TA = +25°C)

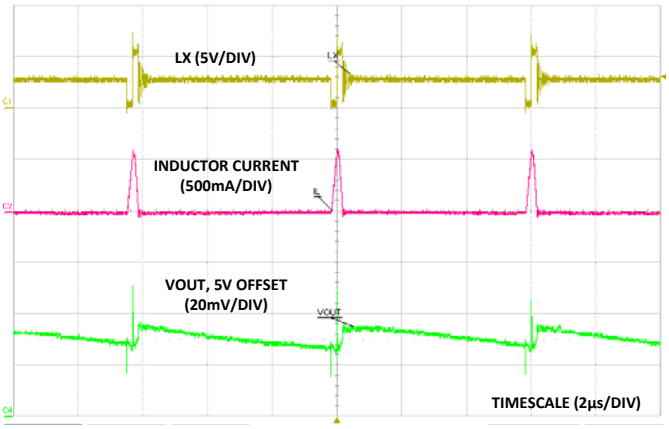


FIGURE 11. PFM MODE OPERATION (VIN = 3.6V, VOUT = 5V, 10mA LOAD)

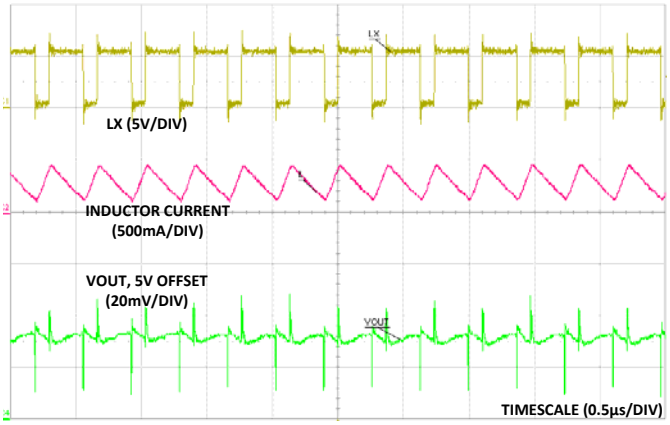


FIGURE 12. PWM MODE OPERATION (VIN = 3.6V, VOUT = 5V, 200mA LOAD)

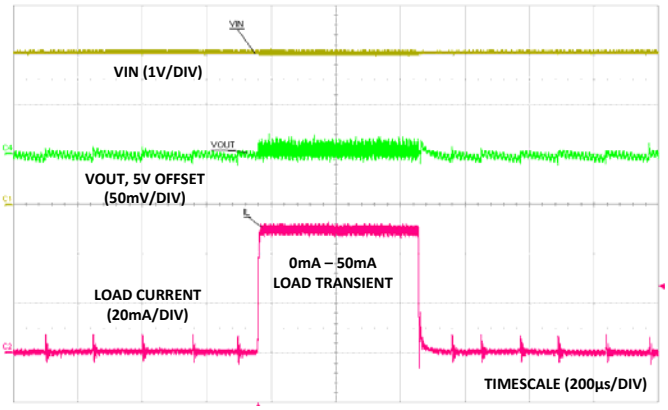


FIGURE 13. LOAD TRANSIENT (VIN = 3.0V, VOUT = 5V)

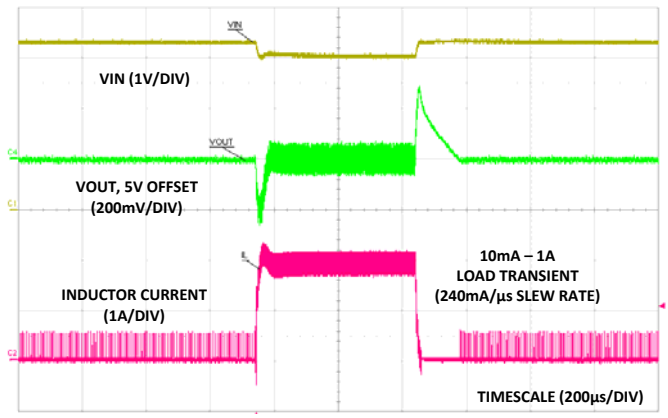


FIGURE 14. LOAD TRANSIENT (VIN = 3.0V, VOUT = 5V)

Typical Performance Curves (Continued)

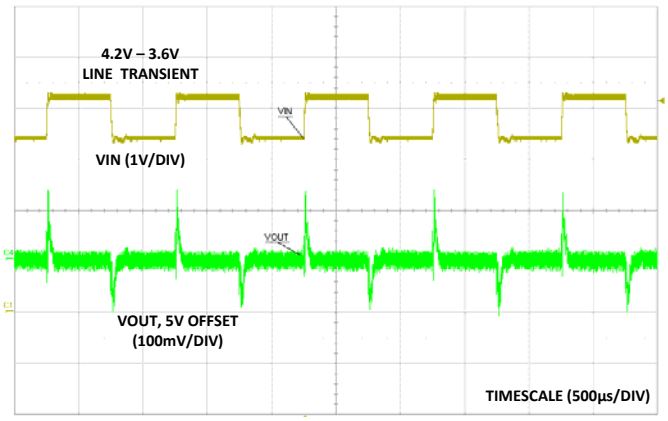


FIGURE 15. LINE TRANSIENT (VOUT = 5V)

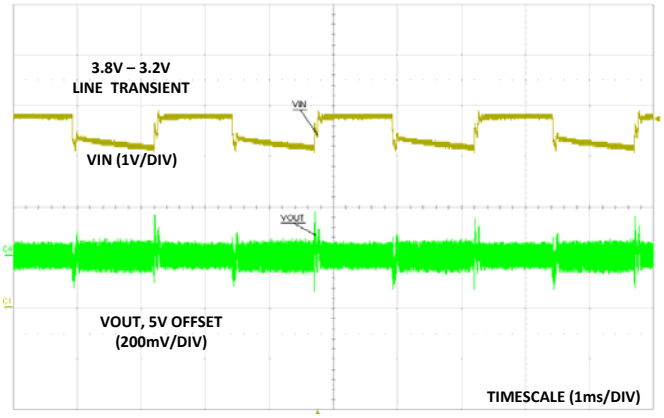


FIGURE 16. LINE TRANSIENT (VOUT = 5V)

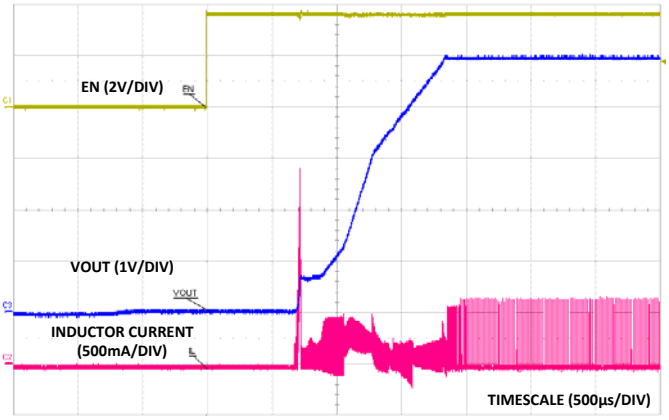


FIGURE 17. START-UP WITH NO LOAD (VIN = 3.6V, VOUT = 5V)

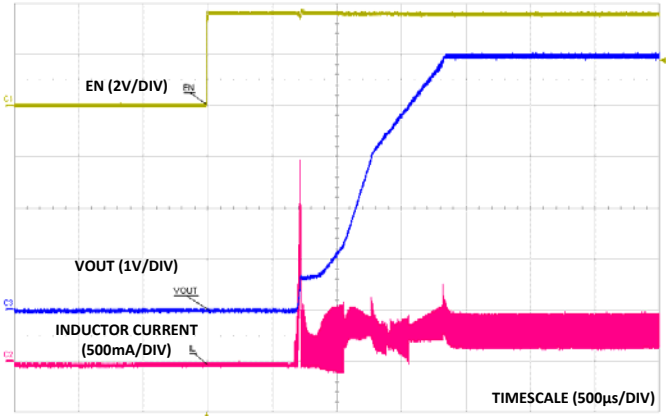


FIGURE 18. START-UP WITH 25Ω (VIN = 3.6V, VOUT = 5V)

Functional Description

Functional Overview

Refer to the “Block Diagram” on page 2. The ISL91117 implements a complete boost switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs.

Internal Supply and References

Referring to the “Block Diagram” on page 2, the ISL91117 provides two power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides the operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin EN allows the device to be enabled. Driving the EN pin LOW invokes a power-down mode, where most internal device functions, including input and output power-good detection, are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and GND is activated. This internal resistor has typical 120Ω resistance.

POR Sequence and Soft-start

Bringing the EN pin HIGH allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up, and stabilizes. The device then starts operating. There is a typical 1ms delay between assertion of the EN pin and the start of switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input in-rush currents. During soft-start, the reference voltage is ramped up to provide a ramping VOUT voltage. While the output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input in-rush current spikes. Once the output voltage exceeds that threshold, switching frequency is increased to its nominal value.

The soft-start time is typically 3ms. Increasing the load current will increase these typical soft-start times.

Short Circuit Protection

The ISL91117 provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-Channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the VIN voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91117 if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +125°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL91117 will execute its soft-start sequence.

External Synchronization

An external sync feature is provided. Applying a clock signal with a frequency between 2.75MHz and 3.25MHz at the MODE input, forces the ISL91117 to synchronize to this external clock. The MODE input supports standard logic levels.

PWM Operation

The control scheme of the device is based on the peak current mode control, and the control loop is compensated internally. The peak current of the N-channel MOSFET switch is sensed to limit the maximum current flowing through the switch and the inductor.

The control circuit includes ramp generator, slope compensator, error amplifier, PWM comparator (see “Block Diagram” on page 2). The ramp signal is derived from the inductor current. This ramp signal is then compared to the error amplifier output to generate the PWM gating signals for driving both N-channel and P-channel MOSFETs. The PWM operation is initialized by the clock from the internal oscillator (typical 2.6MHz). The N-channel MOSFET is turned ON at the beginning of a PWM cycle, the P-channel MOSFET remains OFF, and the current starts ramping up. When the sum of the ramp and the slope compensator output reaches the error amplifier output voltage, the PWM comparator outputs a signal to turn OFF the N-channel MOSFET. Here, both MOSFETs remain OFF during the dead-time interval, and then the P-channel MOSFET is turned ON and remains ON until the end of this PWM cycle. During this time, the inductor current ramps down until the next clock. At this point, following a short dead time, the N-channel MOSFET is again turned ON, repeating as previously described.

PFM Operation

The boost converter enters the PFM mode of operation under light load conditions. When the inductor current is sensed to cross zero, the converter enters PFM mode. In this mode, each pulse cycle is still synchronized by the PWM clock. The N-channel MOSFET is turned ON at the rising edge of the clock and turned OFF when the inductor peak current reaches a certain current limit. Then the P-channel MOSFET is turned ON, and it stays ON until the inductor current goes to zero. Subsequently, both N-channel and P-channel MOSFETs are turned OFF until the next clock cycle starts, at which time the N-channel MOSFET is turned ON again.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. In addition to the inductor current limit for PFM operation, the PFM pulses are also controlled by output voltage. These pulses continue until VOUT

has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until VOUT decays to the lower threshold of the hysteretic PFM controller.

Applications Information

Component Selection

The fixed-output version of the ISL91117 requires only three external power components to implement the boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable ISL91117 versions require three additional components to program the output voltage. Two external resistors program the output voltage, and a small capacitor is added to improve stability and response.

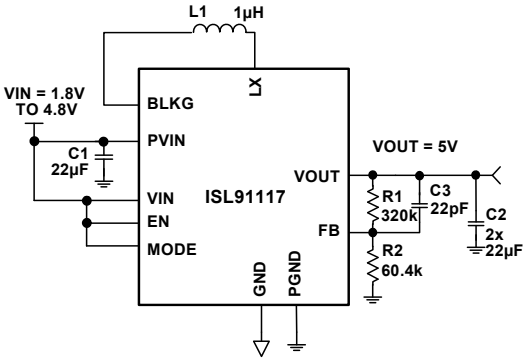


FIGURE 19. TYPICAL ISL91117IIAZ APPLICATION

Output Voltage Programming, Adjustable Version

Setting and controlling the output voltage of the ISL91117IIAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R1 and R2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R1 and R2 should be positioned close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor (C3 in Figure 19) in parallel with resistor R1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 22pF for R1 = 320kΩ. An NPO type capacitor is recommended.

Non-Adjustable Version FB Pin Connection

The fixed output version of the ISL91117 does not require external resistors or a capacitor on the FB pin. Simply connect VOUT to FB, as shown in Figure 20.

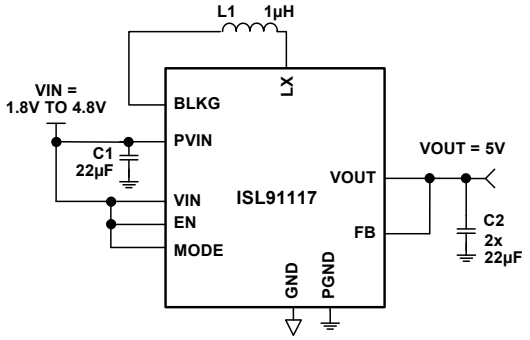


FIGURE 20. TYPICAL ISL91117II7Z APPLICATION

Inductor Selection

An inductor with high frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
Coilcraft	XFL4020-102ME	www.coilcraft.com
Murata	LQH5BPN1R0NT0	www.murata.com

PVIN and VOUT Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 22µF. The recommended VOUT capacitor value is 2x22µF or 47µF.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91117. The input and output capacitors should be positioned as closely to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible, and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

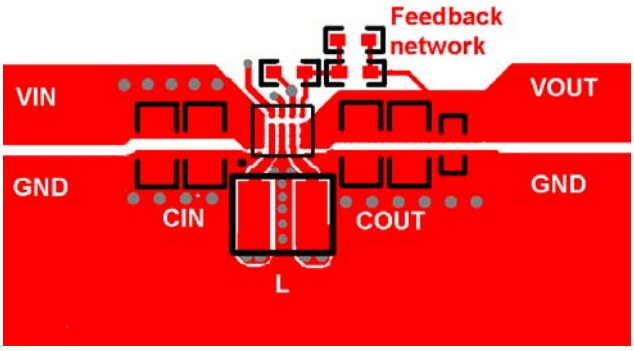


FIGURE 21. RECOMMENDED LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 7, 2014	FN8569.3	Updated Related Literature. Figure 18 on page 8 Title changed from START-UP WITH NO LOAD (VIN = 3.6V, VOUT = 5V) to START-UP WITH 25Ω (VIN = 3.6V, VOUT = 5V).
February 4, 2014	FN8569.2	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

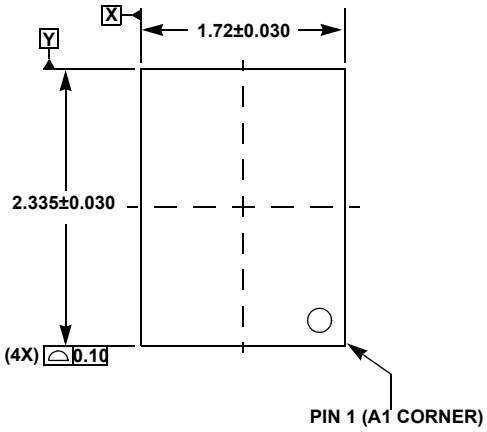
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

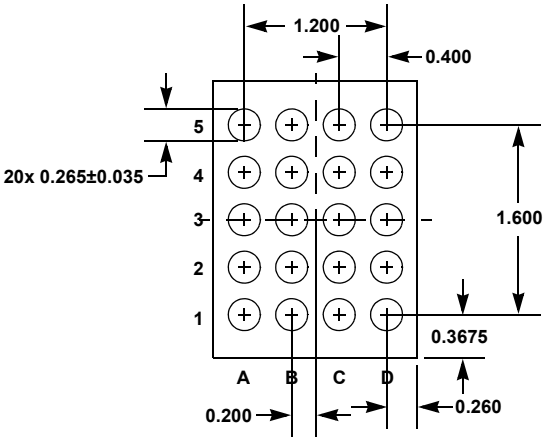
W4x5.20F

20 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm PITCH)

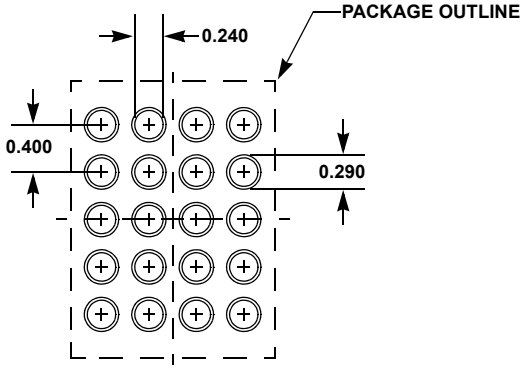
Rev 0, 5/13



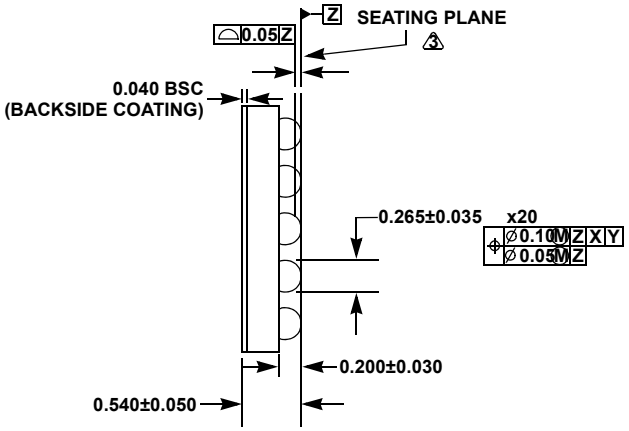
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z .
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.