

COMPLIANCE

TO-92



Pin Definition:

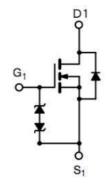
- 1. Source 2. Gate
- 2. Gale 3. Drain



PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (mA)	
60	5 @ V _{GS} = 10V	100	
	5.5 @ V _{GS} =5V	100	

Block Diagram



N-Channel MOSFET

ESD Protection

Features

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High Speed Switching

Low On-Resistance

Low Voltage Drive

Ordering Information

Part No.	Package	Packing
TSM2N7000KCT B0	TO-92	1Kpcs / Bulk
TSM2N7000KCT A3	TO-92	2Kpcs / Ammo

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	±20	V	
Drain Current	Continuous @ T _A =25°C	I _D	300		
	Pulsed	I _{DM}	700	mA	
Drain Reverse Current	Continuous @ T _A =25°C	I _{DR}	300	mA	
	Pulsed	I _{DMR}	700		
Maximum Power Dissipation		P _D	400	mW	
Operating Junction Temperature		TJ	+150	°C	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	TL	10	S
Junction to Ambient Thermal Resistance (PCB mounted)	RƏ _{JA}	357	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t \leq 5 sec.



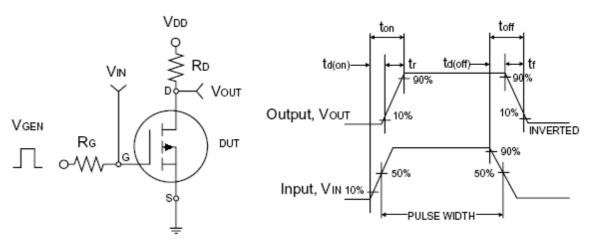
Electrical Specifications (Ta = 25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 10\mu A$	BV _{DSS}	60			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	1.0		2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±10	uA
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I _{DSS}			1.0	uA
	V _{GS} = 10V, I _D = 100mA		3	5		
Drain-Source On-State Resistance	$V_{GS} = 5V, I_{D} = 100mA$	R _{DS(ON)}		3.6	5.5	Ω
Forward Transconductance	$V_{DS} = 10V, I_{D} = 200mA$	g _{fs}	100			mS
Diode Forward Voltage	$I_{S} = 300 \text{mA}, V_{GS} = 0 \text{V}$	V _{SD}		0.9	1.2	V
Dynamic ^b	·					
Total Gate Charge	$V_{DS} = 10V, I_D = 250mA,$ $V_{GS} = 4.5V$	Q _g		0.4		nC
Input Capacitance		C _{iss}		7.32		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	C _{oss}		3.42		pF
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		7.63		
Switching ^c		1			1	
Turn-On Delay Time	$V_{DD} = 30V, R_{G} = 10\Omega$	t _{d(on)}		25		
Turn-Off Delay Time	$I_{\rm D} = 100 {\rm mA}, V_{\rm GEN} = 10 {\rm V},$	t _{d(off)}		35		nS

Notes:

a. pulse test: PW ≤300µS, duty cycle ≤2% b. For DESIGN AID ONLY, not subject to production testing.

b. Switching time is essentially independent of operating temperature.

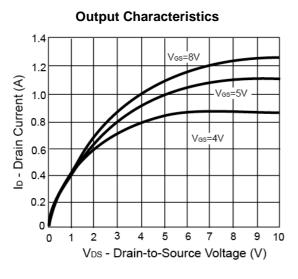


Switching Test Circuit

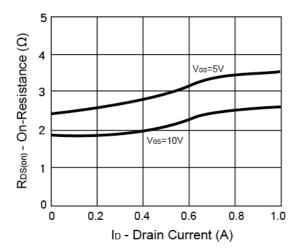
Switchin Waveforms



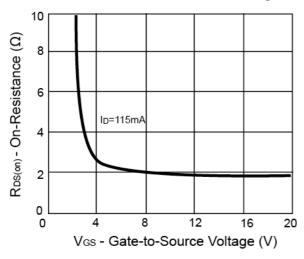
Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

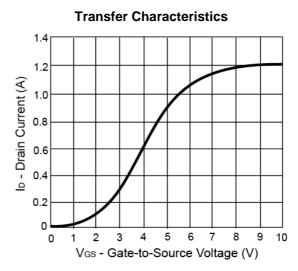


On-Resistance vs. Drain Current

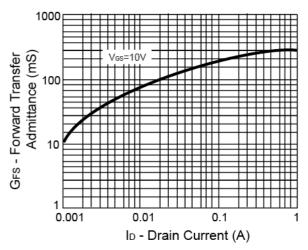


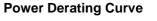
On-Resistance vs. Gate-Source Voltage

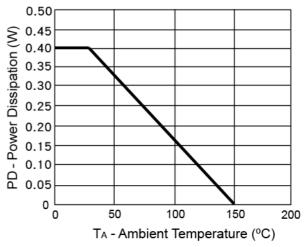




Forward Transfer Admittance vs. Drain Current

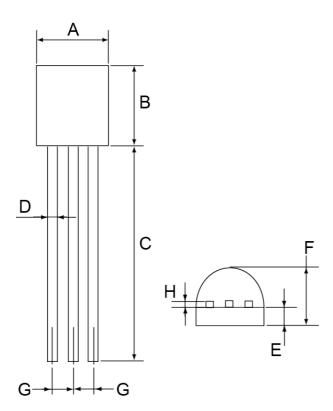








TO-92 Mechanical Drawing



TO-92 DIMENSION					
	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
А	4.30	4.70	0.169	0.185	
В	4.30	4.70	0.169	0.185	
С	13.53 (typ)		0.532 (typ)		
D	0.39	0.49	0.015	0.019	
E	1.18	1.28	0.046	0.050	
F	3.30	3.70	0.130	0.146	
G	1.27	1.31	0.050	0.051	
Н	0.33	0.43	0.013	0.017	

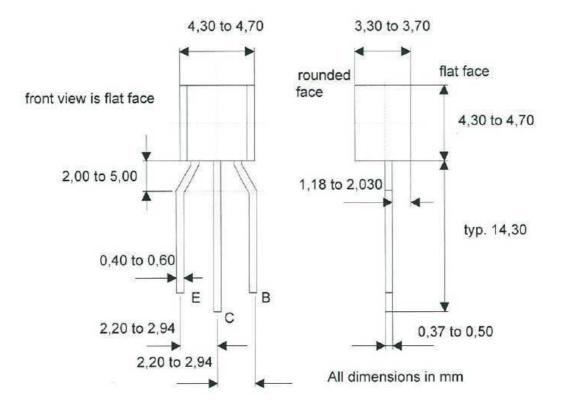
Marking Diagram



- Y = Year Code
- M = Month Code
 - (A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L = Lot Code







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