

## MAX8973A

## 9A, Three-Phase Step-Down Switching Regulator

### General Description

The MAX8973A high-efficiency, three-phase, DC-DC step-down switching regulator delivers up to 9A of output current in a compact footprint with excellent transient response. Each phase operates at a 2MHz fixed frequency, allowing the use of small magnetic components. Maxim Integrated's proprietary Rotational Phase Spreading algorithm optimizes efficiency at low output currents. Software-selectable forced-PWM mode allows either fixed-frequency operation, or improved efficiency at light load with a variable frequency in skip mode. The triple-inductor architecture reduces the size of the external components while providing the benefit of ripple current cancellation. The MAX8973A operates from a 2.6V to 4.5V input voltage range.

An I<sup>2</sup>C 3.0-compatible serial interface, supporting clock rates up to 3.4MHz, controls key regulator parameters such as output voltage, output slew rate, and on/off control. Output voltage is programmable from 0.60625V to 1.4V in 6.25mV increments. The default output voltage is factory programmable. An EN input enables and disables the output, while a DVS pin selects two different output voltages without relying on the serial interface.

Fully differential remote sense ensures precise DC regulation at the point of load. Total output error is less than 0.8% over, line, and temperature at 1.2V output. Output ripple is typically < 1% of the output voltage setting when the processor is in the Idle state (light loads) and < 0.5% at medium and high loads.

Other features include internal soft-start control circuitry to reduce inrush current, guaranteed monotonic voltage adjustment, over-current protection, and over-temperature protection. The MAX8973A operates over the -40°C to +85°C extended temperature range and is packaged in an ultra-small WLP package.

### Features

- Up to 9A Output Current
- > 91% Peak Efficiency at 3.6V<sub>IN</sub>, 1.2V<sub>OUT</sub>
- Rotational Phase Spreading Maximizes Efficiency at Light Loads
- Initial Accuracy of 0.5% at 1.2V Output
- 0.8% Output Accuracy Over Line and Temperature at 1.2V Output
- Enhanced Transient Response Minimizes Output Droop with Large Load Steps
- Soft-Stop Recovers Output Capacitor Charge When Converter is Disabled
- Programmable V<sub>OUT</sub>: 0.60625V to 1.4V (6.25mV step size)
- Powers Up into Prebiased Output
- 3.4MHz I<sup>2</sup>C 3.0-Compatible Serial Interface
- Fixed 2MHz PWM Switching Frequency per Phase
- Small (< 1μH) Inductor for Each Phase
- Overcurrent, Short-Circuit, and Thermal Protection

### Applications

- Smartphones
- Tablets
- Ultrabooks

***Ordering Information and Typical Operating Circuit appear at end of data sheet.***

For related parts and recommended products to use with this part, refer to [www.maximintegrated.com/MAX8973.related](http://www.maximintegrated.com/MAX8973.related).

---

**TABLE OF CONTENTS**


---

General Description . . . . .	1
Features . . . . .	1
Applications . . . . .	1
Absolute Maximum Ratings . . . . .	5
Package Thermal Characteristics . . . . .	5
Electrical Characteristics . . . . .	5
Typical Operating Characteristics . . . . .	18
Pin Configuration . . . . .	25
Pin Description . . . . .	25
Detailed Description . . . . .	27
Enabling the Regulator . . . . .	29
Startup Delay (BIASEN) . . . . .	29
Startup Ramp Rate . . . . .	29
Disabling the Regulator (Active Discharge) . . . . .	29
Soft-Stop (Active Energy Recovery) . . . . .	30
Resistive Discharge . . . . .	30
Setting the Output Voltage . . . . .	30
DVS . . . . .	30
Default Power-Up Voltage . . . . .	30
Slew Rate Control . . . . .	31
Control Scheme . . . . .	31
Modes of Operation (Skip, Mid, CCM) . . . . .	31
Modes of Operation (FPWM) . . . . .	31
Current Sensing . . . . .	31
Maximum Output Current . . . . .	32
Overload and Short Circuit Protection . . . . .	32
Enhanced Transient Response (ETR) . . . . .	32
Remote Sense . . . . .	32
Thermal Protection . . . . .	32
I <sup>2</sup> C Interface . . . . .	32
I <sup>2</sup> C Interface Features . . . . .	32
I <sup>2</sup> C System Configuration . . . . .	33
I <sup>2</sup> C Interface Power . . . . .	33
I <sup>2</sup> C Data Transfer . . . . .	33
I <sup>2</sup> C Start and Stop Conditions . . . . .	33
I <sup>2</sup> C Acknowledge Bit . . . . .	33
I <sup>2</sup> C Slave Address . . . . .	34
I <sup>2</sup> C Clock Stretching . . . . .	34

**TABLE OF CONTENTS (continued)**

I2C General Call Address .....	34
I2C Communication Speed .....	35
I2C Communication Protocols .....	35
Writing to a Single Register .....	35
Writing to Sequential Registers .....	36
Writing Multiple Bytes Using Register-Data Pairs .....	38
Reading from a Single Register .....	38
Reading from Sequential Registers .....	40
Engaging HS Mode for Operation up to 3.4MHz .....	41
I2C Watchdog Timer (WDTMR) .....	41
Component Selection .....	41
Input Capacitance .....	41
Output Capacitance .....	41
Inductors .....	42
Selection Guide .....	42
Registers .....	42
Register Map .....	42
Register Details .....	43
VOUT Register .....	43
VOUT_DVS Register .....	43
CONTROL1 Register .....	44
CONTROL2 Register .....	45
CHIPID1 Register .....	45
CHIPID2 Register .....	46
PCB Layout Guideline .....	46
Typical Operating Circuit .....	47
Ordering Information .....	48
Package Information .....	48
Chip Information .....	48
Revision History .....	49

---

**LIST OF FIGURES**


---

Figure 1. MAX8973_ Functional Block Diagram . . . . .	27
Figure 2. Typical Applications Circuit. . . . .	28
Figure 3. Soft-Start Discharge . . . . .	30
Figure 4. Rotational Phase Spreading Algorithm. . . . .	31
Figure 5. I <sup>2</sup> C Example System . . . . .	33
Figure 6. START and STOP Conditions . . . . .	33
Figure 7. I <sup>2</sup> C Acknowledge (A) and Not-Acknowledge (nA) . . . . .	34
Figure 8. Slave Address Byte Example . . . . .	34
Figure 9. Writing to a Single Register with the Write Byte Protocol . . . . .	36
Figure 10. Writing to Sequential Registers X to N. . . . .	37
Figure 11. Writing to Multiple Registers with the Multiple Byte Register Data Pair Protocol. . . . .	39
Figure 12. Reading from a Single Register with the Read Byte Protocol . . . . .	39
Figure 13. Reading Continuously from Sequential Registers X to N. . . . .	40
Figure 14. Engaging HS Mode. . . . .	41
Figure 15. MAX8973_ EVKIT Layout Recommendation . . . . .	47

---

**LIST OF TABLES**


---

Table 1. MAX8973A Enable Truth Table . . . . .	29
Table 2. BIASEN and Startup Delay Truth Table. . . . .	29
Table 3. MAX8973A Startup and DVS Ramp Rates . . . . .	29
Table 4. MAX8973A Output Discharge Selection Truth Table. . . . .	29
Table 5. MAX8973A Soft-Stop Slew Rate . . . . .	30
Table 6. Default Output Voltage Settings. . . . .	30
Table 7. DVS Response to Decrease in Target $V_{OUT}$ . . . . .	31
Table 8. MAX8973A Inductor Parameters . . . . .	31
Table 9. Enhanced Transient Response Settings . . . . .	32
Table 10. MAX8973_ I <sup>2</sup> C Slave Addresses. . . . .	34
Table 11. MAX8973_ Selection Guide . . . . .	42



**Absolute Maximum Ratings**

IN <sub>-</sub> , V <sub>CC</sub> , V <sub>DD</sub> to PG <sub>-</sub> .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C) 28-Bump WLP 0.4mm Pitch (derate 20.4mW/°C above +70°C) ..... 1.63W Operating Temperature Range..... -40°C to +85°C Junction Temperature..... +150°C Storage Temperature Range..... -65°C to +150°C Bump Temperature (soldering, reflow)..... +260°C
SDA, SCL to AGND.....	-0.3V to (V <sub>DD</sub> + 0.3V)	
LX <sub>-</sub> to PG <sub>-</sub> .....	-0.3V to (V <sub>IN<sub>-</sub></sub> + 0.3V)	
DVS, EN, BIASEN to AGND.....	-0.3V to (V <sub>CC</sub> + 0.3V)	
SNS+, OUT to AGND.....	-0.3V to (V <sub>CC</sub> + 0.3V)	
PG <sub>-</sub> , SNS- to AGND.....	-0.3V to +0.3V	
IN <sub>-</sub> to V <sub>CC</sub> .....	-0.3V to +0.3V	
RMS LX <sub>-</sub> Current (per bump).....	1.6A	

**Package Thermal Characteristics (Note 1)**

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) (Note 1).....	49°C/W	Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) (Note 1).....	10°C/W
---	--------	--	--------

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Electrical Characteristics**

(V<sub>IN<sub>-</sub></sub> = V<sub>CC</sub> = V<sub>EN</sub> = 3.6V, V<sub>AGND</sub> = V<sub>PG<sub>-</sub></sub> = V<sub>BIASEN</sub> = V<sub>DVS</sub> = 0V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT SUPPLIES</b>					
V <sub>CC</sub> and IN <sub>-</sub> Operating Range		2.6		4.5	V
V <sub>CC</sub> and IN <sub>-</sub> Undervoltage Lockout (UVLO) Threshold	V <sub>IN<sub>-</sub></sub> falling	2.45	2.5	2.55	V
V <sub>CC</sub> and IN <sub>-</sub> UVLO Hysteresis			200		mV
V <sub>CC</sub> and IN <sub>-</sub> Shutdown Supply Current	EN = 0	T <sub>A</sub> = +25°C	2	3	µA
		T <sub>A</sub> = +85°C	2.5		
V <sub>CC</sub> and IN <sub>-</sub> BIAS Enable Supply Current	EN = 0, BIASEN = 1, no switching		34	50	µA
V <sub>CC</sub> and IN <sub>-</sub> Operating Supply Current	FPWM_EN = 0, V <sub>OUT</sub> = 1.2V, no load, no switching, CKADV=11 (ETR disabled)		135	190	µA
	FPWM_EN = 0, V <sub>OUT</sub> = 1.2V, no load, no switching, CKADV = 00 (ETR enabled)		225	345	µA
	FPWM_EN = 1, V <sub>OUT</sub> = 1.2V, no load, f <sub>SW</sub> = 2MHz/phase, inductor losses included		25		mA
<b>LOGIC INTERFACE (DVS, EN, BIASEN)</b>					
Logic Input High Voltage (V <sub>IH</sub> )		1.4			V
Logic Input Low Voltage (V <sub>IL</sub> )				0.4	V
Input Leakage Current	ENPD_EN = 1	-1	0.001	+1	µA
EN Logic Input Pulldown Resistor	Controlled by serial interface command: ENPD_EN = 0	250	500	750	kΩ

**Electrical Characteristics (continued)**

( $V_{IN\_} = V_{CC} = V_{EN} = 3.6V$ ,  $V_{AGND} = V_{PG\_} = V_{BIASEN} = V_{DVS} = 0V$ ,  $V_{EN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C SERIAL INTERFACE</b>					
<b>SDA AND SCL I/O STAGES</b>					
SCL, SDA Input High Voltage ( $V_{IH}$ )	$V_{DD} = 1.8V$	$0.7 \times V_{DD}$			V
SCL, SDA Input High Voltage ( $V_{IL}$ )	$V_{DD} = 1.8V$	$0.3 \times V_{DD}$			V
SCL, SDA Input Hysteresis ( $V_{HYS}$ )		$0.2 \times V_{DD}$			V
SCL, SDA Input Current ( $I_I$ )		-10		+10	$\mu A$
SDA Output Low Voltage ( $V_{OL}$ )	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance ( $C_I$ )			10		pF
Output Fall Time from $V_{IH}$ to $V_{IL}$ ( $t_{OF}$ )				120	ns
SCL Watchdog Timer Period	WDTMR = 0 = OFF (default setting)		$\infty$		ms
	WDTMR = 1	24.5	35	45.5	
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST MODE, AND FAST MODE PLUS</b>					
Clock Frequency ( $f_{SCL}$ ) (Note 3)				1000	kHz
Hold Time (Repeated) START Condition ( $t_{HD;STA}$ ) (Note 3)		0.26			$\mu s$
CLK Low Period ( $t_{LOW}$ ) (Note 3)		0.5			$\mu s$
CLK High Period ( $t_{HIGH}$ ) (Note 3)		0.26			$\mu s$
Set-Up Time Repeated START Condition ( $t_{SU;STA}$ ) (Note 3)		0.26			$\mu s$
DATA Hold Time ( $t_{HD;DAT}$ ) (Note 3)		0			$\mu s$
DATA Setup Time ( $t_{SU;DAT}$ ) (Note 3)		50			ns
Setup Time for STOP Condition ( $t_{SU;STO}$ ) (Note 3)		0.26			$\mu s$
Bus Free Time Between STOP and START ( $t_{BUF}$ ) (Note 3)		0.5			$\mu s$
Capacitive Load for Each Bus Line ( $C_B$ ) (Note 3)				550	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter (Note 3)	Response Time of Comparators			50	ns
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING FOR HIGH-SPEED MODE</b>					
<b>C<sub>B</sub> = 100pF</b>					
Clock Frequency ( $f_{SCL}$ )				3.4	MHz
Setup Time Repeated START Condition ( $t_{SU;STA}$ )		160			ns
Hold Time Repeated START Condition ( $t_{HD;STA}$ )		160			ns

**Electrical Characteristics (continued)**

( $V_{IN\_} = V_{CC} = V_{EN} = 3.6V$ ,  $V_{AGND} = V_{PG\_} = V_{BIASEN} = V_{DVS} = 0V$ ,  $V_{EN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Low Period ( $t_{LOW}$ )		160			ns
Clock High Period ( $t_{HIGH}$ )		60			ns
Data Setup Time ( $t_{SU;DAT}$ )		10			ns
Data Hold Time ( $t_{HD;DAT}$ )		0		70	ns
Minimum SCL Rise Time ( $t_{RCL,MIN}$ )			10		ns
Maximum SCL Rise Time ( $t_{RCL,MAX}$ )			40		ns
Minimum Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit ( $t_{RCL1,MIN}$ )			10		ns
Maximum Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit ( $t_{RCL1,MAX}$ )			80		ns
Minimum SCL Fall Time ( $t_{FCL,MIN}$ )			10		ns
Maximum SCL Fall Time ( $t_{FCL,MAX}$ )			40		ns
Minimum SDA Rise Time ( $t_{RDA,MIN}$ )			10		ns
Maximum SDA Rise Time ( $t_{RDA,MAX}$ )			80		ns
Minimum SDA Fall Time ( $t_{FDA,MIN}$ )			10		ns
Maximum SDA Fall Time ( $t_{FDA,MAX}$ )			80		ns
Setup Time for STOP Condition ( $t_{SU;STO}$ )		160			ns
Capacitive Load for Each Bus Line ( $C_B$ ) (Note 3)				100	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter				10	ns
<b><math>C_B = 400pF</math></b>					
Clock Frequency ( $f_{SCL}$ ) (Note 3)				1.7	MHz
Setup Time Repeated START Condition ( $t_{SU;STA}$ ) (Note 3)		160			ns
Hold Time Repeated START Condition ( $t_{HD;STA}$ ) (Note 3)		160			ns
Clock Low Period ( $t_{LOW}$ ) (Note 3)		320			ns

**Electrical Characteristics (continued)**

( $V_{IN\_} = V_{CC} = V_{EN} = 3.6V$ ,  $V_{AGND} = V_{PG\_} = V_{BIASEN} = V_{DVS} = 0V$ ,  $V_{EN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock High Period ( $t_{HIGH}$ ) (Note 3)		120			ns
Data Setup Time ( $t_{SU,DAT}$ ) (Note 3)		10			ns
Data Hold Time ( $t_{HD,DAT}$ ) (Note 3)		0		150	ns
Minimum SCL Rise Time ( $t_{RCL,MIN}$ )			20		ns
Maximum SCL Rise Time ( $t_{RCL,MAX}$ )			80		ns
Minimum Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit ( $t_{RCL1,MIN}$ )			20		ns
Maximum Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit ( $t_{RCL1,MAX}$ )			160		ns
Minimum SCL Fall Time ( $t_{FCL,MIN}$ )			20		ns
Maximum SCL Fall Time ( $t_{FCL,MAX}$ )			80		ns
Minimum SDA Rise Time ( $t_{RDA,MIN}$ )			20		ns
Maximum SDA Rise Time ( $t_{RDA,MAX}$ )			160		ns
Minimum SDA Fall Time ( $t_{FDA,MIN}$ )			20		ns
Maximum SDA Fall Time ( $t_{FDA,MAX}$ )			160		ns
Setup Time for STOP Condition ( $t_{SU,STO}$ ) (Note 3)		160			ns
Capacitive Load for Each Bus Line ( $C_B$ ) (Note 3)				400	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter (Note 3)				10	ns
<b>STEP-DOWN CONVERTER</b>					
Minimum Output Capacitance Required for Stability (Note 3)	Actual output capacitance, sum of all 3 phases $V_{OUT} = 0.60625V$ to $1.4V$ $I_{OUT} = 0$ to $9A$			24.5	$\mu F$
OUT Voltage Range	6.25mV steps, 7 bits, monotonic	0.60625		1.4	V

## Electrical Characteristics (continued)

( $V_{IN\_} = V_{CC} = V_{EN} = 3.6V$ ,  $V_{AGND} = V_{PG\_} = V_{BIASEN} = V_{DVS} = 0V$ ,  $V_{EN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUT Voltage Accuracy	No load, $V_{CC} = V_{IN\_} = 2.6V$ to $4.5V$ , $V_{OUT} = 1.2V$ , FPWM_EN = 1	$T_A = +25^{\circ}C$	-0.5		+0.5	%
	No load, $V_{CC} = V_{IN\_} = 2.6V$ to $4.5V$ , $V_{OUT} = 1.2V$ , FPWM_EN = 1	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	-0.8		+0.8	
	No load, $V_{CC} = V_{IN\_} = 2.6V$ to $4.5V$ , $V_{OUT} = 0.60625V$ , FPWM_EN = 1	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	-1.5		+1.5	
	No load, $V_{CC} = V_{IN\_} = 2.6V$ to $4.5V$ , $V_{OUT} = 1.4V$ , FPWM_EN = 1	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	-1.25		+1.25	
Load Regulation				-0.001		V/A
Output Voltage Slew Rate	RAMP[1:0] = 11		200		mV/ $\mu$ s	
	RAMP[1:0] = 10		50			
	RAMP[1:0] = 01		25			
	RAMP[1:0] = 00		12.5			
Peak Current Limit	Each phase	MAX8973A	3.72	4	4.28	A
NMOS Current Limit	Each phase, valley current after PMOS current limit and $V_{OUT} < 75%$ of target		55% of $I_{LIM}$ setting			A
Negative Current Limit	FPWM_EN = 1 or ramping down output voltage, each phase		-1.33			A
n-Channel MOSFET Zero-Crossing Threshold			50			mA
Switching Frequency per Phase	FPWM_EN = 1		1.9	2	2.1	MHz
Soft-Start Delay	BIASEN = 0, From EN rising to $V_{OUT}$ at 10%		240			$\mu$ s
	BIASEN = 1, From EN rising to $V_{OUT}$ at 10%		20			$\mu$ s

**Electrical Characteristics (continued)**

( $V_{IN\_} = V_{CC} = V_{EN} = 3.6V$ ,  $V_{AGND} = V_{PG\_} = V_{BIASEN} = V_{DVS} = 0V$ ,  $V_{EN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

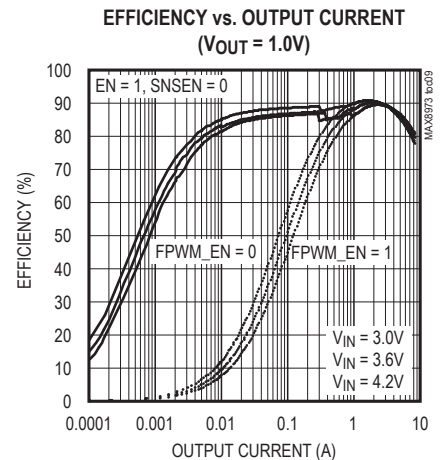
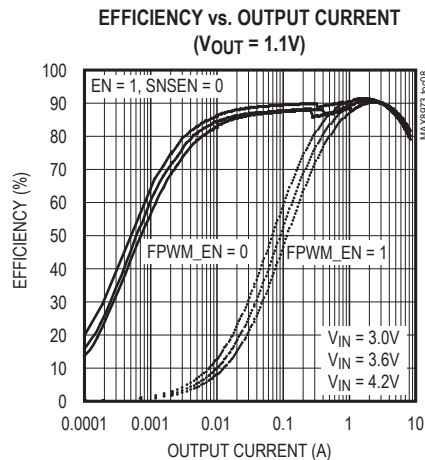
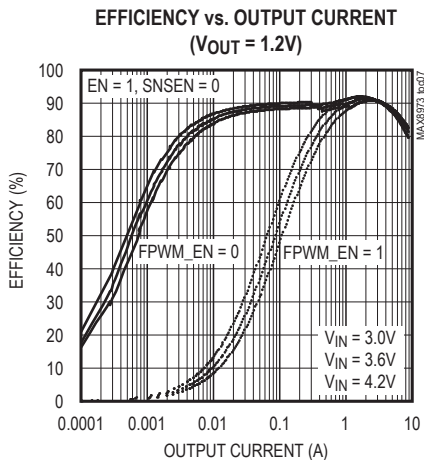
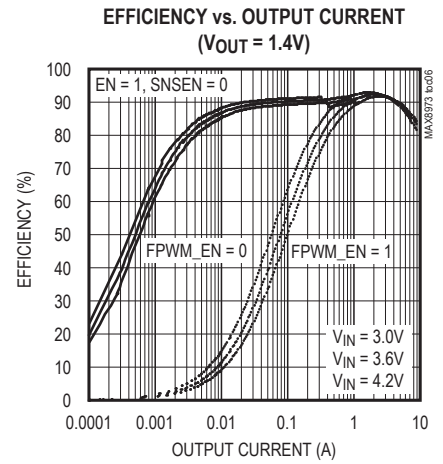
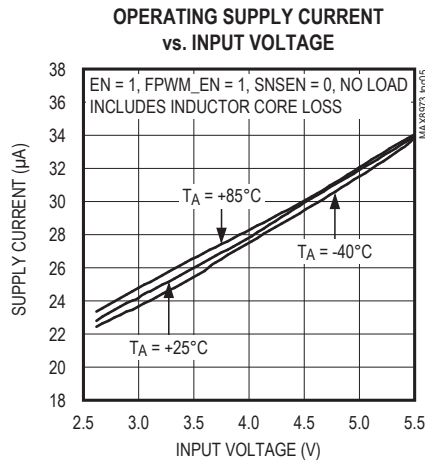
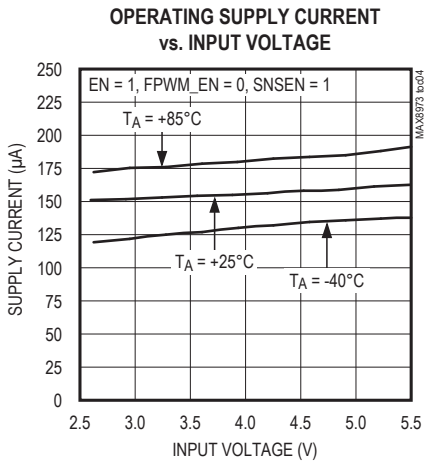
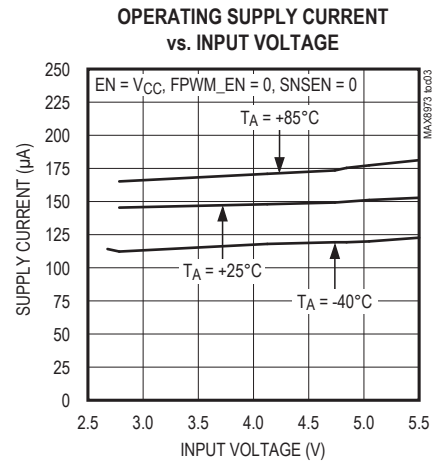
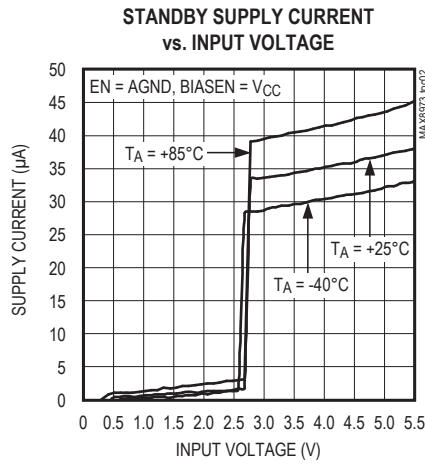
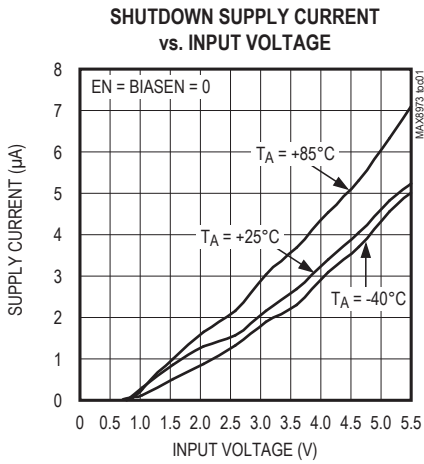
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Soft-Start Ramp Time	From $V_{OUT} = 10\%$ to $90\%$ , RAMP[1:0] = 0b11 200mV/ $\mu$ s slew rate, $V_{OUT}$ set to 1V		4		$\mu$ s	
	From $V_{OUT} = 10\%$ to $90\%$ , RAMP[1:0] = 0b10, 0b01, or 0b00 20mV/ $\mu$ s slew rate, $V_{OUT}$ set to 1V		40			
LX p-Channel MOSFET On-Resistance	Each phase, $I_{N\_}$ to $LX\_$ , $I_{LX\_} = -200mA$		50	90	m $\Omega$	
LX n-Channel MOSFET On-Resistance	Each phase, FPWM_EN = 0, $LX\_$ to PGND, $I_{LX\_} = 200mA$		25	45	m $\Omega$	
LX Leakage	$V_{LX\_} = 5.5V$ or $0V$	$T_A = +25^{\circ}C$	-1	+0.03	+1	$\mu$ A
		$T_A = +85^{\circ}C$		0.25		
OUT Discharge Resistance	During shutdown from OUT to AGND		100		$\Omega$	
SNS+ Input Impedance			340		k $\Omega$	
SNS- Input Impedance			280		k $\Omega$	
Remote Sense Compensation Range	From OUT to SNS+			100	mV	
	From GND to SNS-			-100	mV	
OUT Input Impedance			53		k $\Omega$	
<b>THERMAL PROTECTION</b>						
Thermal Shutdown Threshold			160		$^{\circ}C$	
Thermal Shutdown Threshold Hysteresis			20		$^{\circ}C$	

**Note 2:** 100% production tested at  $T_A = +25^{\circ}C$ , limits over the operating range are guaranteed by design.

**Note 3:** Guaranteed by design, not production tested.

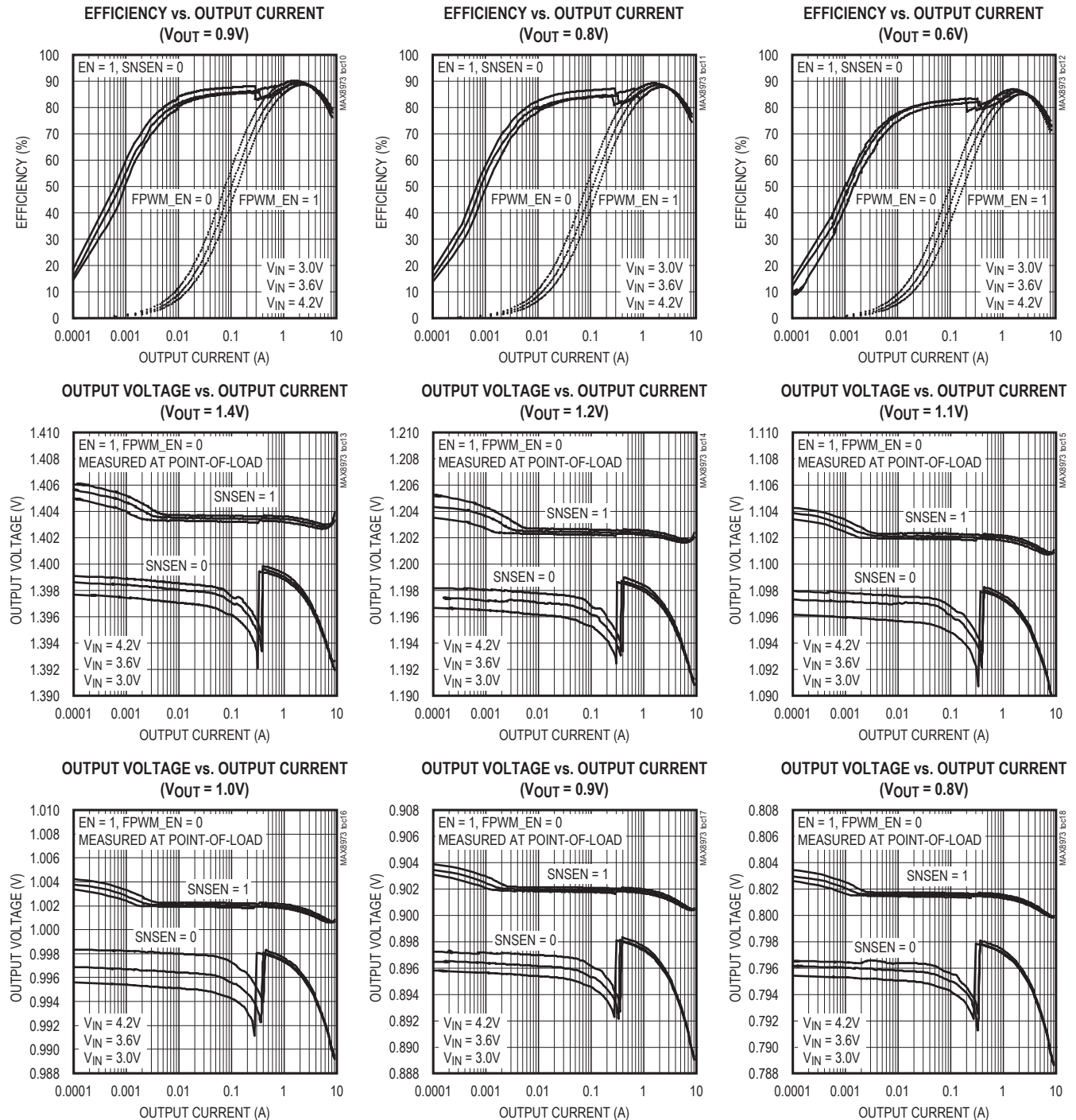
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4](#).)



Typical Operating Characteristics (continued)

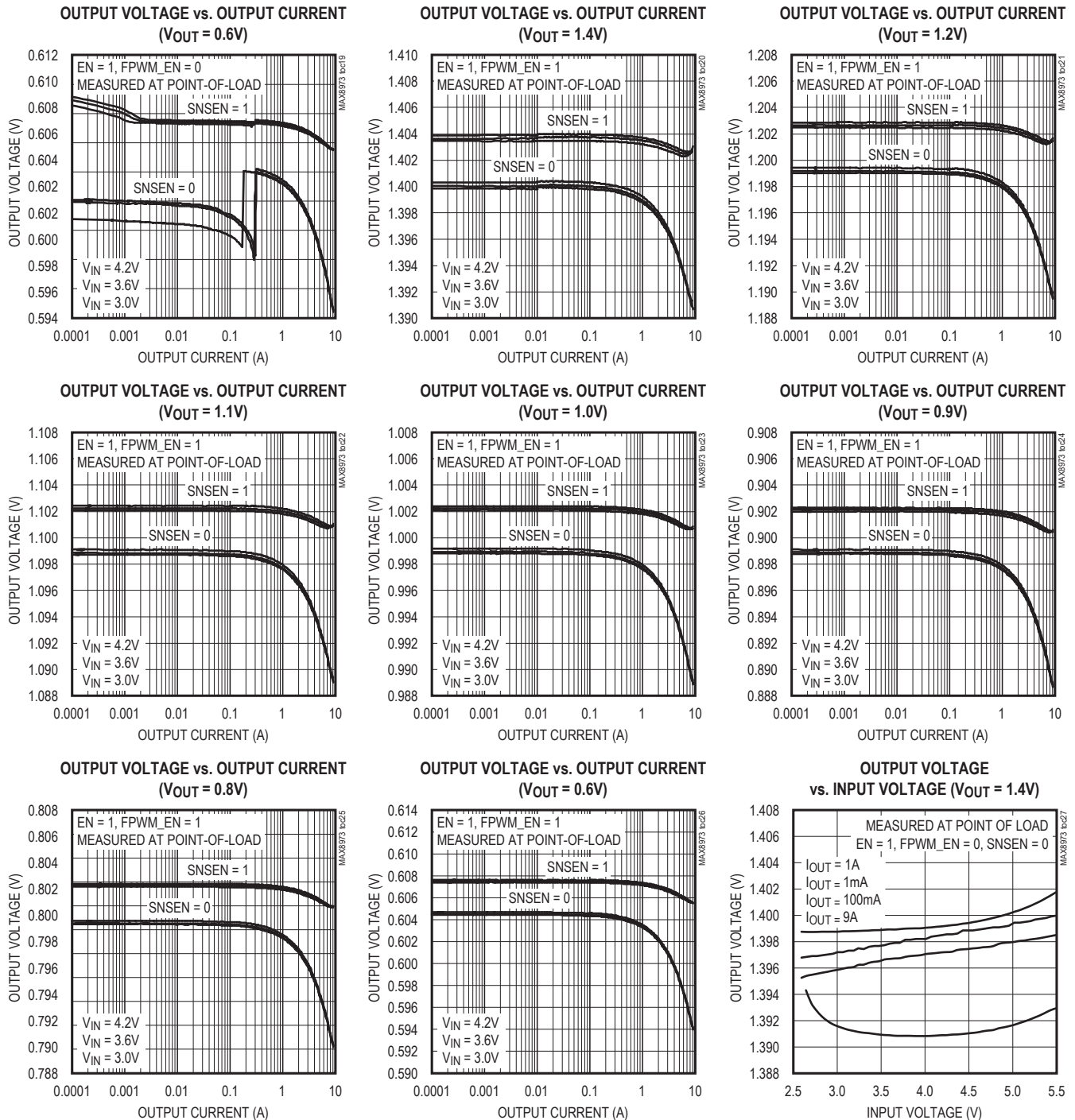
( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)





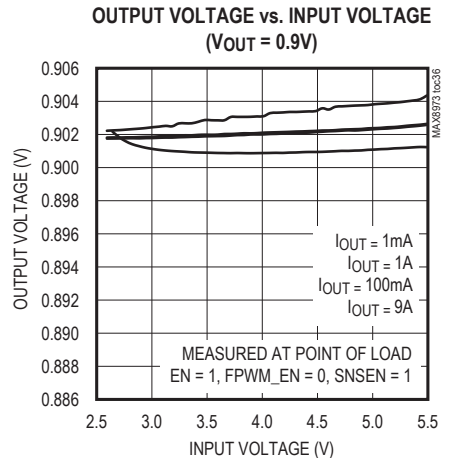
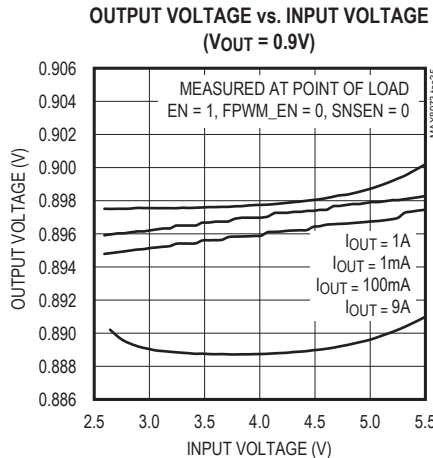
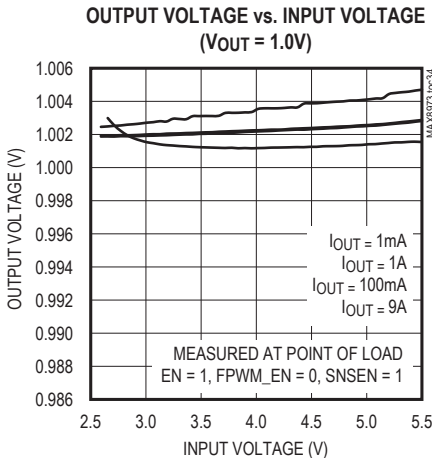
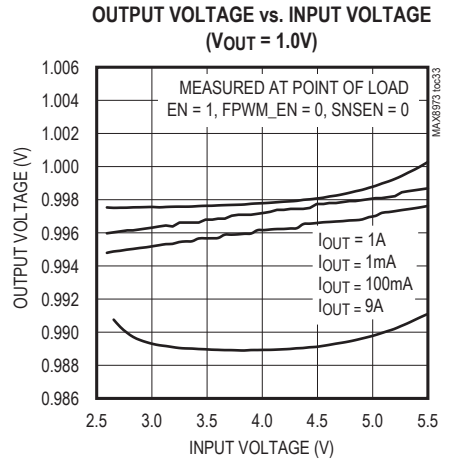
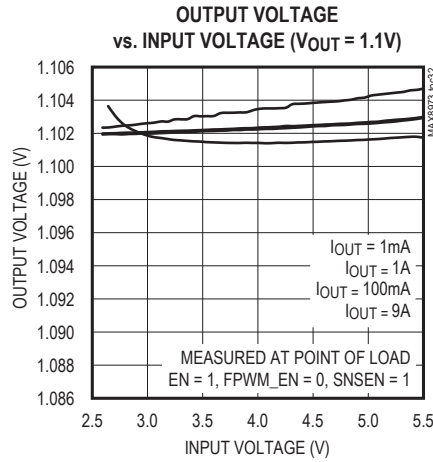
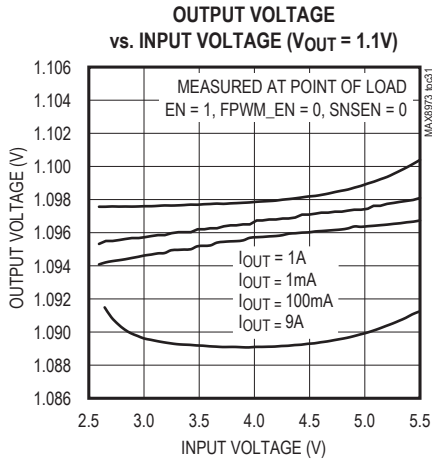
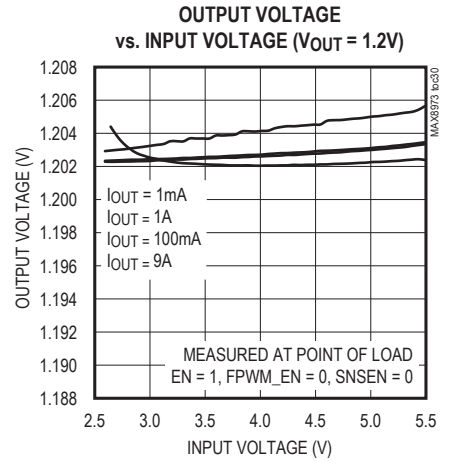
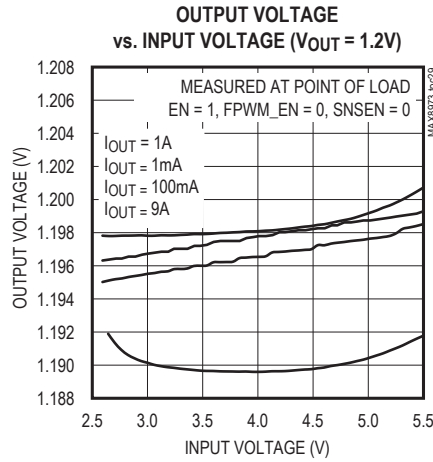
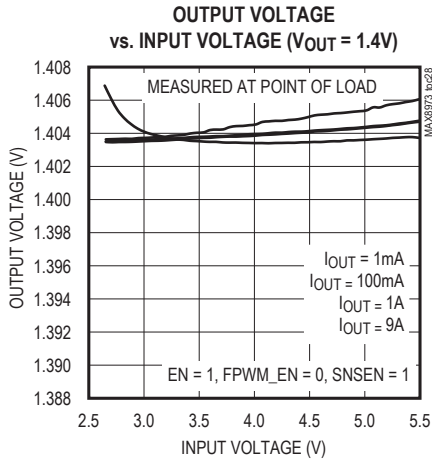
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4.](#))



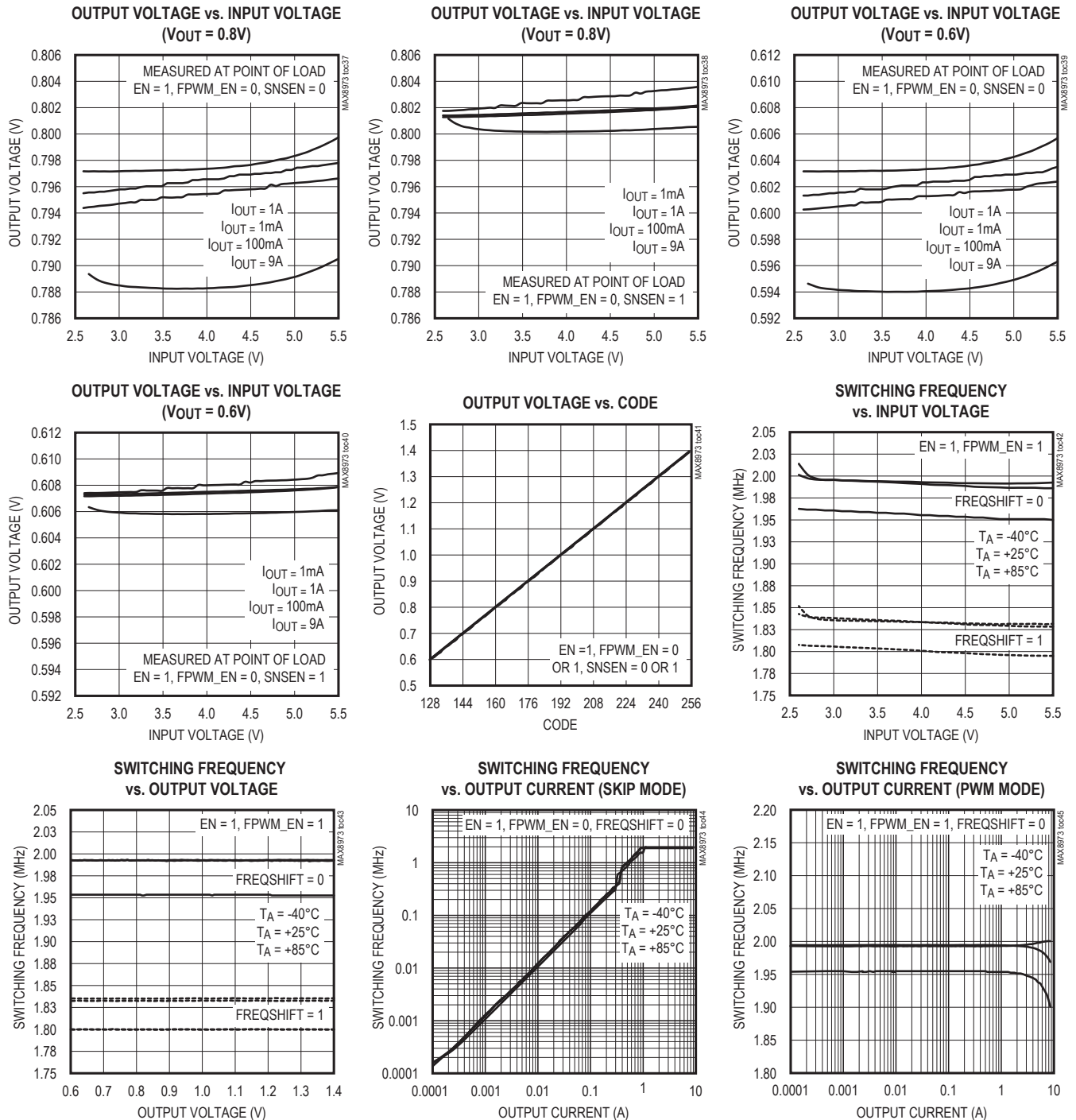
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)



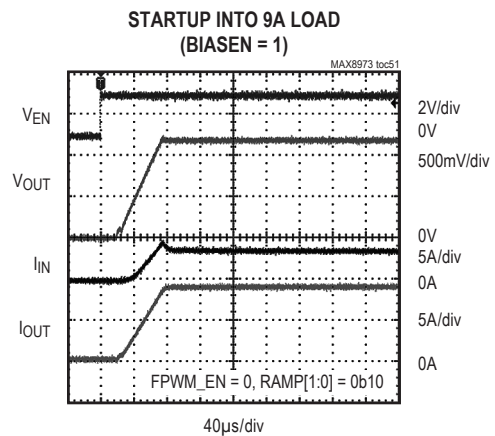
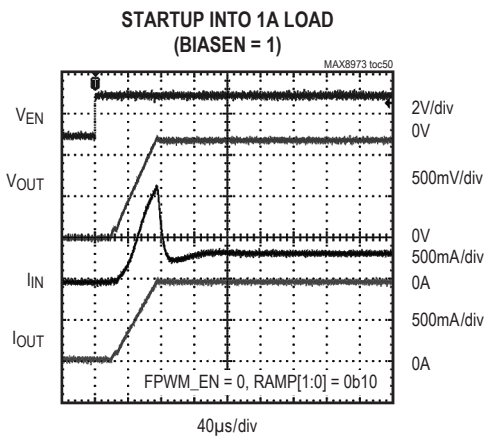
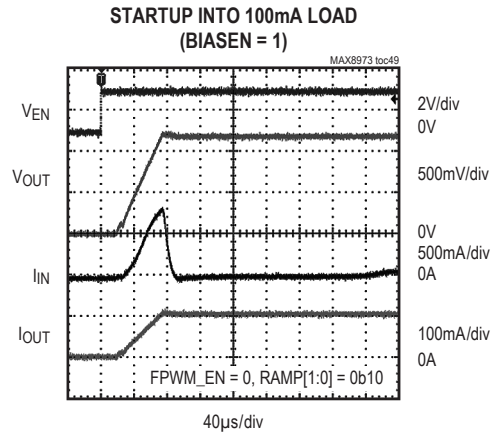
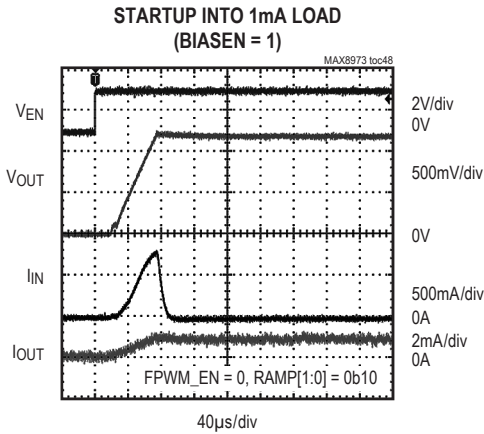
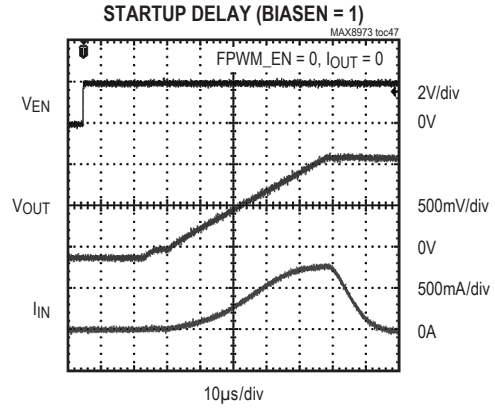
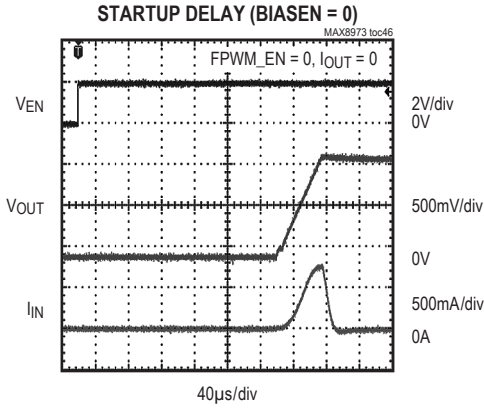
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4](#).)



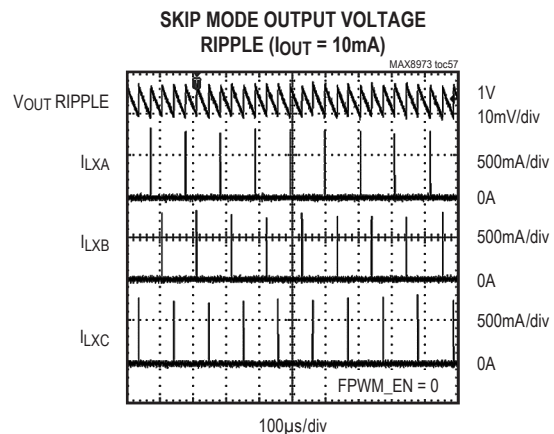
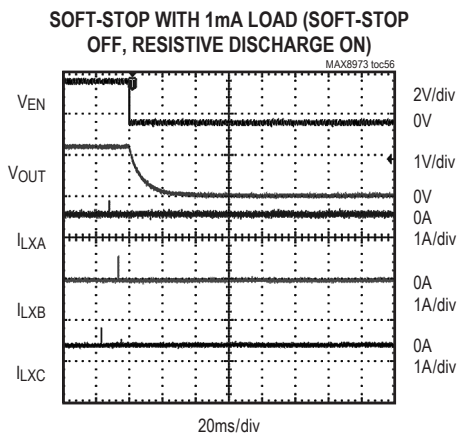
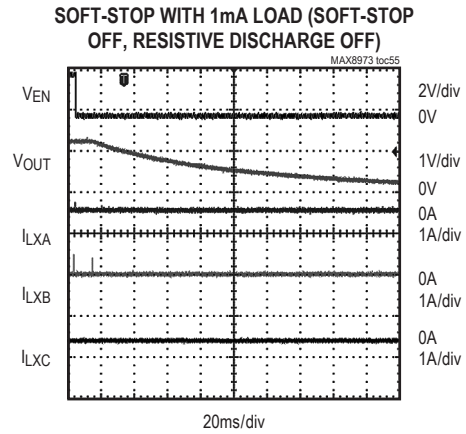
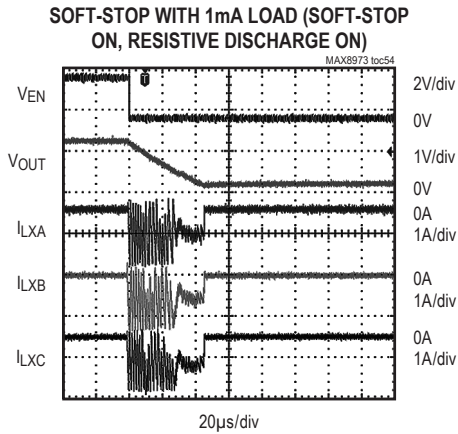
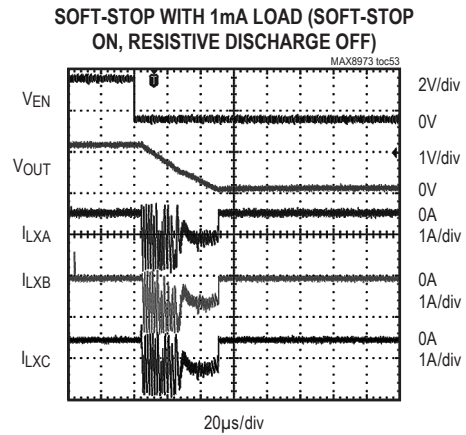
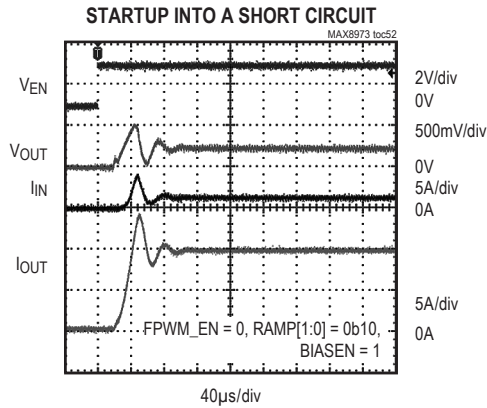
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4.](#))



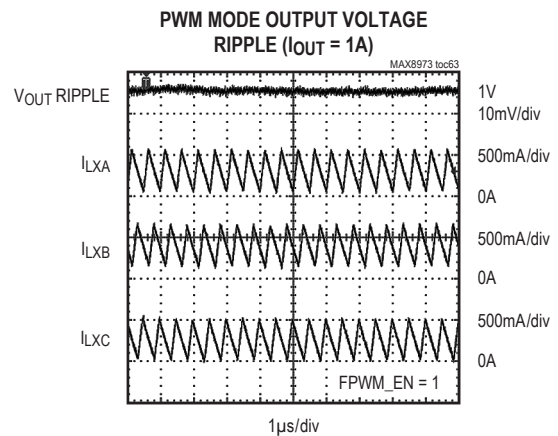
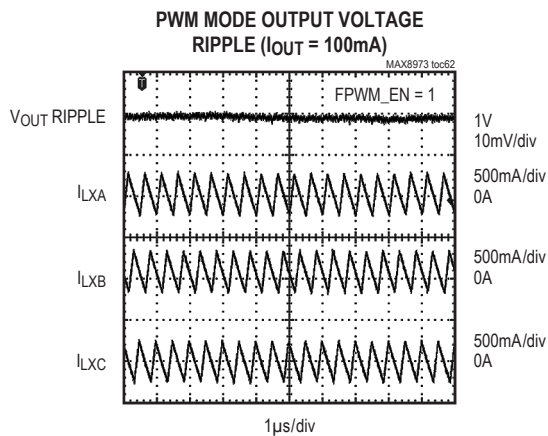
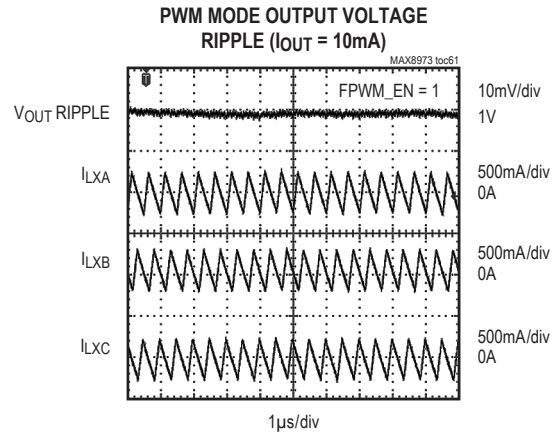
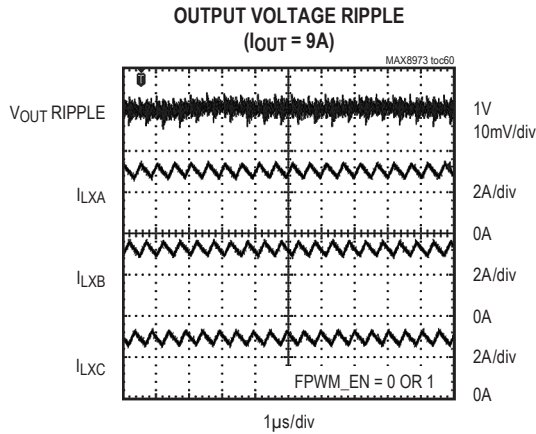
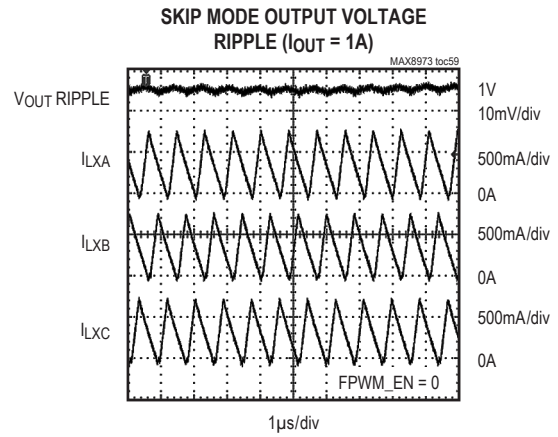
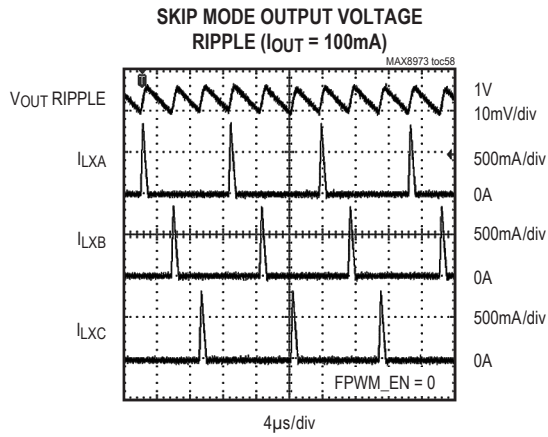
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4.](#))



Typical Operating Characteristics

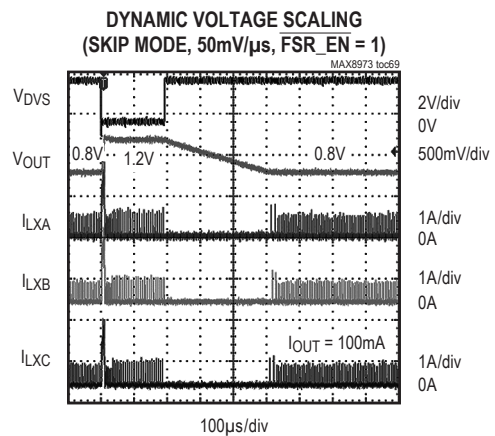
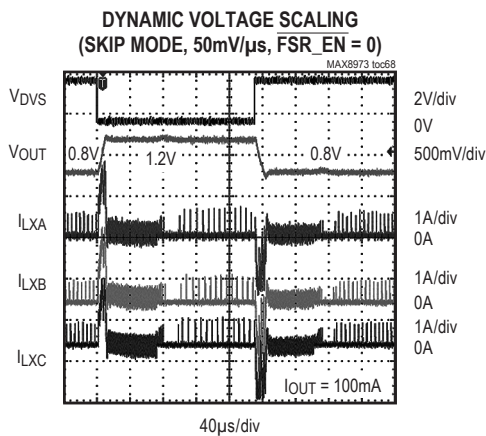
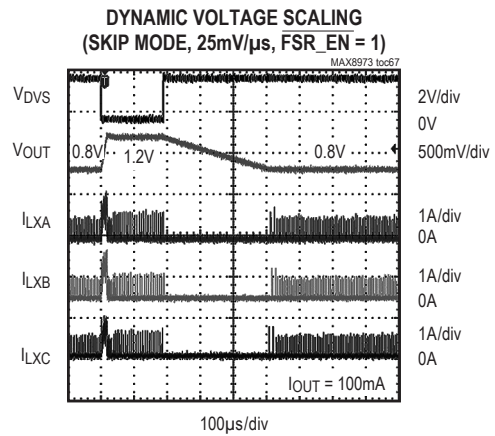
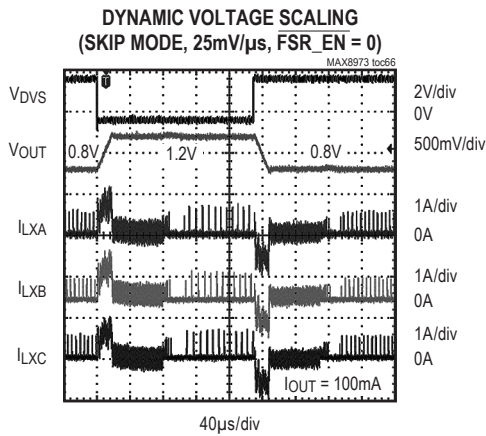
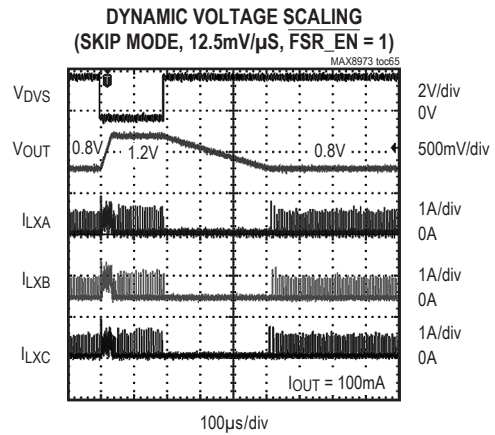
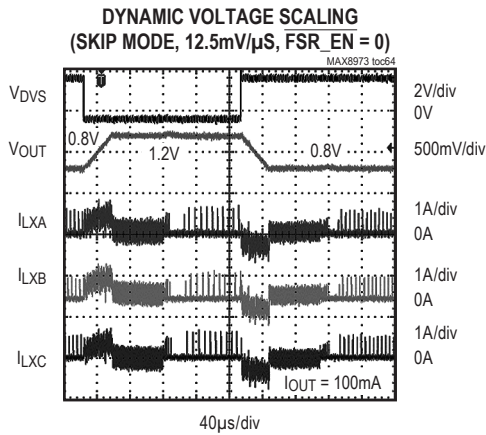
( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)





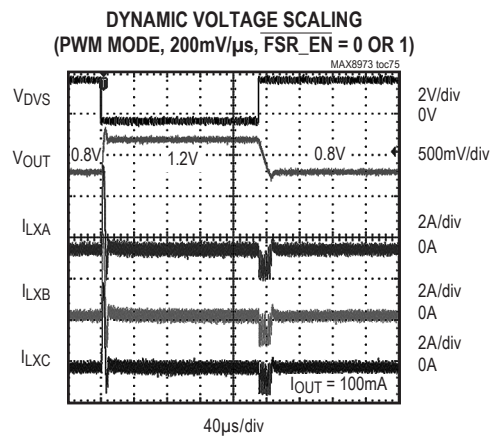
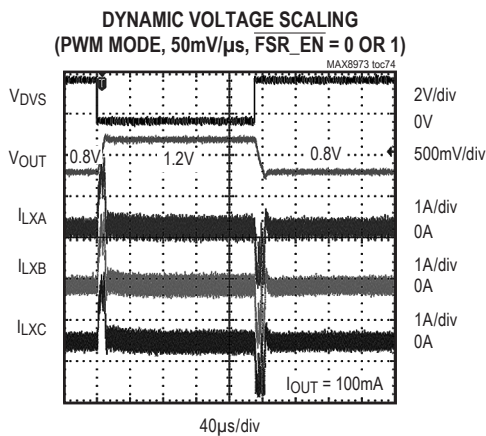
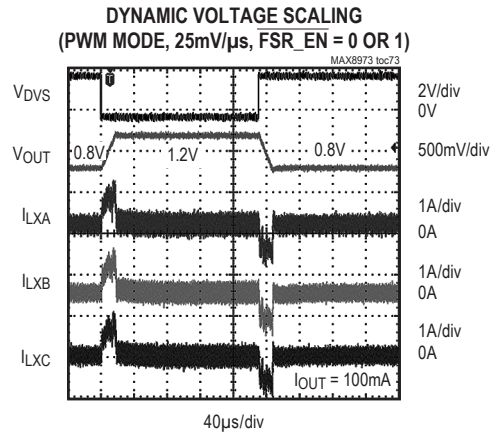
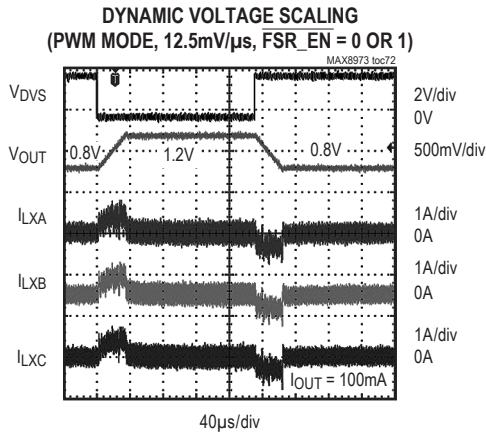
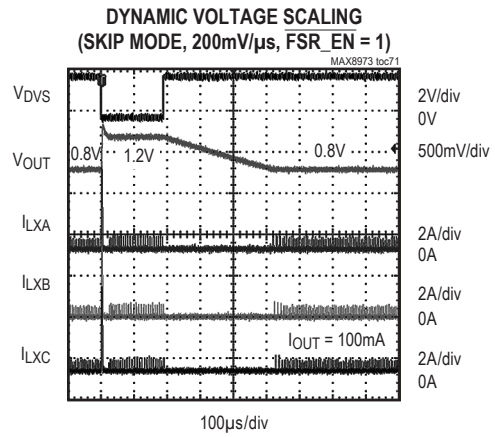
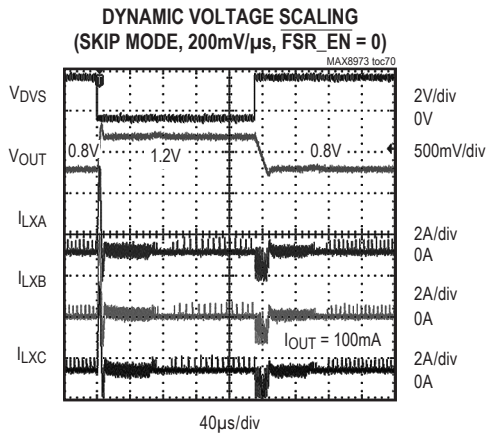
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4](#).)



Typical Operating Characteristics (continued)

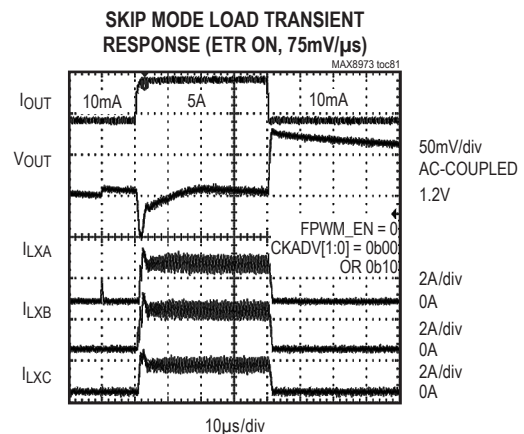
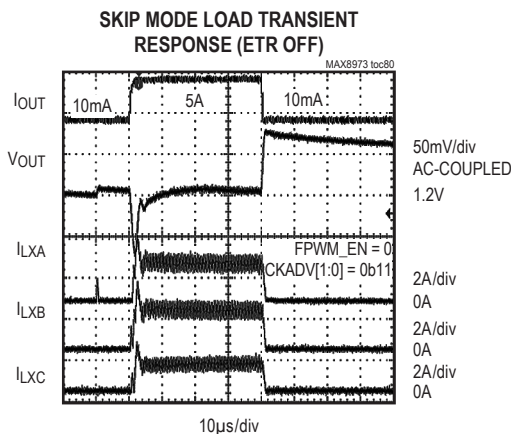
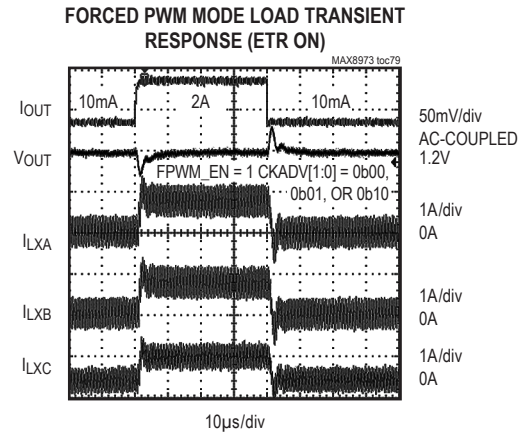
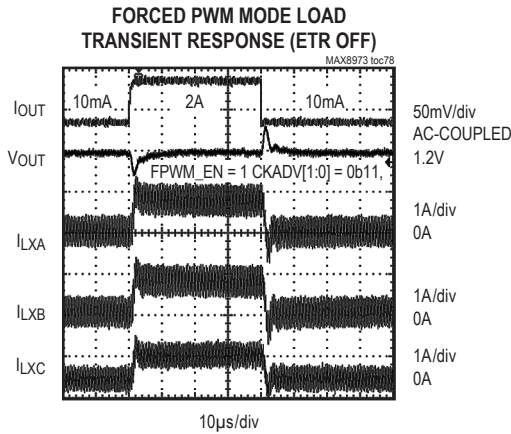
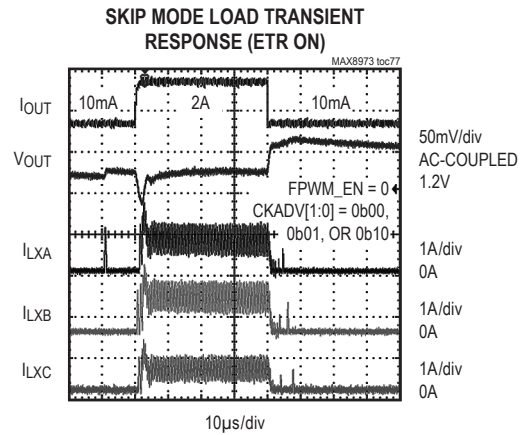
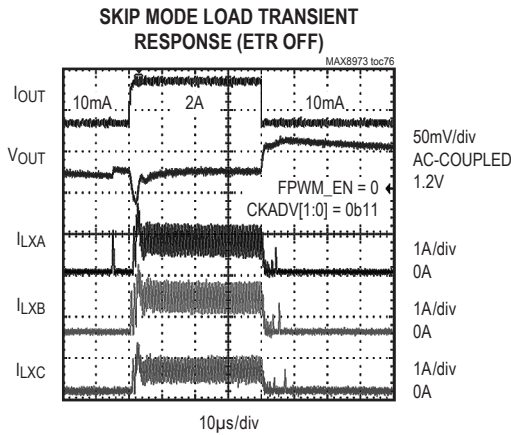
( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of [Figure 4](#).)





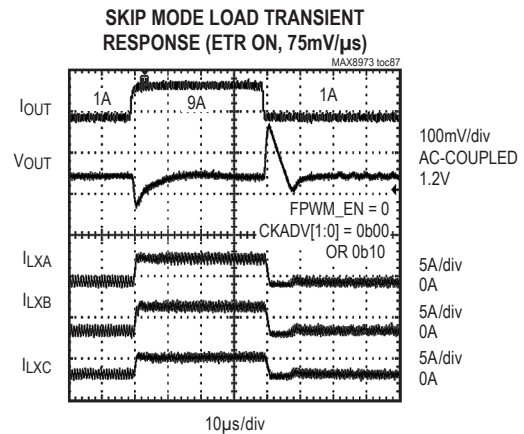
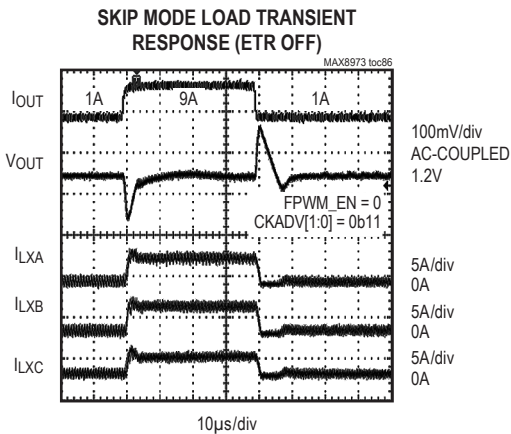
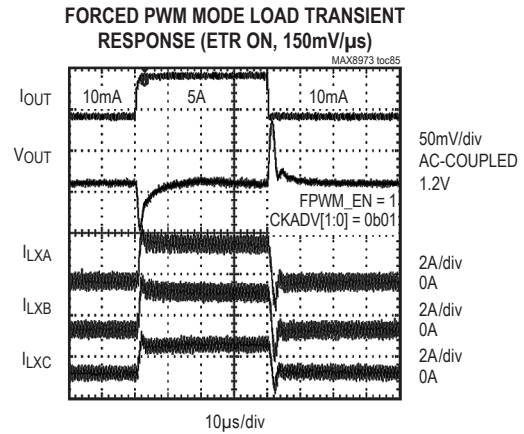
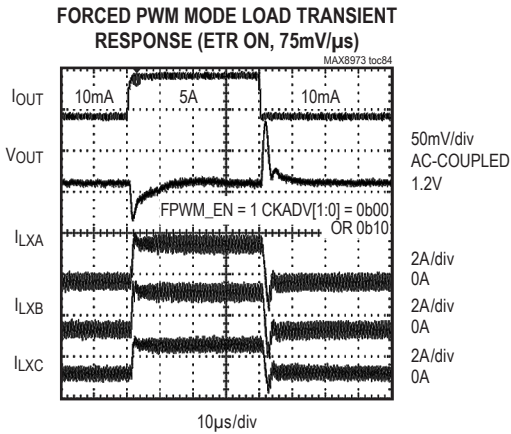
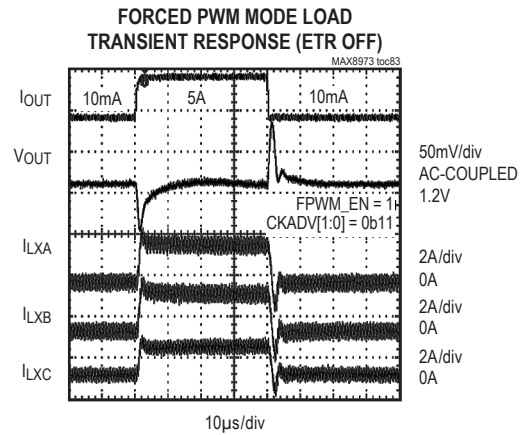
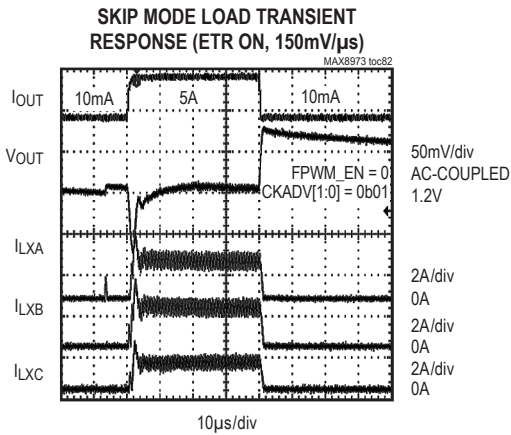
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)



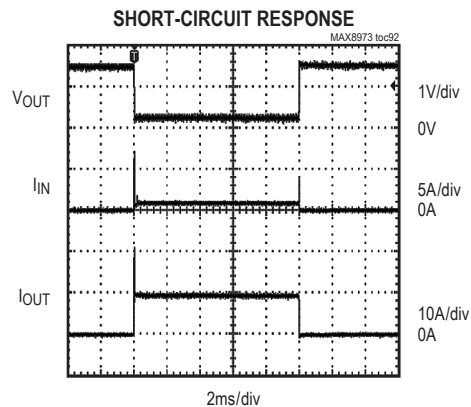
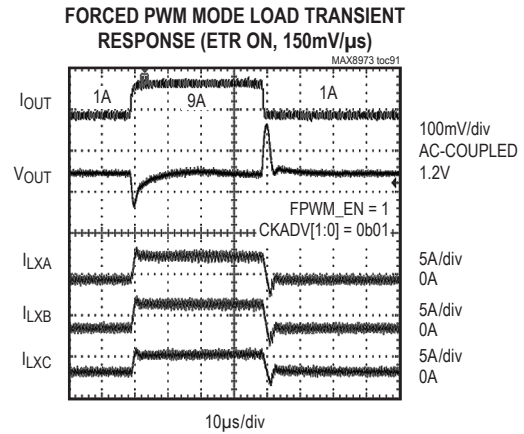
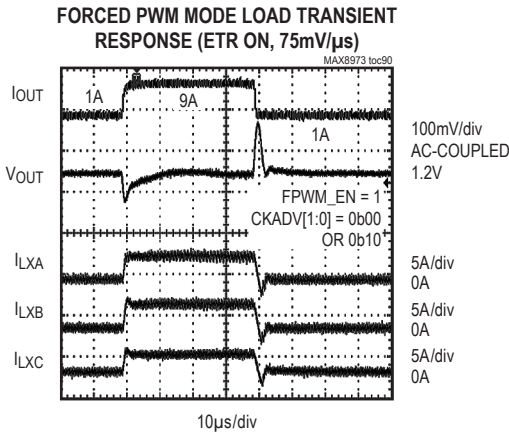
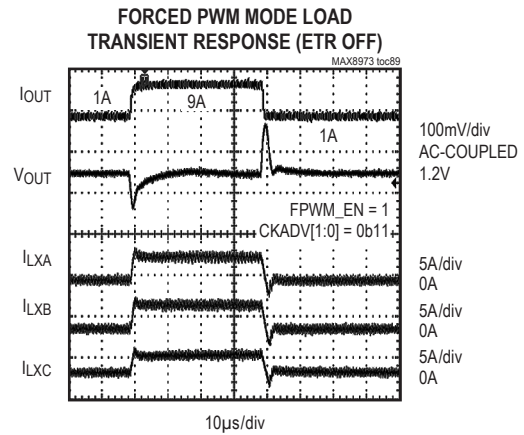
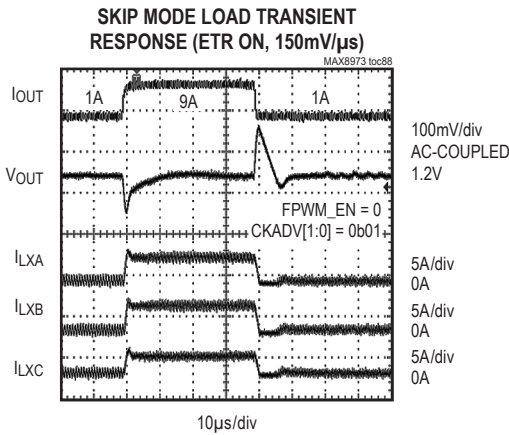
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)



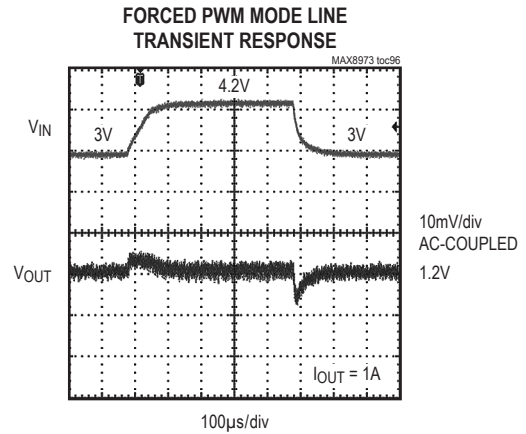
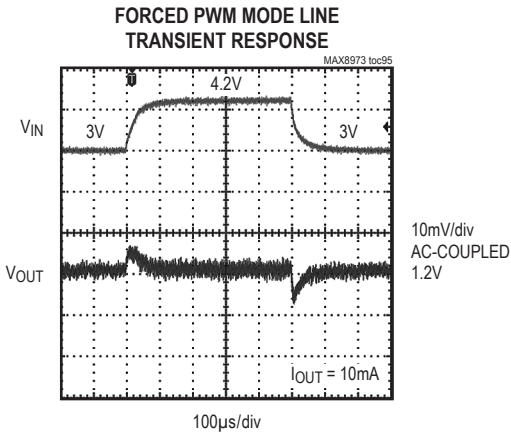
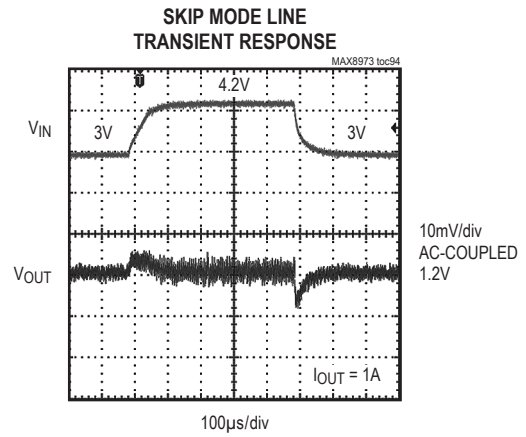
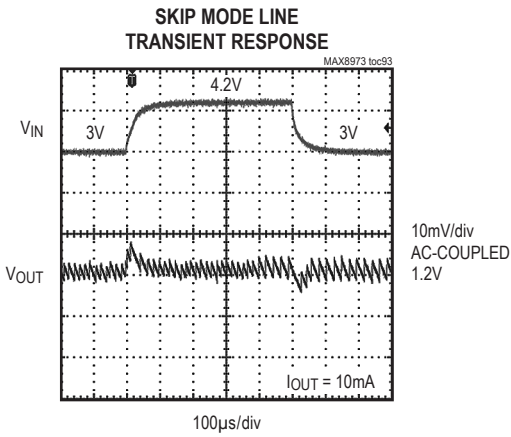
Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)

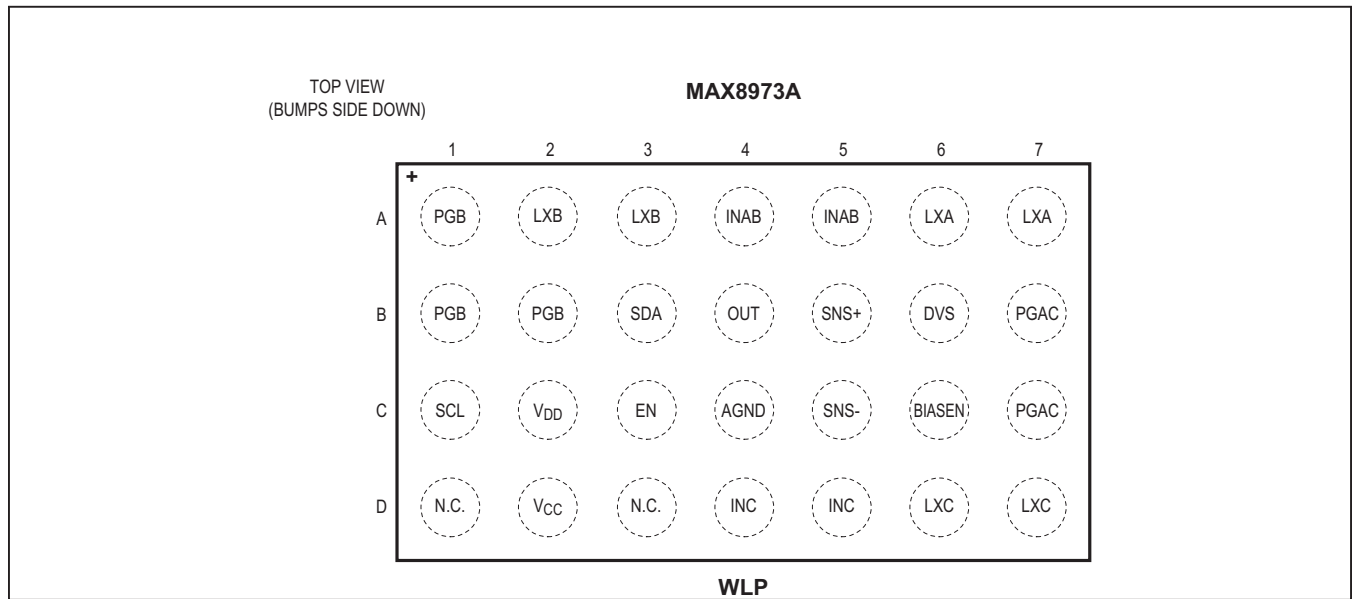


Typical Operating Characteristics (continued)

( $V_{IN} = 3.6V$ ,  $V_{DD} = 1.8V$ ,  $V_{OUT} = 1.2V$ , circuit of Figure 4.)



Pin Configuration



Pin Description

PIN	NAME	DESCRIPTION
A1, B1, B2	PGB	Power Ground for Phase B. Pins A1, B1, and B2. Local to Phase B power devices. Bypass INAB (pin A4) and the Phase B output capacitor to PGB (pins A1/B1/B2). Connect all PG_ pins with a power GND plane underneath the device for heatsinking purposes.
A2, A3	LXB	Inductor Connection for Phase B. LXB connects to the drains of the internal p-Channel and n-Channel FETs. LXB is high impedance in shutdown.
A4	INAB	Power Supply Input to Phase A and B. Pin A4 is local to Phase B power devices. INAB powers the internal p-Channel and n-Channel FETs. Bypass INAB (pin A4) to PGB (pins A1/B1/B2) with a 10µF ceramic capacitor as close as possible to the device. Connect all IN_ pins to the same power source.
A5	INAB	Power Supply Input to Phase A and B. Pin A5 is local to Phase A power devices. INAB powers the internal p-Channel and n-Channel FETs. Bypass INAB (pin A5) to PGAC (pins B7/C7) with a 10µF ceramic capacitor as close as possible to the device. Connect all IN_ pins to the same power source.
A6, A7	LXA	Inductor Connection for Phase A. LXA connects to the drains of the internal p-Channel and n-Channel FETs. LXA is high impedance in shutdown.
B3	SDA	Serial Data Input/Output. SDA is compatible with 1.2V logic.
B4	OUT	Buck Converter Output Node. In addition to setting the regulation point of the converter, OUT also discharges the output capacitor when the converter is shutdown. Connect OUT to common V <sub>OUT</sub> (at the local output capacitors).
B5	SNS+	Output Voltage Remote Sense Positive Input. Connect SNS+ to the positive terminal of the bulk capacitance at the load. Route SNS- and SNS+ as a differential pair through the PCB. The remote sense feature may be disabled through software.

## Pin Description (continued)

PIN	NAME	DESCRIPTION
B6	DVS	DVS Logic Input. When DVS is low the output voltage is programmed by register 0x00h ( $V_{OUT}$ ). When DVS is driven high to $V_{CC}$ , the output voltage is programmed by register 0x01h ( $V_{OUT\_DVS}$ ).
B7, C7	PGAC	Power Ground for Phase A and C. Pin B7 and C7 are local to Phase A and C power devices. Bypass INC (pins D4/D5) and the Phase C output capacitor to PGAC (pins B7/C7). Bypass INAB (pin A5 only) and the Phase A output capacitor to PGAC (pins B7/C7). Connect all PG_ pins with a power GND plane underneath the device for heatsinking.
C1	SCL	Serial Clock Input
C2	$V_{DD}$	Logic Power Supply Input for Serial Interface. Connect $V_{DD}$ to a 1.8V supply. Bypass $V_{DD}$ to AGND with a 0.1 $\mu$ F ceramic capacitor.
C3	EN	EN Logic Input. EN enables buck converter. Drive high to $V_{CC}$ to enable the buck converter. EN has a 500k $\Omega$ resistor to AGND that is connected by default but can be disconnected through the serial interface. The EN input is OR'd with the EN bit in the CONTROL1 register in the MAX8973A.
C4	AGND	Analog Ground
C5	SNS-	Output Voltage Remote Sense Negative Input. Connect SNS- to the negative terminal of the bulk capacitance at the load. Route SNS- and SNS+ as a differential pair through the PCB. The remote sense feature may be disabled through software.
C6	BIASEN	BIASEN Logic Input. BIASEN enables the MAX8973A bias to allow for faster start-up when the EN pin is driven high. Drive high to $V_{CC}$ to enable the fast startup mode. The BIASEN input is OR'd with the BIASEN bit in the Control register.
D1, D3	N.C.	Connect to AGND.
D2	$V_{CC}$	Analog Power Supply Bypass Node. Bypass $V_{CC}$ to AGND with a 1 $\mu$ F ceramic capacitor. $V_{CC}$ is internally connected to INC (pin D4) through a 20 $\Omega$ internal resistor. $V_{CC}$ supplies the internal reference, bias circuitry, feedback circuitry, and serial interface.
D4, D5	INC	Power Supply Input to Phase C. Pins D4 and D5 are local to Phase C power devices. INC powers the internal p-Channel and n-Channel FETs. INC also power $V_{CC}$ through an on-chip 20 $\Omega$ filter resistor. Bypass INC (pins D4/D5) to PGAC (pins B7/C7) with a 10 $\mu$ F ceramic capacitor as close as possible to the device. Connect all IN_ pins to the same power source.
D6, D7	LXC	Inductor Connection for Phase C. LXC connects to the drains of the internal p-Channel and n-Channel FETs. LXC is high impedance in shutdown.

**Detailed Description**

The MAX8973A high-efficiency, three-phase, DC-DC step-down switching regulator with differential remote sensing combines ultra-high efficiency and very fast transient response with world-class accuracy over load, line, and temperature. Three-phase operation with 2MHz switching frequency for each phase allows the use of miniature external components. Differential remote sensing improves output accuracy by providing a Kelvin-sense connection directly at the load. Total output error is less than 0.8% over line, and temperature.

The MAX8973A supports up to a 3.4MHz I<sup>2</sup>C 3.0-compatible serial interface. The output voltage is programmable through the serial interface from 0.60625V to 1.4V in 6.25mV steps. Operating modes and output voltage slew rates of the MAX8973A are also programmable through the serial interface.

Other features include internal soft-start control circuitry to reduce inrush current, overcurrent protection, overtemperature protection, and startup into a prebiased output. A user-enabled slew rate control ramps up and down the output voltage in a controlled manner. An option to slew the output voltage at 200mV/μs is provided, allowing the output voltage to respond to step change commands in as little as 10μs.

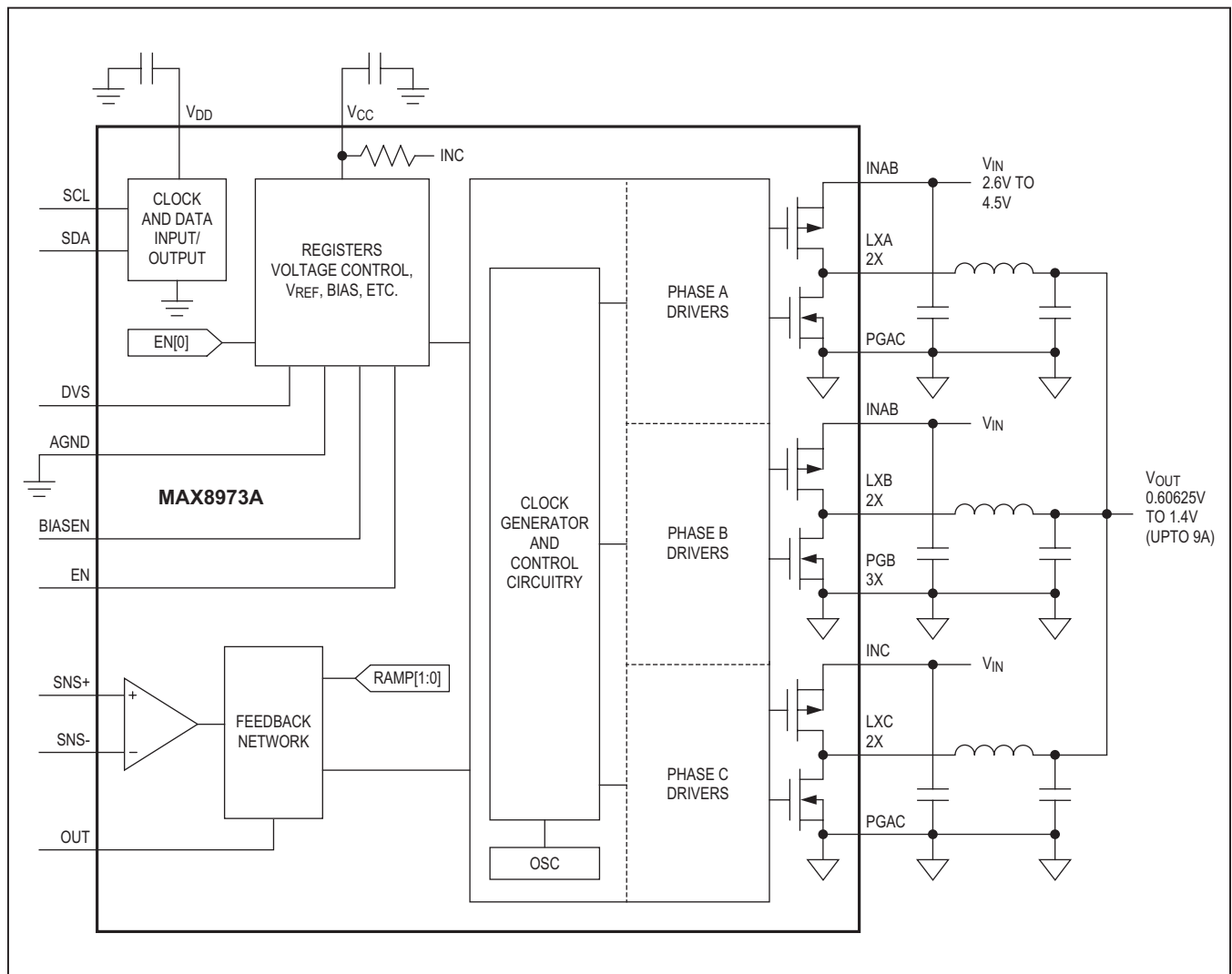


Figure 1. MAX8973\_ Functional Block Diagram



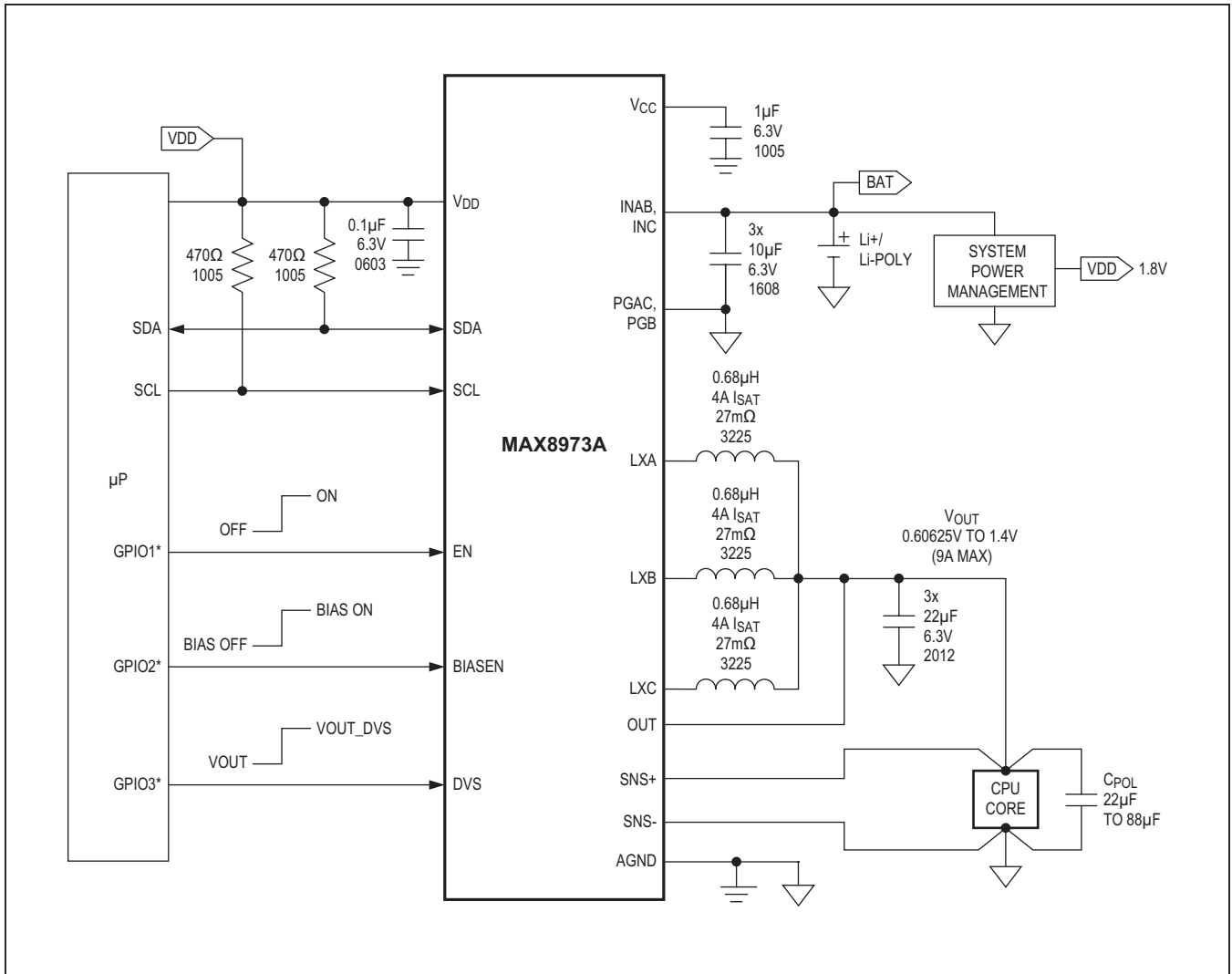


Figure 2. Typical Applications Circuit



### Enabling the Regulator

The MAX8973A output is enabled by driving the EN input high or by setting the EN bit to a 1 with an I<sup>2</sup>C command. The EN input and the EN bit are logically OR'd. Disable the regulator by driving the EN input low and setting the EN bit to a 0. [Table 1](#) shows the logic truth table for the hardware EN input and I<sup>2</sup>C register bit. The register contents may be written at any time to configure the MAX8973A output.

### Startup Delay (BIASEN)

To reduce the startup delay in applications where the CPU core must turn on quickly, the BIASEN logic input is logically OR'd with the BIASEN register bit to set the delay, defined as EN rising to the start of the V<sub>OUT</sub> ramp.

The startup delay is 240μs (typ) when both the BIASEN input and the BIASEN bit are low. Delay is reduced to 20μs (typ) when the BIASEN input is high or the BIASEN bit is set to 1. Selecting the shorter 20μs delay increases quiescent current consumption by 34μA if the EN input is low and the EN bit is set to 0 (step-down regulator is off). [Table 2](#) provides the truth table for the BIASEN input and register bit.

### Startup Ramp Rate

The MAX8973A features selectable startup ramp rates. The startup ramp rate is programmed to 20mV/μs by default, with an optional rate of 200mV/μs. The RAMP[1:0] bits in the CONTROL1 register select the startup ramp rate, as shown in [Table 3](#) on page 26. The RAMP[1:0]

bits control the DVS ramp rate, in addition to the startup ramp rate. The default setting for the RAMP[1:0] bits is 0b10, which selects the 20mV/μs startup ramp rate and the 50mV/μs DVS ramp rate.

When the fastest startup ramp rate is selected, the actual output voltage may ramp at a rate slower than 200mV/μs when a charging a large output capacitance due to peak inductor current limit.

### Disabling the Regulator (Active Discharge)

Disable the MAX8973A step-down regulator output by driving the EN logic input low and setting the EN bit to 0. [Table 1](#) shows the truth table for enabling and disabling the converter. The MAX8973A provides two different mechanisms for discharging the output capacitance. A resistive discharge path discharges the MAX8973A output capacitance when the converter is disabled. The resistive discharge path is selected with the AD\_EN bit in the CONTROL2 register. In addition to the resistive discharge path, a soft-stop function actively pulls energy from the output capacitance, and recycles this energy back into the input capacitance and battery. The soft-stop function is enabled by setting the FSR\_EN bit in the CONTROL1 register to a 0. The soft-stop function discharges the output capacitance at a slew rate selected by the RAMP[1:0] bits in the CONTROL1 register. [Table 4](#) shows the truth table for the active discharge functions.

**Table 1. MAX8973A Enable Truth Table**

EN (INPUT)	EN (BIT)	REGULATOR STATUS
0	0	Off
0	1	On
1	0	On
1	1	On

**Table 2. BIASEN and Startup Delay Truth Table**

BIASEN (PIN)	BIASEN (BIT)	STARTUP DELAY (μs)	I <sub>CC</sub> (μA)
0	0	240	2
0	1	20	34
1	0	20	34
1	1	20	34

**Table 3. MAX8973A Startup and DVS Ramp Rates**

RAMP[1:0]	STARTUP RAMP RATE (mV/μs)	DVS RAMP RATE (mV/μs)
0b00	20	12.5
0b01	20	25
0b10	20	50
0b11	200	200

**Table 4. MAX8973A Output Discharge Selection Truth Table**

AD_EN (BIT)	FSR_EN (BIT)	OUTPUT DISCHARGE METHOD
0	0	Soft-stop only
0	1	None (load current only)
1	0	Soft-stop and resistive
1	1	Resistive only

**Soft-Stop (Active Energy Recovery)**

The MAX8973A features a soft-stop mechanism to actively discharge the output capacitance when the regulator is disabled. Setting the  $\overline{\text{FSR\_EN}}$  bit in the CONTROL1 register to a 0 enables the soft-stop function when the converter is disabled. Soft-stop ramps down the target output voltage at a rate selected by the RAMP[1:0] bits in the CONTROL1 register. Table 5 lists the selectable soft-stop slew rates. Figure 3 illustrates the soft-stop behavior.

Note that when the fastest soft-stop ramp rate is selected, the actual output voltage may ramp down at a rate slower than  $200\text{mV}/\mu\text{s}$  when discharging a large output capacitance due to negative inductor current limit.

The soft-stop function takes advantage of the switching converter topology, by operating the converter as a boost regulator to discharge the output capacitance and transfer the energy stored in the output capacitance into the input capacitance. The soft-stop function keeps the MAX8973A enabled until the output voltage is discharged to  $100\text{mV}$  (typ), at which time resistive discharge starts, completely discharging the output capacitance to GND.

**Table 5. MAX8973A Soft-Stop Slew Rate**

RAMP[1:0]	SOFT-STOP RAMP RATE (mV/ $\mu\text{s}$ )
0b00	20
0b01	20
0b10	20
0b11	200

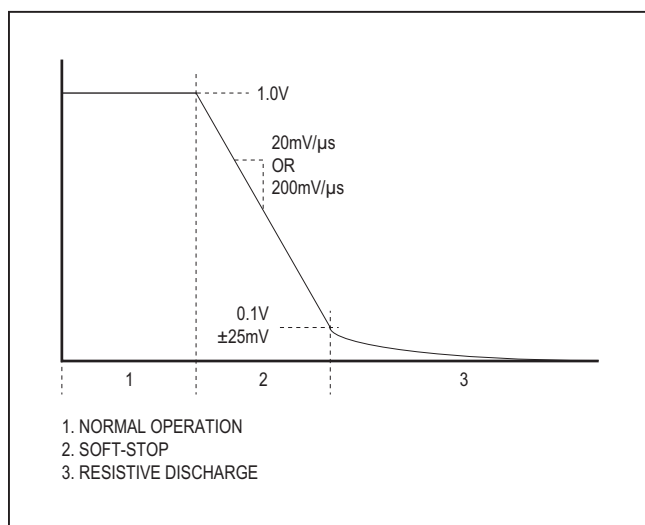


Figure 3. Soft-Start Discharge

A negative inductor current limit protects the internal switches from excessive power dissipation while the soft-stop function is active. When discharging a large output capacitance, the negative current limit may determine the discharge ramp rate, rather than the value set by the RAMP[1:0] settings in Table 5.

**Resistive Discharge**

Setting  $\text{AD\_EN} = 1$  in the CONTROL2 register connects a  $100\Omega$  pulldown resistor from OUT to AGND when the MAX8973A regulator is disabled. If  $\text{AD\_EN} = 0$  and soft-stop is not enabled, the MAX8973A output drifts to GND at a rate determined by the load current.

**Setting the Output Voltage**

The MAX8973A features two registers for setting the output voltage,  $V_{\text{OUT}}$  and  $V_{\text{OUT\_DVS}}$ . This flexibility in how the output voltage is set. Either the  $V_{\text{OUT}}$  (or  $V_{\text{OUT\_DVS}}$ ) register can be written repeatedly with the DVS input tied to a fixed logic state, or both registers can be written with the DVS logic input toggling between the two registers. The output voltage ramps to the new target voltage according to the RAMP[1:0] settings shown in Table 3, regardless of which method is used to change the output voltage.

**DVS**

The MAX8973A output voltage toggles between two different voltage settings by driving the DVS logic input high or low. The DVS logic input selects the default power-up voltage or dynamically changes the output voltage setting between target voltages programmed through the serial interface.

**Default Power-Up Voltage**

The MAX8973A default output voltage is selected by driving the DVS logic input high or low prior to enabling the step-down regulator. Table 6 lists the default voltage settings for the MAX8973A.

The MAX8973A power-up voltages may be changed by writing new target output voltages to the  $V_{\text{OUT}}$  register ( $\text{DVS} = \text{AGND}$ ) and/or the  $V_{\text{OUT\_DVS}}$  register ( $\text{DVS} = V_{\text{DD}}$ ) prior to driving the EN pin high or setting the EN bit = 1 to enable the step-down regulator.

**Table 6. Default Output Voltage Settings**

PART NUMBER	DEFAULT $V_{\text{OUT}}$	
	DVS = AGND	DVS = $V_{\text{DD}}$
MAX8973A	1.0V	1.2V

**Slew Rate Control**

The MAX8973A provides four programmable ramp rates for output voltage transitions between target codes. The output voltage is always actively ramped when the new target voltage is greater than the current output voltage. Table 3 lists the four settings for DVS ramp rates, set by the RAMP[1:0] bits in the CONTROL1 register.

If the new target voltage is less than the current output voltage, the ramp-down response is determined by the state of the FSR\_EN and FPWM\_EN bits. Table 7 below summarizes the MAX8973A response to a command to decrease the target output voltage.

**Control Scheme**

The MAX8973A three-phase step-down regulator operates with a pulse-skipping scheme under light-to-medium loads, and transitions to a 2MHz fixed-frequency switching scheme under moderate-to-heavy loading. Alternatively, the MAX8973A may operate with forced-PWM mode under all loads, if configured by setting the FPWM\_EN bit in the CONTROL1 register to a 1.

**Modes of Operation (Skip, Mid, CCM)**

Under light loads, the MAX8973A operates in skip mode with Rotational Phase Spreading. Under Rotational Phase Spreading, all three phases continue to switch in an interleaved manner, regardless of load. As load current increases, the switching pulses become more frequent. As load current continues to increase, the on-times of all three phases begin to overlap, but each phase continues pulse skipping when considered on an individual basis to maximize efficiency. As load current continues to increase, the inductor currents lift off, and a seamless transition into CCM operation occurs. The MAX8973A switches at a fixed 2MHz per phase switching frequency while operating in CCM mode. Once in CCM operation, as load current decreases and the inductor current in any

**Table 7. DVS Response to Decrease in Target VOUT**

FSR_EN	FPWM_EN	DVS RESPONSE
0	0	Output ramps down at rate set by RAMP[1:0]
0	1	Output ramps down at rate set by RAMP[1:0]
1	0	Output decays at rate set by load current and output capacitance
1	1	Output ramps down at rate set by RAMP[1:0]

phase triggers a zero-crossing, the step-down regulator seamlessly transitions back into pulse-skipping mode.

In skip and mid modes, the amplitude of the inductor current pulses is fixed. In CCM mode, the switching frequency is fixed, and the peak-to-peak inductor ripple current depends on the duty cycle and inductance.

**Modes of Operation (FPWM)**

The MAX8973A step-down regulator operates in forced PWM mode, regardless of load current, by setting the FPWM\_EN bit in the CONTROL1 register to a 1. In forced PWM mode, the MAX8973A switches at a fixed 2MHz per phase under all load conditions. Negative inductor current is allowed under light load conditions in forced PWM mode.

**Current Sensing**

The MAX8973A uses a lossless current-sensing scheme for control loop stability. The time constant of the inductance and the inductor’s DCR is matched to an internal RC network. The MAX8973A are factory trimmed for optimization with particular inductances and ranges of DCR. See Table 8 on page 30 for a list of optimal inductor parameters for each version of the MAX8973A.

The INDUCTOR[1:0] bits in the CONTROL2 register influence the gain and slope compensation of the current sense signal generated by the internal RC network used for sensing the inductor current. **Note: The INDUCTOR[1:0] settings should not be modified while the converter is operating.**

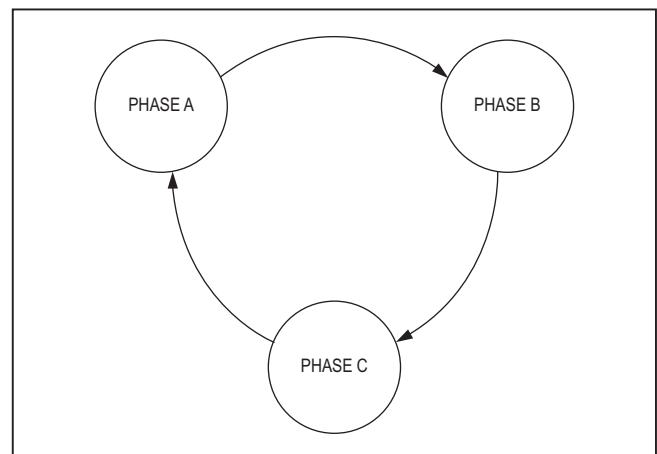


Figure 4. Rotational Phase Spreading Algorithm

**Table 8. MAX8973A Inductor Parameters**

PART NUMBER	L (µH)	DCR (mΩ)
MAX8973A	0.68	27

### Maximum Output Current

The MAX8973A maximum output current is influenced by many parameters. Use the following equation to determine the worst-case maximum output current:

$$I_{OUTMAX} = N \times (PLIM - (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{2 \times L \times V_{IN} \times f})$$

Where N = 3 (number of phases), PLIM = minimum peak current limit,  $V_{IN}$  = maximum input voltage,  $V_{OUT}$  = maximum output voltage, L = minimum expected inductance, and f = minimum switching frequency.

### Overload and Short Circuit Protection

The MAX8973A is protected against overloads with a peak current limit for each phase. In the event that an overload is applied to the output of the MAX8973A, the inductor current for each phase ramps up to the current limit to try to maintain the output in regulation.

The MAX8973A is protected against a short-circuited output. In the event that the output is short-circuited, the inductor currents for each phase ramp up to the peak current limit, at which time the high-side MOSFET is turned off. If  $V_{OUT} < 75\%$  of its target, the high-side is held off until the inductor current decreases to the NMOS current limit, at which time the high-side is allowed to turn on again. This prevents inductor current from running away, and also reduces power dissipation by reducing the output power that the device can provide. The MAX8973A does not automatically turn off when the output is short-circuited. If the short-circuit is removed, the MAX8973A output ramps back up to the target voltage, and normal operation resumes.

### Enhanced Transient Response (ETR)

The MAX8973A features an enhanced transient response circuit that is enabled through software. The enhanced transient response reduces the voltage droop during large load steps by temporarily allowing all three phases to fire in unison, slewing total inductor current faster than would normally be possible if all three phases continued to operate 120° out of phase. The enhanced transient response detector features two selectable sensitivity settings, which select the output voltage slew rate during load transients that triggers the ETR circuit. The sensitivity of the ETR detector is set by the CKADV[1:0] bits in the CONTROL2 register. [Table 9](#) summarizes the ETR settings.

**Table 9. Enhanced Transient Response Settings**

CKADV[1:0]	Sensitivity	$V_{OUT} \Delta V/\Delta t$
00	High	75mV/μs
01	Low	150mV/μs
10	High	75mV/μs
11	Off	N/A

### Remote Sense

The MAX8973A features differential remote sensing of the output voltage at the point of load. Differential remote sensing compensates for voltage drops across the traces carrying high current from the MAX8973A output to the point of load. Differential remote sensing is enabled by writing a 1 to the SNSEN bit in the CONTROL1 register.

### Thermal Protection

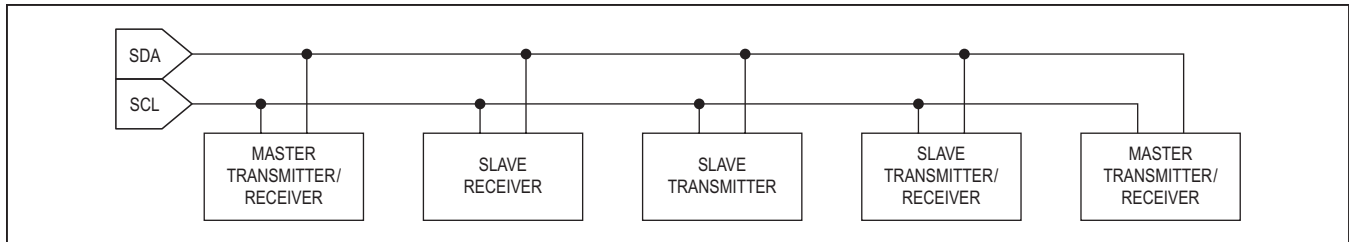
The MAX8973A is protected against thermal overload with an internal temperature sensor. If the die temperature reaches 160°C, the MAX8973A step-down regulator immediately turns off. The step-down regulator restarts when the die temperature decreases by 20°C.

### I<sup>2</sup>C Interface

The MAX8973A step-down regulator provides an I<sup>2</sup>C 3.0-compatible (3.4MHz) serial interface. This 2-wire serial interface consists of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX8973A acts as a slave-only device in normal mode where it relies on the master to generate a clock signal. The MAX8973A supports SCL clock rates from 0Hz to 3.4MHz. I<sup>2</sup>C is an open-drain bus and therefore SDA and SCL require pull-ups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize cross-talk and undershoot on bus signals.

### I<sup>2</sup>C Interface Features

- I<sup>2</sup>C revision 3.0-compatible serial communications channel
  - 0Hz to 100kHz (standard mode)
  - 0Hz to 400kHz (fast mode)
  - 0Hz to 1MHz (fast mode plus)
  - 0Hz to 3.4MHz (high-speed mode)
- Does not utilize I<sup>2</sup>C clock stretching

Figure 5. I<sup>2</sup>C Example System

### I<sup>2</sup>C System Configuration

The I<sup>2</sup>C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 5 shows an example of a typical I<sup>2</sup>C system. A device on the I<sup>2</sup>C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX8973A I<sup>2</sup>C-compatible interfaces are operating in normal mode, they are a slave on the I<sup>2</sup>C bus and it can be both a transmitter and a receiver.

### I<sup>2</sup>C Interface Power

The MAX8973A I<sup>2</sup>C interface derives its power from an externally supplied power rail ( $V_{DD}$  in Figure 1). Cycling  $V_{IN\_}$  resets the I<sup>2</sup>C registers.

### I<sup>2</sup>C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals.

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

### I<sup>2</sup>C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START (S) condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA, while SCL is high (Figure 6).

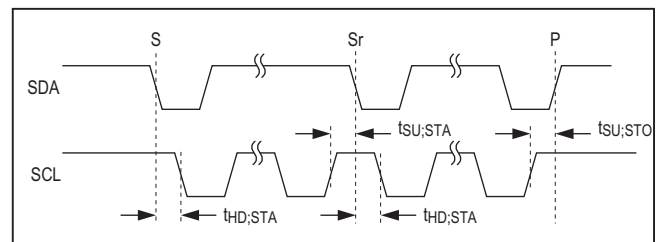


Figure 6. START and STOP Conditions

A START condition from the master signals the beginning of a transmission to the MAX8973A. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition. The STOP condition frees the bus. To issue a series of commands to the slave, the master may issue repeated start (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the MAX8973A internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feed-through.

### I<sup>2</sup>C Acknowledge Bit

Both the I<sup>2</sup>C bus master and the MAX8973A (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 7).

To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.



Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

**I<sup>2</sup>C Slave Address**

The MAX8973A implements 7-bit slave addressing. An I<sup>2</sup>C bus master initiates communication with a slave device (MAX8973A) by issuing a START condition followed by the slave address. As shown in Table 10, the MAX8973A responds to a single slave address. The MAX8973A does not acknowledge all addresses besides the ones listed in Table 10.

Figure 8 shows an example of the slave address byte format. As shown, the slave address byte consists of seven address bits and a read/write bit (R/W). After receiving the factory set slave address shown in Table 10, the MAX8973A issues an acknowledge by pulling SDA low during the ninth clock cycle.

**I<sup>2</sup>C Clock Stretching**

The clock signal generation for the I<sup>2</sup>C bus is generally the responsibility of the master device. The I<sup>2</sup>C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is called clock stretching. The MAX8973A does not support clock stretching.

**I<sup>2</sup>C General Call Address**

The MAX8973A does not implement the I<sup>2</sup>C specification's general call address. If the MAX8973A sees the general call address (0b0000\_0000), it issues a not acknowledge (nA).

**Table 10. MAX8973\_ I<sup>2</sup>C Slave Addresses**

PART NUMBER	SLAVE ADDRESS WRITE	SLAVE ADDRESS READ
MAX8973A	0x36	0x37

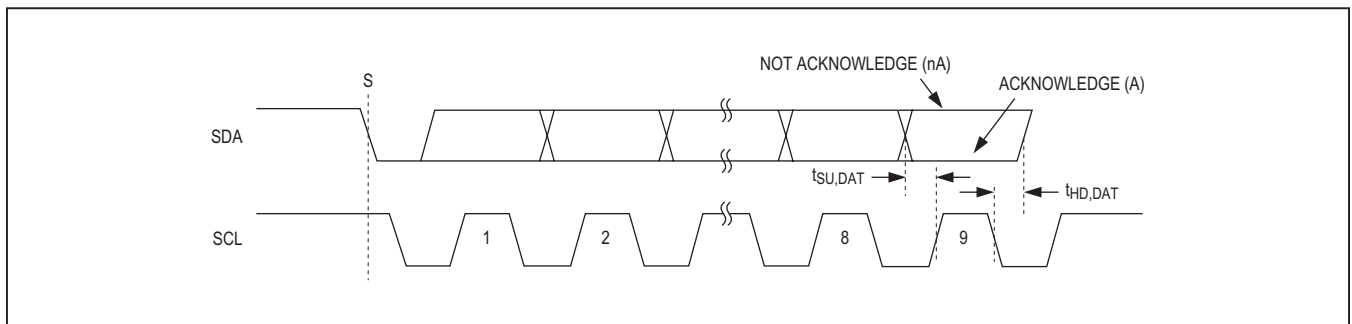


Figure 7. I<sup>2</sup>C Acknowledge (A) and Not-Acknowledge (nA)

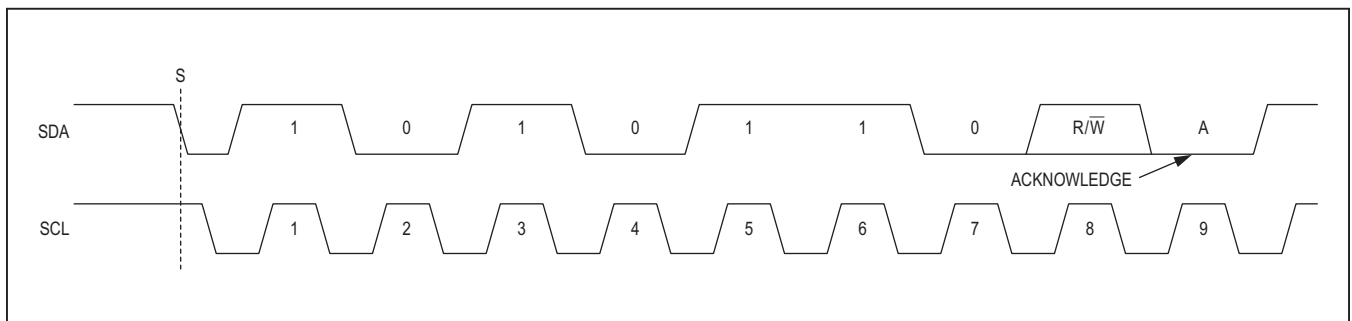


Figure 8. Slave Address Byte Example

**I<sup>2</sup>C Communication Speed**

The MAX8973A is compatible with all 4 communication speed ranges as defined by the revision 3.0 I<sup>2</sup>C specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance ( $C \times R$ ) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. See the *Pullup Resistor Sizing* section of the I<sup>2</sup>C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6k $\Omega$  pullup resistors, a 400kHz bus needs about a 1.5k $\Omega$  pullup resistors, and a 1MHz bus needs 680 $\Omega$  pullup resistors. When the open-drain bus is low, the pullup resistor is dissipating power, and that lower value pullup resistors dissipate more power ( $V^2/R$ ).

Operating in high-speed mode requires some special considerations. For a full list of considerations see the I<sup>2</sup>C 3.0 specification. The major considerations with respect to the MAX8973A are:

- The I<sup>2</sup>C bus master use current source pullups to shorten the signal rise times.
- The I<sup>2</sup>C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the MAX8973A inputs filters are set for standard mode, fast mode, or fast mode plus (i.e. 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the [Engaging HS Mode for Operation up to 3.4MHz](#) section.

**I<sup>2</sup>C Communication Protocols**

The MAX8973A supports both writing and reading from its registers. The MAX8973A supports writing to a single register, writing multiple bytes using register-data pairs, reading from a single register, and reading from sequential registers.

**Writing to a Single Register**

[Figure 9](#) shows the protocol for the I<sup>2</sup>C master device to write one byte of data to the MAX8973A. This protocol is the same as the SMBus specification's write byte protocol. The write byte protocol is as follows:

- 1) The master sends a start (S) command.
- 2) The master sends the 7-bit slave address followed by a write bit ( $R/\bar{W} = 0$ ).
- 3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 4) The master sends an 8-bit register pointer.
- 5) The slave acknowledges the register pointer.
- 6) The master sends a data byte.
- 7) The slave updates with the new data
- 8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
- 9) The master sends a stop (P) condition or a repeated start (Sr) condition. Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

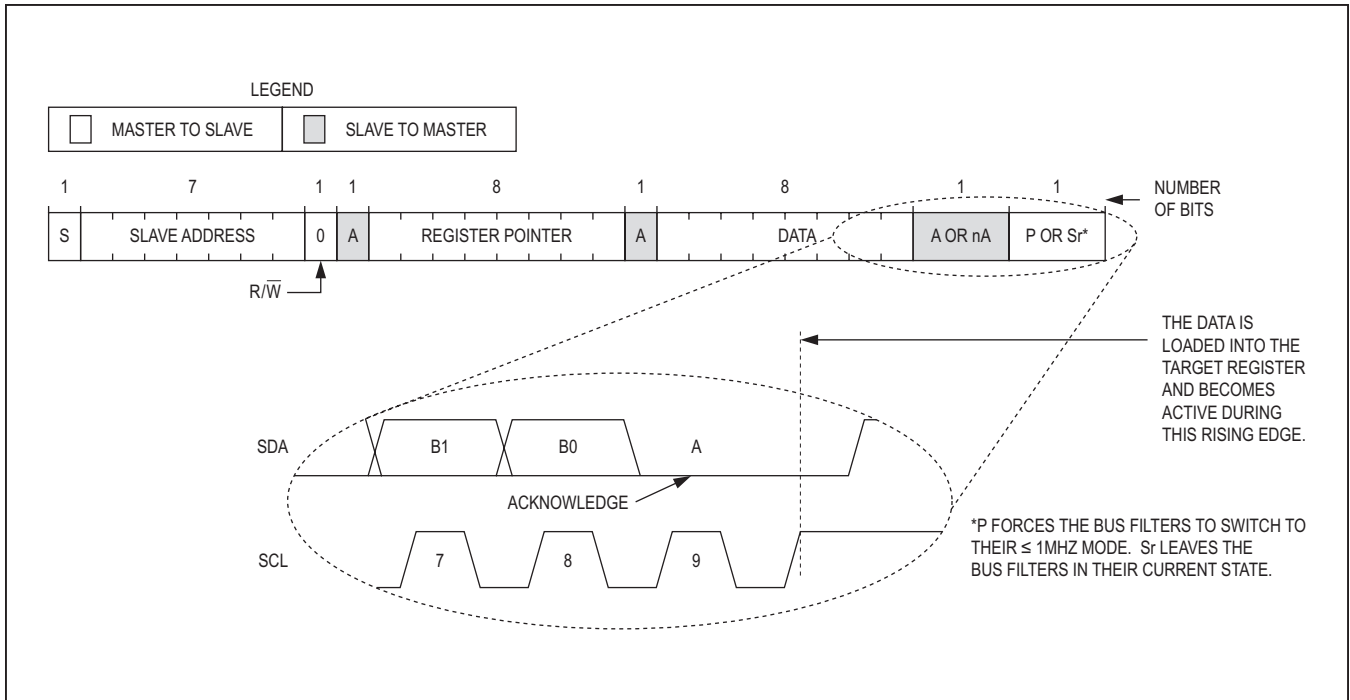


Figure 9. Writing to a Single Register with the Write Byte Protocol

### Writing to Sequential Registers

Figure 10 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol, except the master continues to write after it sends the first byte of data. When the master is done writing, it issues a stop (P) or repeated start (Sr). This protocol is recommended when configuring the device during initialization. The writing to sequential registers protocol is as follows:

- 1) The master sends a start command (S).
- 2) The master sends the 7-bit slave address followed by a write bit (R/W=0).
- 3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 4) The master sends an 8-bit register pointer.
- 5) The slave acknowledges the register pointer.
- 6) The master sends a data byte.
- 7) The slave acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
- 8) Steps 6 to 7 are repeated as many times as the master requires.
- 9) During the last acknowledge related clock pulse, the master may issue an acknowledge or a not-acknowledge.
- 10) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a repeated start leaves the bus input filters in their current state.



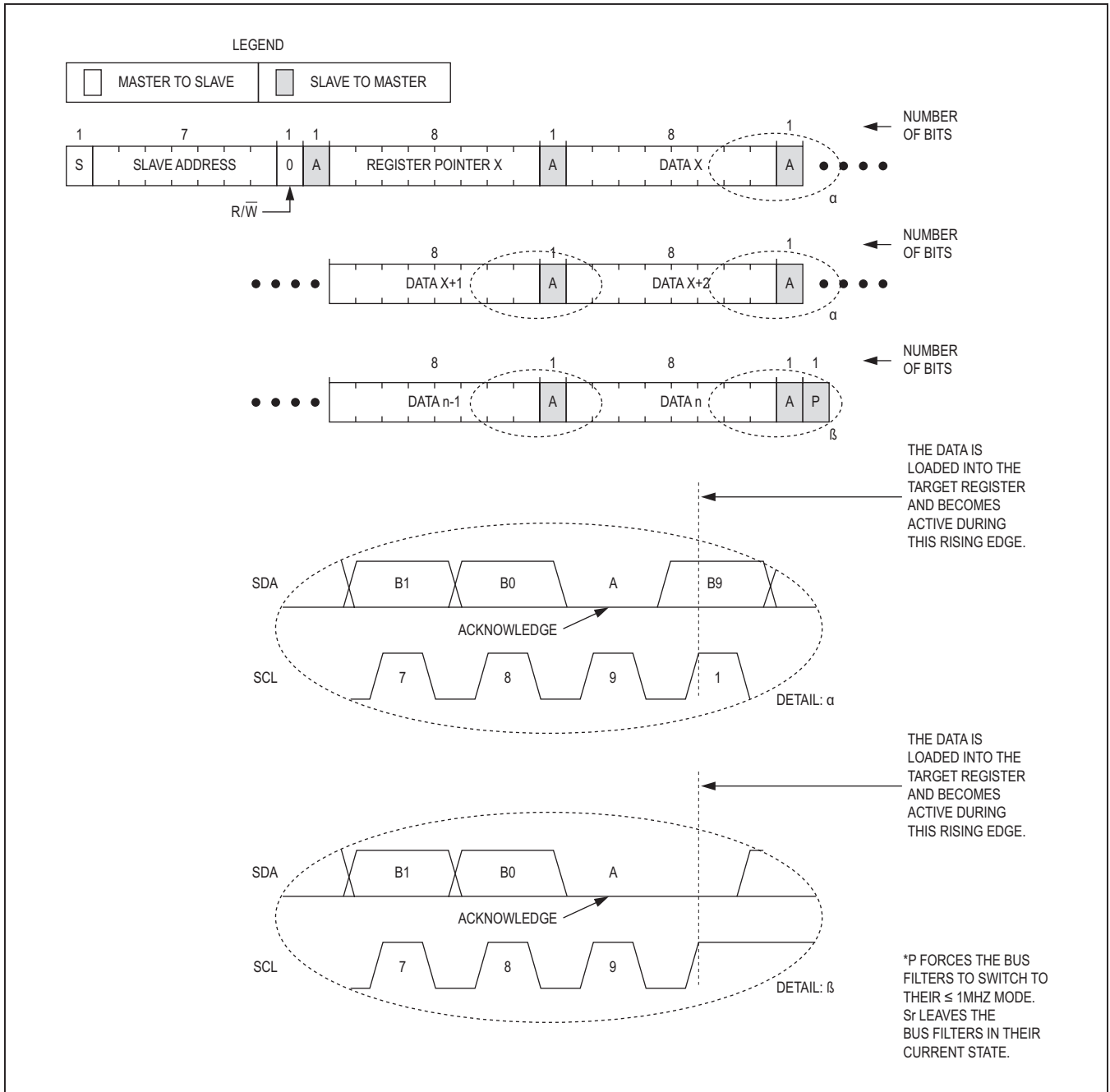


Figure 10. Writing to Sequential Registers X to N

### Writing Multiple Bytes Using Register-Data Pairs

Figure 11 shows the protocol for the I<sup>2</sup>C master device to write multiple bytes to the MAX8973A using register-data pairs. This protocol allows the I<sup>2</sup>C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a stop condition. The multiple byte register-data pair protocol is as follows:

- 1) The master sends a start (S) command.
- 2) The master sends the 7-bit slave address followed by a write bit ( $R/\overline{W} = 0$ ).
- 3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 4) The master sends an 8-bit register pointer.
- 5) The slave acknowledges the register pointer.
- 6) The master sends a data byte.
- 7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
- 8) Steps 5 to 7 are repeated as many times as the master requires.
- 9) The master sends a stop (P) condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

### Reading from a Single Register

Figure 12 shows the protocol for the I<sup>2</sup>C master device to read one byte of data to the MAX8973A. This protocol is the same as the SMBus specification's read byte protocol. The read byte protocol is as follows:

- 1) The master sends a start (S) command.
- 2) The master sends the 7-bit slave address followed by a write bit ( $R/\overline{W} = 0$ ).
- 3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 4) The master sends an 8-bit register pointer.
- 5) The slave acknowledges the register pointer.
- 6) The master sends a repeated start (Sr) command.
- 7) The master sends the 7-bit slave address followed by a read bit ( $R/\overline{W} = 1$ ).
- 8) The addressed slave asserts an acknowledge by pulling SDA low.
- 9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- 10) The master issues a not-acknowledge (nA).
- 11) The master sends a stop condition (P) or a repeated start (Sr) condition. Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an repeated start leaves the bus input filters in their current state.

Note that every time the MAX8973A receives a stop (P), its register pointer is set to 0x00. If reading register 0x00 after a stop (P) has been issued, steps 1 to 6 in the above algorithm can be skipped.

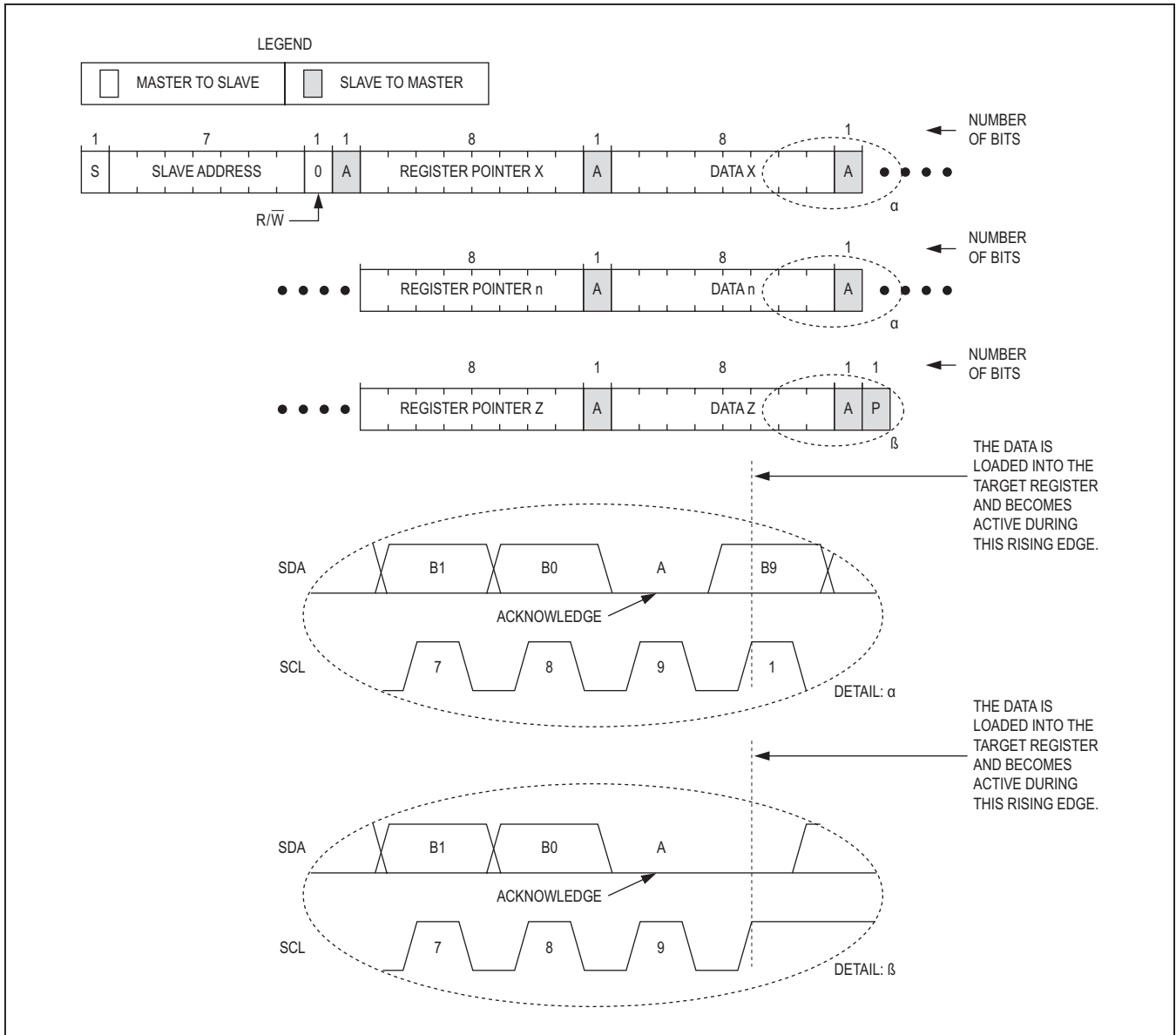


Figure 11. Writing to Multiple Registers with the Multiple Byte Register Data Pair Protocol

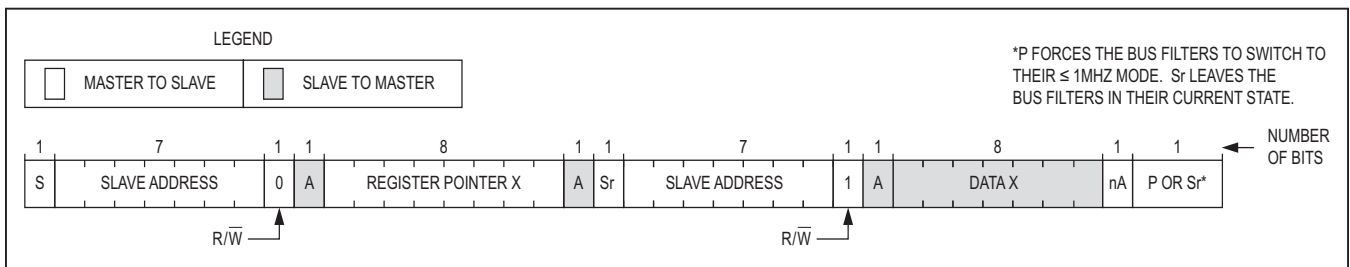


Figure 12. Reading from a Single Register with the Read Byte Protocol

### Reading from Sequential Registers

Figure 13 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data—when the master has all the data it requires it issues a not-acknowledge (nA) and a stop (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

- 1) The master sends a start (S) command.
- 2) The master sends the 7-bit slave address followed by a write bit ( $R/\bar{W} = 0$ ).
- 3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 4) The master sends an 8-bit register pointer.
- 5) The slave acknowledges the register pointer.
- 6) The master sends a repeated start (Sr) command.
- 7) The master sends the 7-bit slave address followed by a read bit ( $R/\bar{W} = 1$ ). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.

- 8) The addressed slave asserts an acknowledge (A) by pulling SDA low.
- 9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- 10) The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
- 11) Steps 9 and 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
- 12) The master sends a stop (P) condition or a repeated start (Sr) condition. Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that every time the MAX8973A receives a stop (P), its register pointer is set to 0x00. If reading register 0x00 after a stop has been issued, steps 1 to 6 in the above algorithm can be skipped.

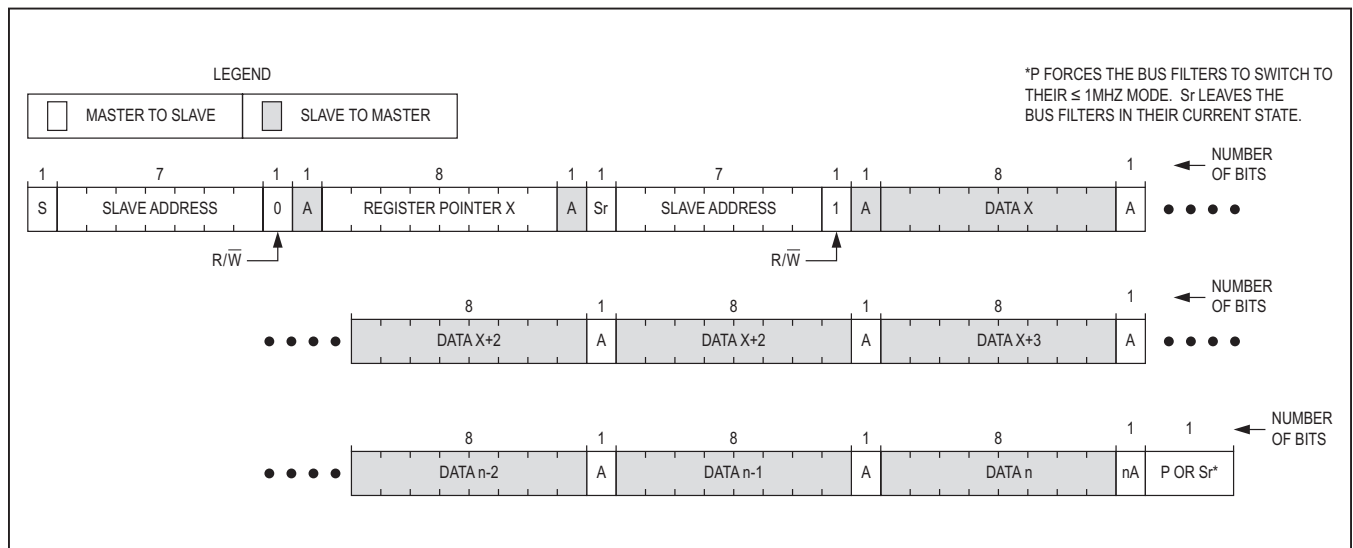


Figure 13. Reading Continuously from Sequential Registers X to N

**Engaging HS Mode for Operation up to 3.4MHz**

Figure 14 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz. The engaging HS-mode protocol is as follows:

- 1) Begin the protocol while operating at a bus speed of 1MHz or lower
- 2) The master sends a start command (S).
- 3) The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
- 4) The addressed slave issues a not acknowledge (nA).
- 5) The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation.

**I<sup>2</sup>C Watchdog Timer (WDTMR)**

The MAX8973A features a 35ms watchdog timer that resets the I<sup>2</sup>C state machine in the event that the I<sup>2</sup>C bus gets hung. The I<sup>2</sup>C watchdog timer is enabled by writing a 1 to the WDTMR bit in the CONTROL2 register.

When the I<sup>2</sup>C watchdog timer is enabled, an I<sup>2</sup>C START command begins the timer, a falling edge of SCL clears the I<sup>2</sup>C watchdog timer, and an I<sup>2</sup>C STOP command resets and disables the timer.

**Component Selection**

**Input Capacitance**

The MAX8973A requires a 10µF input bypass capacitor for each phase. Each input capacitor must be placed as close as possible to the device. Each input capacitor case size should be 0603 (EIA)/1608 (metric) or larger to provide adequate effective capacitance and to allow LX traces to be routed under the input capacitors. Phase A is

bypassed from INAB (bump A5) to PGAC (bumps B7 and C7). Phase B is bypassed from INAB (bump A4) to PGB (bumps A1, B1, and B2). Phase C is bypassed from INC (bumps D4 and D5) to PGAC (bumps B7 and C7).

**Output Capacitance**

The MAX8973A requires local output capacitance in order to stabilize the converter and to limit the amplitude of output droop and soar during load transients and load release. Use the following equation to calculate the absolute minimum output capacitance per phase required to limit the voltage droop during load transient events:

$$C_{OUT} \geq \frac{(L \times (I_{STEP}^2))}{(2 \times V_{DROOP} \times (V_{IN} - V_{OUT}))}$$

Where C<sub>OUT</sub> = effective output capacitance per phase, L = inductance per phase, I<sub>STEP</sub> = transient load step per phase, V<sub>DROOP</sub> = voltage droop during load step, V<sub>IN</sub> = input voltage, and V<sub>OUT</sub> = output voltage. This formula calculates the minimum theoretical capacitance required for an infinitely fast converter. For most designs, an effective capacitance per phase 50% greater than the calculated value should suffice.

Use the following equation to calculate output voltage soar during load release:

$$V_{SOAR} = \frac{(L \times (I_{STEP}^2))}{(2 \times C_{OUT} \times V_{OUT})}$$

An 0805 (EIA)/2012 (metric) 22µF X5R capacitor for each phase is recommended at a minimum, regardless of load step amplitude. Additional output capacitance may be placed at the point of load to further improve transient response. If remote capacitance is installed, ensure that the total local output capacitance is at least 2x the total remote capacitance to ensure that the MAX8973A's control loop is not adversely affected by the remote capacitance.

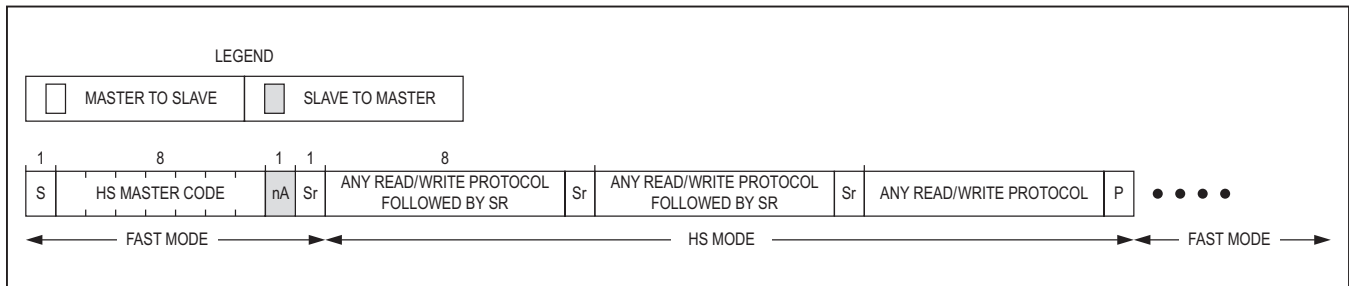


Figure 14. Engaging HS Mode

**Inductors**

The MAX8973A control loop is influenced by the inductance and DCR of the inductor. Each MAX8973A version is factory-tuned for a particular inductance and DCR, where the DCR is considered to be the inductor's DCR plus the trace resistance from inductor to the output capacitor for each phase. It is highly recommended that the inductance and DCR does not deviate from the recommendations in the data sheet. [Table 8](#) lists the inductor parameters for each MAX8973A version. Refer to the MAX8973EV Kit for a list of recommended inductors.

The MAX8973A does not actively match inductor currents. Inductor current matching between phases is largely determined by how well the DCR of the inductors match each other.

Saturation current and temperature rise current ratings for the inductor should also be considered. Ensure that the inductor's saturation current rating meets or exceeds the maximum value for the peak current limit in the [Electrical Characteristics](#) table. Ensure that the temperature rise current rating for the inductor exceeds the maximum expect RMS output current from the MAX8973A.

**Selection Guide****Table 11. MAX8973\_ Selection Guide**

PART NUMBER	PARAMETER							
	I <sub>OUT_MAX</sub>	DEFAULT V <sub>OUT</sub>	DEFAULT V <sub>OUT_DVS</sub>	L <sub>IDEAL</sub>	DCR	SOFT-START/STOP RAMP RATE	DVS SLEW RATE	I <sup>2</sup> C SLAVE ADDRESS
MAX8973A	9A	1.0V	1.2V	0.68μH	27mΩ	20mV/μs	50mV/μs	0x36/0x37

**Registers****Register Map**

REGISTER ADDRESS	REGISTER NAME	DEFAULT CONTENTS	BIT7 (MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0 (LSB)
0x00h	VOUT	0x3Fh	EN	VOUT[6:0]						
0x01h	VOUT_DVS	0xDFh	RSVD	VOUT_DVS[6:0]						
0x02h	CONTROL1	0x02h	SNSEN	FPWM_EN	FSR_EN	AD_EN	BIASEN	FREQ SHIFT	RAMP [1:0]	
0x03h	CONTROL2	0x1Dh	RSVD	WDTMR	ENPD_EN	RSVD	CKADV [1:0]		INDUCTOR [1:0]	
0x04h	CHIPID1	0x80h	DIETYPE[7:0]							
0x05h	CHIPID2	0x14h	DASH[3:0]				MASK REV[3:0]			

**Register Details****VOUT Register**

Register Name	VOUT
Address	0x00h
Reset Value	MAX8973A: 0x3Fh
Type	Read/write
Special Features	Reset upon V <sub>CC</sub> UVLO or thermal shutdown

BIT	NAME	DESCRIPTION	DEFAULT
7	EN	<b>Converter Enable (Logically OR'd with EN Pin)</b> 0 = Converter is off 1 = Converter is on	0b0
6:0	VOUT [6:0]	<b>Output Voltage Selection</b> 0x00 = 0.60625V 0x01 = 0.61250V 0x0F = 0.70000V 0x1F = 0.80000V 0x3F = 1.00000V 0x47 = 1.05000V 0x5F = 1.20000V 0x7F = 1.40000V	0b011 1111 (1.0V) (MAX8973A)

**VOUT\_DVS Register**

Register Name	VOUT_DVS
Address	0x01h
Reset Value	MAX8973A: 0xDFh
Type	Read/write
Special Features	Reset upon V <sub>CC</sub> UVLO or thermal shutdown

BIT	NAME	DESCRIPTION	DEFAULT
7	RSVD	Reserved	0b1
6:0	VOUT_DVS [6:0]	<b>Output Voltage Selection</b> 0x00 = 0.60625V 0x01 = 0.61250V 0x0F = 0.70000V 0x1F = 0.80000V 0x3F = 1.00000V 0x47 = 1.05000V 0x5F = 1.20000V 0x7F = 1.40000V	0b101 1111 (1.2V) (MAX8973A)



**CONTROL1 Register**

Register Name	CONTROL1
Address	0x02h
Reset Value	MAX8973A: 0x02h
Type	Read/write
Special Features	Reset upon $V_{CC}$ UVLO or thermal shutdown

BIT	NAME	DESCRIPTION	DEFAULT
7	SNS_EN	<b>Remote Sense Enable</b> 0 = Remote Sense Circuit Disabled. 1 = Remote Sense Circuit Enabled.	0b0
6	FPWM_EN	<b>Forced PWM Mode Enable</b> 0 = Automatic transition from Skip Mode to PWM mode with change in load current. 1 = Forced PWM mode under all load conditions.	0b0
5	$\overline{\text{FSR\_EN}}$	<b>Active-Low Falling Slew Rate Enable</b> 0 = The slew rate control circuit is active when the output voltage is decreased. The desired regulation voltage is decreased at a rate set by RAMP[1:0] and forced PWM mode is enabled so that negative inductor current can be used to pull energy out of the output capacitor. 1 = The slew rate control circuit is disabled when the output voltage is decreased. The desired regulation voltage is decreased at a rate set by RAMP[1:0], but it is up to the external load to drain energy from the output capacitor in order to pull down on the output voltage.	0b0
4	AD_EN	<b>Output Active Discharge Enable</b> 0 = 100 $\Omega$ discharge resistance is disabled when EN is low. 1 = 100 $\Omega$ discharge resistance is enabled when EN is low.	0b0
3	BIASEN	Enables step-down regulator bias to reduce the time delay to begin the output voltage ramp. The BIASEN bit is logically OR'd with the BIASEN pin. 0 = REF, BIAS, etc. off when buck is disabled. Startup delay is 240 $\mu$ s (typ). 1 = REF, BIAS, etc. on when buck is disabled. Startup delay is 20 $\mu$ s (typ).	0b0
2	FREQSHIFT	<b>Frequency Shift</b> 0 = 2MHz (typ) switching frequency per phase in CCM and FPWM modes. 1 = 1.82MHz (typ) switching frequency per phase in CCM and FPWM modes.	0b0
1:0	RAMP[1:0]	<b>Slew Rate Selection</b> 00 = Sets startup/softstop slew rate = 20mV/ $\mu$ s and DVS slew rate = 12.5mV/ $\mu$ s 01 = Sets startup/softstop slew rate = 20mV/ $\mu$ s and DVS slew rate = 25mV/ $\mu$ s 10 = Sets startup/softstop slew rate = 20mV/ $\mu$ s and DVS slew rate = 50mV/ $\mu$ s 11 = Sets startup/softstop slew rate = 200mV/ $\mu$ s and DVS slew rate = 200mV/ $\mu$ s	0b10

**CONTROL2 Register**

Register Name	CONTROL2
Address	0x03h
Reset Value	MAX8973A: 0x1Dh
Type	Read/write
Special Features	Reset upon V <sub>CC</sub> UVLO or thermal shutdown

BIT	NAME	DESCRIPTION	DEFAULT
7	RSVD	Reserved	0b0
6	WDTMR	<b>I<sup>2</sup>C Watchdog Timer Enable</b> 0 = SCL watchdog timer is disabled. 1 = SCL watchdog timer is enabled with a 35ms period. An I <sup>2</sup> C START (S) condition starts the timer. A falling edge of SCL clears the watchdog timer. An I <sup>2</sup> C STOP (P) condition stops and resets the timer.	0b0
5	$\overline{\text{ENPD\_EN}}$	<b>Active-Low Enable for EN Pulldown Resistance</b> 0 = 500k $\Omega$ pulldown resistance from EN to AGND is enabled. 1 = 500k $\Omega$ pulldown resistance from EN to AGND is disabled.	0b0
4	RSVD	Reserved	0b1
3:2	CKADV[1:0]	<b>Enhanced Transient Response Enable and Sensitivity Selection</b> 00 = Enhanced transient response circuit is enabled and set for high sensitivity. 75mV/ $\mu$ s output slew rate triggers the ETR response. 01 = Enhanced transient response circuit is enabled and set for low sensitivity. 150mV/ $\mu$ s output slew rate triggers the ETR response. 10 = Enhanced transient response circuit is enabled and set for high sensitivity. 75mV/ $\mu$ s output slew rate triggers the ETR response. 11 = Enhanced transient response circuit is disabled.	0b11
1:0	INDUCTOR [1:0]	<b>Slope Compensation Adjustment and RCS Gain for Inductor DCR Sensing</b> 00 = Slope Compensation and RCS = Nominal -30% 01 = Nominal 10 = Slope Compensation and RCS = Nominal + 30% 11 = Slope Compensation and RCS = Nominal + 60%	0b01

**CHIPID1 Register**

Register Name	CHIPID1
Address	0x04h
Reset Value	0x80h
Type	Read only
Special Features	Read only

BIT	NAME	DESCRIPTION	DEFAULT
7:0	DIETYPE [7:0]	Die type	0b1000 0000

**CHIPID2 Register**

Register Name	CHIPID2
Address	0x05h
Reset Value	0x14h
Type	Read only
Special Features	Read only

BIT	NAME	DESCRIPTION	DEFAULT
7:4	DASH[3:0]	0001 = MAX8973A	0b0001
3:0	RSVD	Reserved	0b0100

**PCB Layout Guideline**

The MAX8973A WLP package and bump configuration allows for a small total PCB area. The following recommendations for PCB layout are provided to minimize PCB area and to provide optimal performance from the MAX8973A. Careful PCB layout is important for minimizing ground bounce and noise. [Figure 15](#) is an example layout showing the critical power components for the MAX8973A. The arrangement of components not shown in [Figure 15](#) is less critical. Refer to the MAX8973A EV Kit for a complete PCB layout example. Use the following list of guidelines in addition to [Application Note 1891: Wafer-Level Packaging \(WLP\) and its Applications \(\[www.maximintegrated.com/ucsp\]\(http://www.maximintegrated.com/ucsp\)\)](#) to layout the MAX8973A PCB.

The following guidelines are arranged in terms of priority from most critical to least critical:

- 1) Place CINA as close to INAB and PGAC as possible. Place CINB as close to INAB and PGB as possible. Place CINC as close to INC and PGAC as possible. Each phase's input capacitor delivers a high di/dt current pulse when the high-side MOSFET turns on. It is essential that parasitic inductance in the power input traces be minimized for high efficiency and reliability.
- 2) Minimize the trace length from each phase's output capacitor GND terminal to the input capacitor's GND

terminal for that same phase. This minimizes the area of the current loop when the high-side MOSFET is conducting. Keep all sensitive signals, such as feedback nodes outside of these current loops with as much isolation as your design allows.

- 3) Minimize the trace impedance from LX\_ to each phase's inductor and from each inductor to the output capacitor for each phase. This minimizes the area of each current loop and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency. Keep all sensitive signals, such as feedback nodes outside of these current loops and away from the LX switching voltage with as much isolation as your design allows.
- 4) Create a PGND plane on the 2nd layer of the PCB immediately below the power components and bumps carrying high switching currents. This reduces parasitic inductance in the traces carrying high currents and shields signals on inner PCB layers from the switching waveforms on the top layer of the PCB.
- 5) Connect the feedback terminal (OUT) to the local output capacitors for Phase A and Phase C. The OUT connection to the local output capacitors should be placed as close to the MAX8973A as possible to minimize the effects of voltage drop in the output trace connected to the load.

- 6) Place the  $V_{CC}$  bypass capacitor as close to the MAX8973A as possible. Noise coupling into  $V_{CC}$  may disturb the reference and bias circuitry of the MAX8973A if this capacitor is installed away from the device.
- 7) Create a small AGND island for the  $V_{CC}$  and  $V_{DD}$  bypass capacitors. Connect this AGND island to the MAX8973A PGND plane for Phase A and Phase C, between the PGND terminals of the Phase A and Phase C output capacitors. This results in the most accurate sensing of the output voltage by the local feedback loop (OUT to AGND).
- 8) Each of the MAX8973A bumps has approximately the same ability to remove heat from the die. Connect as much metal as possible to each bump to minimize the  $\theta_{JA}$  associated with the MAX8973A.
- 9) Connect the power output of each phase together on a power plane with as many vias as practical to minimize trace impedance.

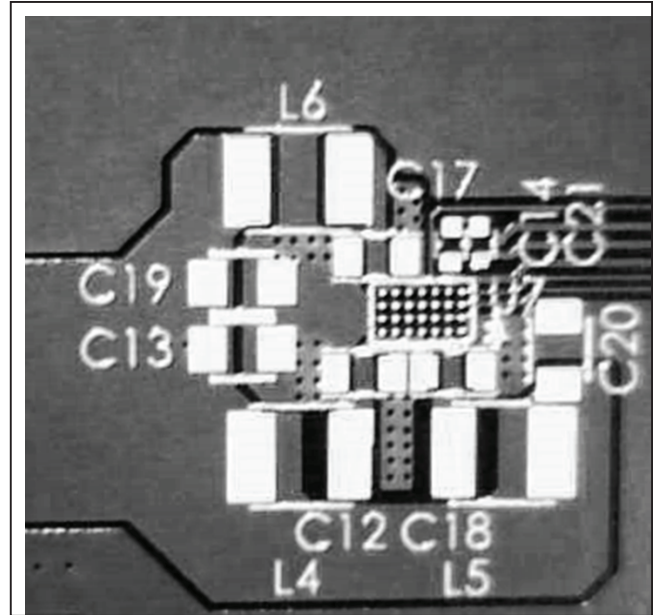
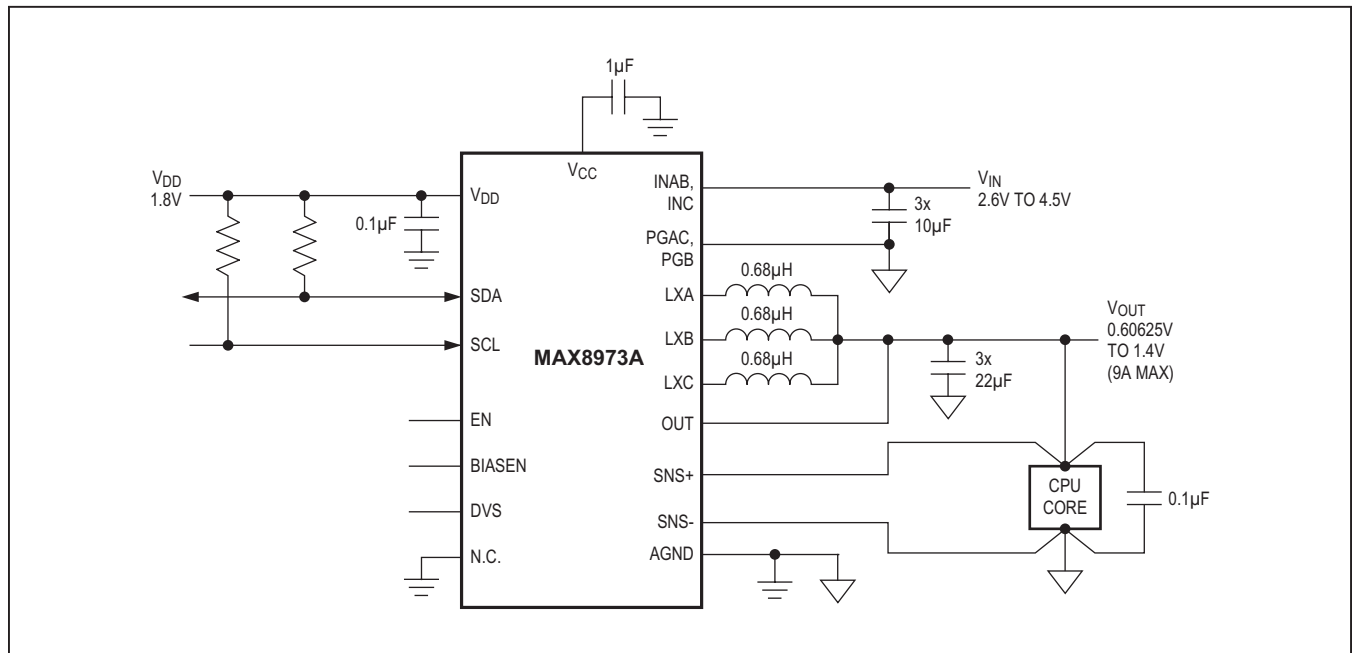


Figure 15. MAX8973\_ EVKIT Layout Recommendation

Typical Operating Circuit



Ordering Information

PART	DEFAULT V <sub>OUT</sub>	I <sub>OUT,MAX</sub>	PIN-PACKAGE
MAX8973AEWI+T	1.0V/1.2V	9A	28 WLP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 WLP	W282B3+1	<a href="#">21-0627</a>	<a href="#">Refer to Application Note 1891</a>

**COMMON DIMENSIONS**

A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.025 BASIC
b	0.27 ±0.03
D1	1.20
E1	2.40
e	0.40 BASIC
SD	0.20 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W282B3+1	3.20	3.23	2.00	2.03	NONE

**NOTES:**

- Terminal pitch is defined by terminal center to center value.
- Outer dimension is defined by center lines between scribe lines.
- All dimensions in millimeter.
- Marking shown is for package orientation reference only.
- Tolerance is ± 0.02 unless specified otherwise.
- All dimensions apply to PbFree (+) package codes only.
- Front - side finish can be either Black or Clear.

**MARKING**

1  
A+  
AAAA

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

$\phi \ 0.05 \ (M) \ (S) \ AB$

- DRAWING NOT TO SCALE -

**maxim integrated**

TITLE: PACKAGE OUTLINE, 28 BUMPS WLP Pkg. 0.40MM PITCH

APPROVAL: DOCUMENT CONTROL NO. 21-0627 REV. A 1/1

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/13	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

*Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*