

## DAC38RFxx: Dual- or Single-Channel, Single-Ended, 14-bit, 9-GSPS, RF-Sampling DAC with JESD204B Interface and On-Chip GSM PLL

### 1 Features

- 14-Bit Resolution
- Maximum DAC Sample Rate: 9 GSPS
- Key Specifications:
  - RF Full Scale Output Power at 2.1 GHz: 0 dBm
  - Spectral Performance
    - $f_{DAC} = 5898.24$  MSPS,  $f_{OUT} = 2.14$  GHz
      - WCDMA ACLR: 73 dBc
      - WCDMA alt-ACLR: 77 dBc
    - $f_{DAC} = 8847.36$  MSPS,  $f_{OUT} = 3.7$  GHz
      - 20 MHz LTE ACLR: 66 dBc
    - $f_{DAC} = 9$  GSPS,  $f_{OUT} = 1.8$  GHz
      - IMD3 = 70 dBc (–6 dBFS, 10 MHz tone spacing)
      - NSD = –157 dBc/Hz
- Dual-Band Digital Upconverter per DAC
  - Max Input Rate: 1 Band: 1250 MSPS  
Complex, 2 bands: 625 MSPS Complex Each
  - 6, 8, 10, 12, 16, 18, 20 or 24x Interpolation
  - 4 Independent NCOs with 48-Bit Resolution
- JESD204B Interface
  - Subclass 1 Support for Multi-chip Synchronization
  - Maximum Lane Rate: 12.5 Gbps
- Single-Ended Output with Integrated Balun Covering 700–3800 MHz
- Internal PLL and VCO with Bypass
  - DAC38RF86/96:  $f_{C(VCO)} = 8.9$  GHz
  - DAC38RF87/97:  $f_{C(VCO)} = 5.9$  GHz
- Power Dissipation: 1.4 – 2.2 W/ch
- Power Supplies: –1.8 V, 1.0 V, 1.8 V
- Package: 10 x 10 mm BGA, 0.8 mm Pitch, 144-Balls

### 2 Applications

- Wireless Communications
- Radar
- Communications Test Equipment
- Arbitrary Waveform Generators
- Military Software Defined Radio
- Satellite Communications (SATCOM)

### 3 Description

The DAC38RFxx is a family of high-performance, dual/single-channel, 14-bit, 9-GSPS, RF-sampling digital-to-analog converters (DACs) that are capable of synthesizing wideband signals from 0 to 4.5 GHz. A high dynamic range allows the DAC38RFxx family to generate 3G/4G signals for wireless basestations with an output frequency up to 4 GHz.

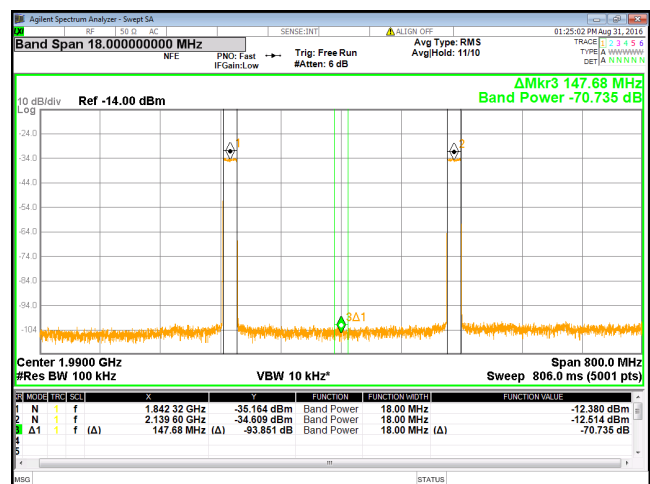
The devices feature a low-power JESD204B Interface with up to 8 lanes, and provides a maximum bit rate of 12.5 Gbps and input sample rate of 1.25 GSPS complex per channel. The DAC38RFxx provides two digital upconverters per DAC, with multiple interpolation rates and a digital quadrature modulator with independent, frequency flexible NCOs. An optional low-jitter PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency reference clock.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC38RF86	FCBGA (144)	10.0 mm x 10.0 mm
DAC38RF96		
DAC38RF87		
DAC38RF97		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### 2x20 MHz LTE at 1.84 GHz and 2.14 GHz, 800 MHz Span



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>59</b>
<b>2 Applications</b> .....	<b>1</b>	8.5 Register Maps .....	<b>62</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>125</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information .....	<b>125</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	9.2 Typical Application: Multi-band Radio Frequency Transmitter .....	<b>126</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>130</b>
<b>7 Specifications</b> .....	<b>7</b>	10.1 Power Supply Sequencing .....	<b>131</b>
7.1 Absolute Maximum Ratings .....	<b>7</b>	<b>11 Layout</b> .....	<b>132</b>
7.2 ESD Ratings .....	<b>7</b>	11.1 Layout Guidelines .....	<b>132</b>
7.3 Recommended Operating Conditions .....	<b>7</b>	11.2 Layout Example .....	<b>134</b>
7.4 Thermal Information .....	<b>8</b>	<b>12 Device and Documentation Support</b> .....	<b>135</b>
7.5 Electrical Characteristics - DC Specifications .....	<b>8</b>	12.1 Related Links .....	<b>135</b>
7.6 Electrical Characteristics - Digital Specifications ....	<b>11</b>	12.2 Receiving Notification of Documentation Updates .....	<b>135</b>
7.7 Electrical Characteristics - AC Specifications .....	<b>14</b>	12.3 Community Resources .....	<b>135</b>
7.8 Timing Requirements .....	<b>17</b>	12.4 Trademarks .....	<b>135</b>
7.9 Typical Characteristics .....	<b>18</b>	12.5 Electrostatic Discharge Caution .....	<b>135</b>
<b>8 Detailed Description</b> .....	<b>23</b>	12.6 Glossary .....	<b>135</b>
8.1 Overview .....	<b>23</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>135</b>
8.2 Functional Block Diagrams .....	<b>23</b>		
8.3 Feature Description .....	<b>25</b>		

## 4 Revision History

DATE	REVISION	NOTES
February 2017	*	Initial release.

## 5 Device Comparison Table

Device	No. of Channels	Output	Interpolation	VCO Center Frequency
DAC38RF86	2	Single ended	6-24	VCO0 = VCO1 = 8.85 GHz
DAC38RF96	2		12-24	VCO0 = VCO1 = 8.85 GHz
DAC38RF87	2		6-24	VCO0 = VCO1 = 5.9 GHz
DAC38RF97	2		12-24	VCO0 = VCO1 = 5.9 GHz

## 6 Pin Configuration and Functions

AAV Package 144-Pin (FCBGA)  
 144-Pin FCBGA  
 Top View

	A	B	C	D	E	F	G	H	J	K	L	M	
12	DACCLKSE	VSSCLK	AGND	AGND	VOUT2	AGND	VDDOUT18	VDDOUT18	AGND	VOUT1	AGND	AGND	12
11	VSSCLK	VSSCLK	AGND	AGND	AGND	VDDA1	VDDA18	VDDA18	VDDA1	AGND	AGND	AGND	11
10	DACCLK+	VDDAPLL18	EXTIO	VEE18N	VEE18N	VSSCLK	VDDL2_1	VDDL2_1	VSSCLK	VEE18N	VEE18N	SDIO	10
9	DACCLK-	VDDAPLL18	RBIAS	VDDAVCO18	VDDAVCO18	VSSCLK	VDDCLK1	VDDCLK1	VSSCLK	RESET\	SCLK	SDO	9
8	VSSCLK	VSSCLK	ATEST	VDDPLL1	VDDPLL1	VSSCLK	VDDL1_1	VDDL1_1	VSSCLK	ALARM	SLEEP	SDEN\	8
7	CLKTX+	VDDTX18	SYNC1+	VDDDIG1	DGND	VDDE1	DGND	VDDE1	DGND	GPI0	GPO0	GPI1	7
6	CLKTX-	VDDTX1	SYNC1-	DGND	VDDDIG1	DGND	VDDE1	DGND	VDDE1	TXENABLE	GPO1	DGND	6
5	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDIO18	TRST\	TMS	DGND	RX3+	5
4	SYSREF-	VDDS18	SYNC0+	VSENSE	VDDDIG1	VDDDIG1	VDDDIG1	TDI	TDO	TCLK	DGND	RX3-	4
3	SYSREF+	VDDS18	SYNC0-	IFORCE	VDDDIG1	AMUX1	AMUX0	VDDT1	VDDT1	TESTMODE	DGND	RX2-	3
2	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDR18	VDDR18	DGND	DGND	RX2+	2
1	RX7+	RX7-	RX6-	RX6+	RX5+	RX5-	RX4-	RX4+	RX0+	RX0-	RX1-	RX1+	1
	A	B	C	D	E	F	G	H	J	K	L	M	

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	C11, C12, D11, E11, F12, J12, K11, L11, M11, M12, D12, L12	-	Analog ground.
ALARM	K8	O	CMOS output for ALARM condition. The ALARM output functionality is defined through the config7 register. Default polarity is active low, but can be changed to active high via config0 alarm_out_pol control bit.
AMUX0	G3	O	Analog test pin for SerDes, Lane 0 to Lane 3. Can be left floating.
AMUX1	F3	O	Analog test pin for SerDes, Lane 4 to Lane 7. Can be left floating.
ATEST	C8	O	Analog test pin for DAC, references and PLL. Can be left floating.
CLKTX+	A7	O	Divided output clock, self-biased, positive terminal.
CLKTX-	A6	O	Divided output clock, self-biased, negative terminal.
DACCLK+	A10	I	Device clock, self-biased, positive terminal.
DACCLK-	A9	I	Device clock, self-biased, negative terminal.
DACCLKSE	A12	I	Single ended device clock optional input. Can be left floating if not used.
DGND	A2, B2, C2, D2, D6, E2, E7, F2, F6, G2, G7, H6, J7, K2, L2, L3, L4, L5, M6	-	Digital ground.
EXTIO	C10		Requires a 0.1 $\mu$ F decoupling capacitor to AGND.
GPI0	L6		Factory use only. User should GND.
GPI1	M7		Factory use only. User should GND.
GPO0	L7		Used for CMOS SYNC0\ signal.
GPI01	K7		Used for CMOS SYNC1\ signal.
IFORCE	D3		Test pin for on chip parametrics. Can be left floating.
RBIAS	C9	I/O	Full-scale output current bias. Change the full-scale output current through DACFS in register DACFS (8.5.72). Expected to be 3.6 k $\Omega$ to GND for 40 mA full scale output.
$\overline{\text{RESET}}$	K9	I	Active low input for chip RESET, which resets all the programming registers to their default state. Internal pull-up.
RX0+	J1	I	CML SerDes interface lane 0 input, positive
RX0-	K1	I	CML SerDes interface lane 0 input, negative
RX1+	M1	I	CML SerDes interface lane 1 input, positive
RX1-	L1	I	CML SerDes interface lane 1 input, negative
RX2+	M2	I	CML SerDes interface lane 2 input, positive
RX2-	M3	I	CML SerDes interface lane 2 input, negative
RX3+	M5	I	CML SerDes interface lane 3 input, positive
RX3-	M4	I	CML SerDes interface lane 3 input, negative
RX4+	H1	I	CML SerDes interface lane 4 input, positive
RX4-	G1	I	CML SerDes interface lane 4 input, negative
RX5+	E1	I	CML SerDes interface lane 5 input, positive
RX5-	F1	I	CML SerDes interface lane 5 input, negative
RX6+	D1	I	CML SerDes interface lane 6 input, positive
RX6-	C1	I	CML SerDes interface lane 6 input, negative
RX7+	A1	I	CML SerDes interface lane 7 input, positive
RX7-	B1	I	CML SerDes interface lane 7 input, negative
SCLK	L9	I	Serial interface clock. Internal pull-down.
$\overline{\text{SDEN}}$	M8	I	Active low serial data enable, always an input to the DAC38RFxx. Internal pull-up.
SDIO	M10	I/O	Serial interface data. Bi-directional in 3-pin mode (default) and uni-directional input 4-pin mode. Internal pull-down.
SDO	M9	O	Uni-directional serial interface data output in 4-pin mode. The SDO pin is tri-stated in 3-pin interface mode (default).
SLEEP	L8	I	Active high asynchronous hardware power-down input. Internal pull-down.
$\overline{\text{SYNC0+}}$	C4	O	Synchronization request to transmitter for JESD204B link 0, LVDS positive output.
$\overline{\text{SYNC0-}}$	C3	O	Synchronization request to transmitter for JESD204B link 0, LVDS negative output.
$\overline{\text{SYNC1+}}$	C7	O	Synchronization request to transmitter for JESD204B link 1, LVDS positive output.

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SYNC1-	C6	O	Synchronization request to transmitter for JESD204B link 1, LVDS negative output.
SYSREF+	A3	I	LVPECL SYSREF positive input. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used for multiple DAC synchronization.
SYSREF-	A4	I	LVPECL SYSREF negative input. (See the SYSREF description)
TCLK	K4	I	JTAG test clock. Internal pull-down
TDI	H4	I	JTAG test data in. Internal pull-up
TDO	J4	O	JTAG test data out. Internal pull-up
TESTMODE	K3	I	This pin is used for factory testing. Recommended to connect to ground.
TMS	K5	I	JTAG test mode select. Internal pull-up
TRST	J5	I	JTAG test reset. Must be connected to ground if not used. Internal pull-up
TXENABLE	K6	I	Transmit enable active high input. Internal pull-down. To enable analog output data transmission, pull the CMOS TXENABLE pin to high. To disable analog output, pull CMOS TXENABLE pin to low. The DAC output is forced to midscale.
VDDA1	F11, J11	I	Analog 1V supply voltage.
VDDA18	G11, H11	I	Analog 1.8V supply voltage. (1.8 V)
VDDPLL1	D8, E8	I	Analog 1V supply for PLL.
VDDAPLL18	B9, B10	I	PLL analog supply voltage. (1.8 V)
VDDAVCO18	D9, E9	I	Analog supply voltage for VCO (1.8 V)
VDDCLK1	G9, H9	I	Internal clock buffer supply voltage (1 V) It is recommended to isolate this supply from VDDDIG1 and VDDA1.
VDDL1_1	G8, H8	I	DAC core supply voltage. (1 V)
VDDL2_1	G10, H10	I	DAC core supply voltage. (1 V)
VDDDIG1	A5, B5, C5, D5, D7, E3, E4, E5, E6, F4, F5, G4, G5	I	Digital supply voltage. (1 V) It is recommended to isolate this supply from VDDCLK1 and VDDA1.
VDDE1	F7, H7, G6, J6	I	Digital Encoder supply voltage (1 V). Must be separated from VDDDIG1 on new substrate device
VDDIO18	H5	I	Supply voltage for all digital I/O and CMOS I/O.
VDDOUT18	G12, H12	I	DAC supply voltage (1.8 V)
VDDR18	H2, J2	I	Supply voltage for SerDes. (1.8 V)
VDDS18	B3, B4	I	Supply voltage for LVDS SYNC0+/- and SYNC1+/- (1.8V)
VDDT1	H3, J3	I	Supply voltage for SerDes termination. (1 V)
VDDTX1	B6	I	Supply voltage for divided clock output. (1 V)
VDDTX18	B7	I	Supply voltage for divided clock output. (1.8 V)
VEE18N	D10, E10, K10, L10	I	Analog supply voltage. (-1.8 V)
VOUT1	K12	O	DAC channel 1 single ended output.
VOUT2	E12	O	DAC channel 2 single ended output.
VSENSE	D4	I	Test pin for on chip parametrics. Can be left floating.
VSSCLK	A8, A11, B8, B11, B12, F8, F9, F10, J8, J9, J10	-	Clock ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range <sup>(2)</sup>	VDDDAC1, VDDDIG1, VDDL1_1, VDDL2_1, VDDCLK1, VDDT1, VDDCLK1, VDDTX1, VDDE1	-0.3	1.3	V
	VDDR18, VDDIO18, VDDS18, VDDAPLL18, VDDOUT18, VDDA18, VDDAVCO18, VDDTX18	-0.3	2.45	V
	VEE18N	-2	-0.5	V
Voltage between AGND and DGND		-0.3	0.3	V
Pin Voltage Range <sup>(2)</sup>	RX[0..7]+/-	-0.5	VDDDIG1 + 0.5 V	V
	S $\overline{DEN}$ , SCLK, SDIO, SDO, TXENABLE, ALARM, RESET, SLEEP, TMS, TCLK, TDI, TDO, $\overline{TRST}$ , TESTMODE, GPIO, GP11, GPO0, GPO1	-0.5	VDDIO + 0.5 V	V
	CLKOUT+/-	-0.5	VDDTX18 + 0.5 V	V
	DACCLK+/-, SYSREF+/-, DACCLKSE	-0.5	VDDCLK1 + 0.5 V	V
	$\overline{SYNC0}$ +/-, $\overline{SYNC1}$ +/-	-0.5	VDDS18 + 0.5 V	V
	VOUT1+/-, VOUT2+/-	-0.5	VDDAOUT18 + 0.5 V	V
	RBIAS, EXTIO, ATEST	-0.5	VDDAOUT18 + 0.5 V	V
	IFORCE, VSENSE	-0.5	VDDDIG1 + 0.5 V	V
AMUX1, AMUX0	-0.5	VDDT1 + 0.5 V	V	
Peak input current (any input)			20	mA
Peak total input current (all inputs)		-30		mA
Junction temperature T <sub>J</sub>			150	°C
Operating free-air temperature, T <sub>A</sub>		-40	85	°C
Storage temperature, T <sub>sig</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Measured with respect to AGND or DGND.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T <sub>J</sub>	Recommended operating temperature			105	°C
	Maximum rated operating junction temperature <sup>(1)</sup>	125			°C
T <sub>A</sub>	Recommended free-air temperature	-40		85	°C

- (1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AAV (FCBGA)	UNIT
		144 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	25	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	1.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics - DC Specifications

Typical values at T<sub>A</sub> = 25°C, full temperature range is T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, nominal supplies, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC ACCURACY</b>					
Resolution		14			bits
<b>ANALOG OUTPUT</b>					
Full scale output signal current		10	30	40	mA
P <sub>(OUTFS)</sub> Full scale output power	50-Ω load 2.1 GHz output frequency		0		dBm
Output Compliance Range		1.3		2.3	V
<b>REFERENCE OUTPUT</b>					
V <sub>REF</sub> Reference output voltage			0.9		V
Reference output current			100		nA
<b>TEMPERATURE COEFFICIENTS</b>					
Reference voltage drift			±8		ppm/°C
<b>REFERENCE VOLTAGE DRIFT</b>					
VDDA18, VDDAPLL18, VDDS18, VDDIO18, VDDR18, VDDAPLL18, VDDOUT18, VDDAVCO18		1.71	1.8	1.89	V
VDDDIG1 VDDA1, VDDT1, VDDAPLL1, VDDCLK1, VDDL1_1, VDDL2_1, VDDTX1, VDDE1		0.95	1	1.05	V
VEE18N		-1.89	-1.8	-1.71	V
<b>POWER SUPPLY CURRENT AND CONSUMPTION</b>					
1 V Digital supplies: VDDDIG1			1478	2290	mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1510	1758	mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18	MODE 1: 2 TX, 1IQ/slice, LMFS = 8411, PLL on, 12x Interpolation, f <sub>INPUT</sub> = 737.28 MSPS, f <sub>DAC</sub> = 8847.36 MSPS, NCO's = 2.14 GHz, CLKTX Disabled		281	290	mA
-1.8 V Supply: VEE18N			159	180	mA
P <sub>DIS</sub> Power Dissipation			3779	4894	mW
1 V Digital supplies: VDDDIG1			1110		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1303		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18	MODE 2: 1 TX, 1IQ/slice, LMFS = 4211, PLL on, 12x Interpolation, f <sub>INPUT</sub> = 737.28 MSPS, f <sub>DAC</sub> = 8847.36 MSPS, NCO = 2.14 GHz, CLKTX Disabled		257		mA
-1.8 V Supply: VEE18N			159		mA
P <sub>DIS</sub> Power Dissipation			3162		mW



## Electrical Characteristics - DC Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , nominal supplies, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1V Digital supplies: VDDDIG1	MODE 3: 2 TX, 2 IQ/slice, LMFS = 8821, PLL on, 24x Interpolation, $f_{\text{INPUT}} = 368.64$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 1.84 GHz, NCO2 = 2.15 GHz, CLKTX Disabled		2253		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1522		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			280		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				4565	
1 V Digital supplies: VDDDIG1	MODE 4: 1 TX, 2 IQ/slice, LMFS = 4421, PLL on, 24x Interpolation, $f_{\text{INPUT}} = 368.64$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 1.84 GHz, NCO2 = 2.15 GHz, CLKTX Disabled		1701		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1314		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			256		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				3763	
1 V Digital supplies: VDDDIG1	MODE 5: 2 TX, 1 IQ/slice, LMFS = 4421, PLL on, 18x Interpolation, $f_{\text{INPUT}} = 491.52$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		1328		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1312		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			249		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				3374	
1 V Digital supplies: VDDDIG1	MODE 6: 1 TX, 1 IQ/slice, LMFS = 2221, PLL on, 18x Interpolation, $f_{\text{INPUT}} = 491.52$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		1027		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1206		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			248		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				2964	
1 V Digital supplies: VDDDIG1	MODE 7: 2 TX, 1 IQ/slice, LMFS = 8411, PLL on, 6x Interpolation, $f_{\text{INPUT}} = 983.04$ MSPS, $f_{\text{DAC}} = 5898.24$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		1157		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1125		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			246		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				3011	
1 V Digital supplies: VDDDIG1	MODE 8: 1 TX, 1 IQ/slice, LMFS = 4211, PLL on, 6x Interpolation, $f_{\text{INPUT}} = 983.04$ MSPS, $f_{\text{DAC}} = 5898.24$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		848		mA
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			647		mA
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			230		mA
-1.8 V Supply: VEE18N			159		mA
$P_{\text{DIS}}$ Power Dissipation				2195	

## Electrical Characteristics - DC Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , nominal supplies, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
1 V Digital supplies: VDDDIG1	MODE 9: 2 TX, 2 IQ/slice, LMFS = 4831, PLL on, 24x Interpolation, $f_{\text{INPUT}} = 368.64$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		2131		mA	
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1324		mA	
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18				251		mA
-1.8 V Supply: VEE18N				159		mA
$P_{\text{DIS}}$ Power Dissipation				4192		mW
1 V Digital supplies: VDDDIG1	MODE 10: 1 TX, 2 IQ/slice, LMFS = 2431, PLL on, 24x Interpolation, $f_{\text{INPUT}} = 368.64$ MSPS, $f_{\text{DAC}} = 8847.36$ MSPS, NCO1 = 2.14 GHz, CLKTX Disabled		1635		mA	
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1212		mA	
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18				250		mA
-1.8 V Supply: VEE18N				159		mA
$P_{\text{DIS}}$ Power Dissipation				3583		mW
1 V Digital supplies: VDDDIG1	MODE 11: Power down mode, no clock, DACs in sleep, Serdes in sleep		63	568	mA	
1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			18	105	mA	
1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18				47	51	mA
-1.8 V Supply: VEE18N				23	28	mA
$P_{\text{DIS}}$ Power Dissipation				208	815	mW
VDDTX1	$f_{\text{DAC}} = 8847$ MSPS, Clock Out Divider Enabled		25		mA	
	$f_{\text{DAC}} = 5898$ MSPS, Clock Out Divider Enabled		19		mA	
VDDTX18	Clock Out Enabled		16		mA	

## 7.6 Electrical Characteristics - Digital Specifications

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14 \text{ GHz}$ ,  $I_{(\text{OUTFS})} = 40 \text{ mA}$ , nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SERDES INPUTS: RX[7:0]+/-</b>					
$V_{\text{DIFF}}$	Receiver input amplitude	50		1200	mV
$V_{\text{COM}}$	Input common mode voltage	TERM = 111	600		mV
		TERM = 001	700		
		TERM = 100	0		
		TERM = 101	250		
$Z_{\text{DDIFF}}$	Internal differential termination	85	100	115	$\Omega$
$f_{\text{SERDES}}$	Serdes bit rate	0.78125		12.5	Gbps
<b>DIFFERENTIAL CLOCK INPUTS: SYSREF+/-, DACCLK+/-</b>					
$f_{\text{DACCLK}}$	DACCLK input frequency	0.1		9	GHz
$V_{\text{COM}}$	Differential input common mode voltage		0.5		V
$V_{(\text{DPP})}$	Differential input peak-to-peak voltage		800	2000	mV
$Z_T$	Internal termination		100		$\Omega$
$C_L$	Input capacitance		2		pF
	Duty cycle (DACCLK only)	40%		60%	
<b>LVDS OUTPUT: SYNC0+/-, SYNC1+/-</b>					
$V_{\text{COM}}$	Output common mode voltage		1.2		V
$Z_T$	Internal termination		100		$\Omega$
$V_{\text{OD}}$	Differential output voltage swing		500		mV
<b>CML OUTPUT: CLKTX+/-</b>					
$V_{\text{OD}}$	CML OUTPUT: CLKTX+/-		1300		mV
<b>CMOS INTERFACE: SDEN, SCLK, SDIO, SDO, TXENABLE, ALARM, RESET, SLEEP, TMS, TCLK, TDI, TDO, TRST, TESTMODE, SYNCSE1, SYNCSE2</b>					
$V_{\text{IH}}$	High-level input voltage	0.7 x VDDIO			V
$V_{\text{IL}}$	Low-level input voltage			0.3 x VDDIO	V
$I_{\text{IH}}$	High-level input current	-40		40	$\mu\text{A}$
$I_{\text{OL}}$	Low-level input current	-40		40	$\mu\text{A}$
$C_I$	CMOS input capacitance			2	pF
$V_{\text{OH}}$	High-level output voltage	$I_{\text{LOAD}} = -100 \mu\text{A}$	VDDIO - 0.2		V
		$I_{\text{LOAD}} = -2 \text{ mA}$	0.8 x VDDIO		
$V_{\text{OL}}$	Low-level output voltage	$I_{\text{LOAD}} = -100 \mu\text{A}$			0.2
		$I_{\text{LOAD}} = -2 \text{ mA}$			0.5
<b>LATENCY</b>					
RX SerDes Digital Delay		full rate, RATE = "00"	34		UI
		half rate, RATE = "01"	29		
		quarter rate, RATE = "10"	26.5		
		eighth rate, RATE = "11"	26.25		
SerDes output to JED204B elastic buffer input latency		21 -39		JESD clock cycles	

### Electrical Characteristics - Digital Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14 \text{ GHz}$ ,  $I_{(\text{OUTFS})} = 40 \text{ mA}$ , nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Latency: JESD Buffer to DAC Output	LMFSHD = 82121, 6x Interpolation		856		DAC clock cycles
	LMFSHD = 82121, 8x Interpolation		1120		
	LMFSHD = 82121, 12x Interpolation		1602		
	LMFSHD = 82121, 16x Interpolation		2091		
	LMFSHD = 42111 or 84111, 6x Interpolation		817		
	LMFSHD = 42111 or 84111, 8x Interpolation		1057		
	LMFSHD = 42111 or 84111, 10x Interpolation		1184		
	LMFSHD = 42111 or 84111, 12x Interpolation		1532		
	LMFSHD = 42111 or 84111, 16x Interpolation		1997		
	LMFSHD = 42111 or 84111, 18x Interpolation		2142		
	LMFSHD = 42111 or 84111, 24x Interpolation		2941		
	LMFSHD = 22210 or 44210, 8x Interpolation		1020		
	LMFSHD = 22210 or 44210, 12x Interpolation		1473		
	LMFSHD = 22210 or 44210, 16x Interpolation		1917		
	LMFSHD = 22210 or 44210, 18x Interpolation		2050		
	LMFSHD = 22210 or 44210, 20x Interpolation		2275		
	LMFSHD = 22210 or 44210, 24x Interpolation		2821		
	LMFSHD = 12410 or 24410, 16x Interpolation		1912		
	LMFSHD = 12410 or 24410, 24x Interpolation		2786		
	LMFSHD = 44210 or 88210, 8x Interpolation		916		
LMFSHD = 44210 or 88210, 12x Interpolation		1317			
LMFSHD = 44210 or 88210, 16x Interpolation		1709			
LMFSHD = 44210 or 88210, 24x Interpolation		2509			
LMFSHD = 24410 or 48410, 16x Interpolation		1672			
LMFSHD = 24410 or 48410, 24x Interpolation		1593			

## Electrical Characteristics - Digital Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14 \text{ GHz}$ ,  $I_{(\text{OUTFS})} = 40 \text{ mA}$ , nominal supplies, LMFSHD = 84111, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSREF TO JESD LMFC RESET	LMFSHD = 82121, 6x Interpolation		5		JESD clock cycles
	LMFSHD = 82121, 8x Interpolation		5		
	LMFSHD = 82121, 12x Interpolation		5		
	LMFSHD = 82121, 16x Interpolation		5		
	LMFSHD = 42111 or 84111, 6x Interpolation		16		
	LMFSHD = 42111 or 84111, 8x Interpolation		16		
	LMFSHD = 42111 or 84111, 10x Interpolation		15		
	LMFSHD = 42111 or 84111, 12x Interpolation		15		
	LMFSHD = 42111 or 84111, 16x Interpolation		13		
	LMFSHD = 42111 or 84111, 18x Interpolation		15		
	LMFSHD = 42111 or 84111, 24x Interpolation		15		
	LMFSHD = 22210 or 44210, 8x Interpolation		8		
	LMFSHD = 22210 or 44210, 12x Interpolation		7		
	LMFSHD = 22210 or 44210, 16x Interpolation		6		
	LMFSHD = 22210 or 44210, 18x Interpolation		7		
	LMFSHD = 22210 or 44210, 20x Interpolation		5		
	LMFSHD = 22210 or 44210, 24x Interpolation		4		
	LMFSHD = 12410 or 24410, 16x Interpolation		9		
	LMFSHD = 12410 or 24410, 24x Interpolation		7		
	LMFSHD = 44210 or 88210, 8x Interpolation		29		
	LMFSHD = 44210 or 88210, 12x Interpolation		27		
	LMFSHD = 44210 or 88210, 16x Interpolation		26		
	LMFSHD = 44210 or 88210, 24x Interpolation		25		
LMFSHD = 24410 or 48410, 16x Interpolation		8			
LMFSHD = 24410 or 48410, 24x Interpolation		6			
Latency	NCO				DAC clock cycles
	Inverse Sinc				
	Multi-band summation				
	PA Protection				
<b>PLL/VCO</b>					
$f_{\text{VCO}}$	VCO operating frequency	DAC38RF86/96	7.96	9	GHz
		DAC38RF87/97	5.24	6.72	GHz

## 7.7 Electrical Characteristics - AC Specifications

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14 \text{ GHz}$ ,  $I_{(\text{OUTFS})} = 40 \text{ mA}$ , nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG OUTPUT</b>						
$f_{\text{DAC}}$	Maximum DAC sample rate			9		GSPS
<b>AC PERFORMANCE - CW</b>						
SFDR	Spurious Free Dynamic Range 0 – $f_{\text{DAC}}/2$	$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		70		dBc
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		67		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		59		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		57		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		64		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		65		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		62		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		50		
SFDR	Spurious Free Dynamic Range within 500 MHz $f_{\text{OUT}} \pm 250 \text{ MHz}$	$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 3651 \text{ MHz}$		51		dBc
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		94		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		88		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		87		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		78		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		92		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		88		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		85		
SFDR	Spurious Free Dynamic Range excluding HD2, HD3 and CMP2 0 – $f_{\text{DAC}}/2$	$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		82		dBc
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 3651 \text{ MHz}$		78		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		72		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		75		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		75		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		71		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		63		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		66		
HD2	2nd Order Harmonic	$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		65		dBc
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		64		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 3651 \text{ MHz}$		62		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		71		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		68		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		59		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		57		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		71		
HD3	3rd Order Harmonic	$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		67		dBc
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		62		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		49		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 3651 \text{ MHz}$		51		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		75		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		72		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		72		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		70		
HD3	3rd Order Harmonic	$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		74		dBc
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		73		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		72		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 2651 \text{ MHz}$		69		
		$f_{\text{CLK}} = 9 \text{ GHz}, f_{\text{OUT}} = 3651 \text{ MHz}$		69		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 501 \text{ MHz}$		75		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 951 \text{ MHz}$		72		
		$f_{\text{CLK}} = 6 \text{ GHz}, f_{\text{OUT}} = 1851 \text{ MHz}$		72		

## Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14\text{ GHz}$ ,  $I_{\text{OUTFS}} = 40\text{ mA}$ , nominal supplies, LMFShd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMP2	Fs/2 clock mixing product ( $f_{\text{OUT}} - f_{\text{OUT}}$ )	$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		79		dBc
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		80		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		76		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		76		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		70		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		67		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		67		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		63		
CMP4+	Fs/N (N = 4, 8, 16) clock mixing product ( $f_{\text{OUT}} \pm f_{\text{OUT}}$ )	$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		90		dBc
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		87		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		83		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		76		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		91		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		88		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		85		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		81		
IMD3	Third-order two-tone intermodulation distortion	$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 501 \pm 5\text{ MHz}$ , -6 dBFS each tone		83		dBc
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 951 \pm 5\text{ MHz}$ , -6 dBFS each tone		79		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 1851 \pm 5\text{ MHz}$ , -6 dBFS each tone		76		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 2651 \pm 5\text{ MHz}$ , -6 dBFS each tone		75		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 501 \pm 5\text{ MHz}$ , -6 dBFS each tone		84		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 951 \pm 5\text{ MHz}$ , -6 dBFS each tone		80		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 1851 \pm 5\text{ MHz}$ , -6 dBFS each tone		74		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 2651 \pm 5\text{ MHz}$ , -6 dBFS each tone		73		
NSD	Noise Spectral Density > 50 MHz offset	$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		-169		dBFS/Hz
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		-163		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		-155		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		-154		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$		-171		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$		-167		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$		-156		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$		-155		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 3651\text{ MHz}$		-153		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 501\text{ MHz}$ , -9 dBFS		-160		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 951\text{ MHz}$ , -9 dBFS		-154		
		$f_{\text{CLK}} = 6\text{ GHz}$ , $f_{\text{OUT}} = 1851\text{ MHz}$ , -9 dBFS		-150		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 2651\text{ MHz}$ , -9 dBFS		-153		
		$f_{\text{CLK}} = 9\text{ GHz}$ , $f_{\text{OUT}} = 3651\text{ MHz}$ , -9 dBFS		-150		

## Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , external differential clock mode at 9 GSPS, 12x Interpolation,  $f_{\text{OUT}} = 2.14\text{ GHz}$ ,  $I_{(\text{OUTFS})} = 40\text{ mA}$ , nominal supplies, LMFShd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD (On-chip PLL)	Noise Spectral Density > 50 MHz offset On-chip PLL enabled	$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 501\text{ MHz}$		-161		dBFS/Hz
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 951\text{ MHz}$		-160		
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 1851\text{ MHz}$		-156		
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 2651\text{ MHz}$		-151		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 501\text{ MHz}$		-171		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 951\text{ MHz}$		-166		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 1851\text{ MHz}$		-156		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 2651\text{ MHz}$		-156		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 3651\text{ MHz}$		-153		
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 501\text{ MHz}, -9\text{ dBFS}$		-154		
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 951\text{ MHz}, -9\text{ dBFS}$		-154		
		$f_{\text{CLK}} = 6\text{ GHz}, f_{\text{OUT}} = 1851\text{ MHz}, -9\text{ dBFS}$		-151		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 2651\text{ MHz}, -9\text{ dBFS}$		-153		
		$f_{\text{CLK}} = 9\text{ GHz}, f_{\text{OUT}} = 3651\text{ MHz}, -9\text{ dBFS}$		-151		
Isolation	Isolation between DAC A and DAC B analog output	< 2 GHz		55		dBc
		>2 GHz to 4 GHz		54		
<b>AC PERFORMANCE – Modulated Signals</b>						
ACPR	WCDMA 1 carrier adjacent channel power ratio	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		78		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		73		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		77		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		73		
Alt-ACLR	WCDMA 1 carrier alternate channel ACPR	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		83		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		77		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		82		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		78		
LTE20	20 MHz LTE adjacent channel power ratio	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 800\text{ MHz}$		74		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2650\text{ MHz}$		68		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 800\text{ MHz}$		74		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2650\text{ MHz}$		68		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 3700\text{ MHz}$		66		
<b>AC PERFORMANCE – Modulated Signals, On-chip PLL enabled</b>						
ACPR	WCDMA 1 carrier adjacent channel power ratio	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		77		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		73		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		75		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		69		
Alt-ACLR	WCDMA 1 carrier alternate channel ACPR	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		82		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		78		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 950\text{ MHz}$		81		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2140\text{ MHz}$		77		
LTE20	20 MHz LTE adjacent channel power ratio	$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 800\text{ MHz}$		75		dBc
		$f_{\text{CLK}} = 5898.24\text{ MHz}, f_{\text{OUT}} = 2650\text{ MHz}$		69		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 800\text{ MHz}$		73		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 2650\text{ MHz}$		67		
		$f_{\text{CLK}} = 8847.36\text{ MHz}, f_{\text{OUT}} = 3700\text{ MHz}$		64		

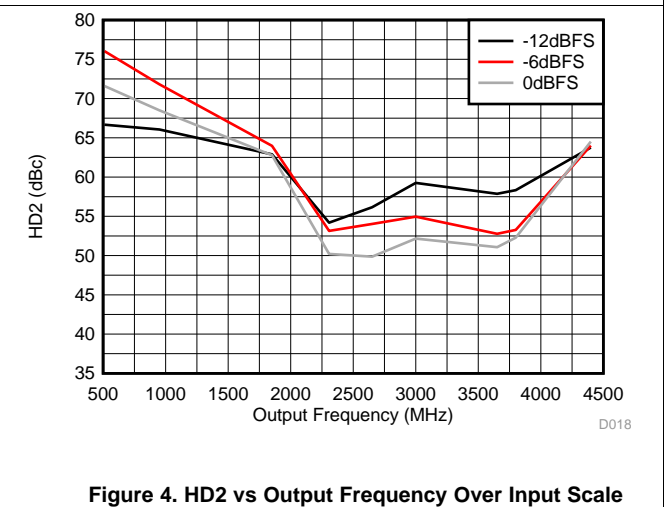
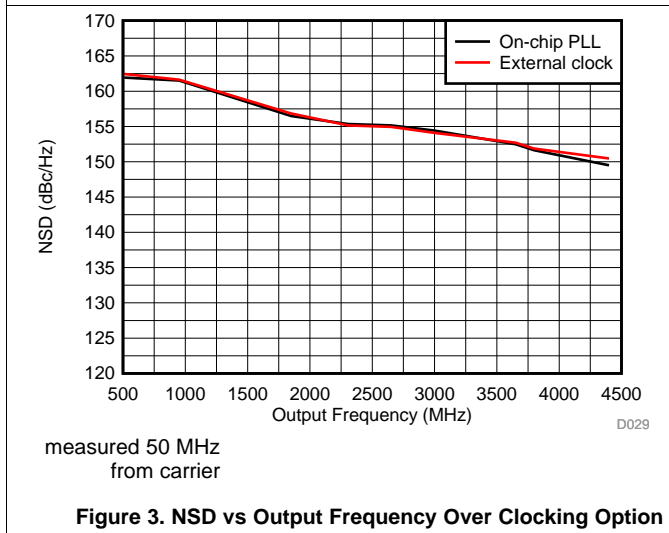
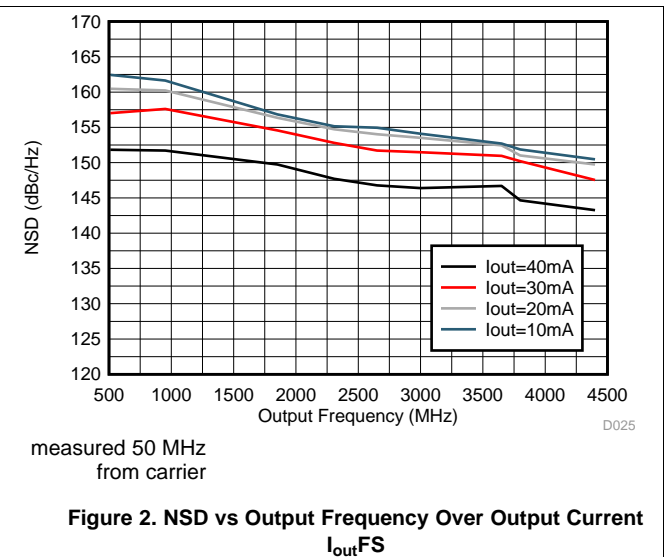
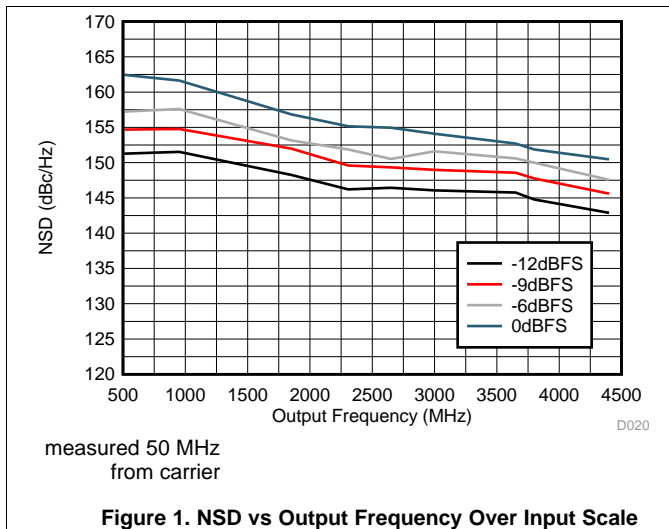


## 7.8 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>DIGITAL INPUT TIMING SPECIFICATIONS</b>					
<b>TIMING: SYSREF+/-</b>					
$t_{s(\text{SYSREF})}$	Setup time, SYSREF+/- valid to rising edge of DACCLK+/-	SYSREF Capture assist disabled		50	ps
$t_{h(\text{SYSREF})}$	Hold time, SYSREF+/- valid after rising edge of DACCLK+/-	SYSREF Capture assist disabled		50	ps
<b>TIMING: SERIAL PORT</b>					
$t_{s(\text{SDEN})}$	Setup time, $\overline{\text{SDEN}}$ to rising edge of SCLK			20	ns
$t_{s(\text{SDIO})}$	Setup time, SDIO valid to rising edge of SCLK			10	ns
$t_{h(\text{SDIO})}$	Hold time, SDIO valid after rising edge of SCLK			5	ns
$t_{(\text{SCLK})}$	Period of SCLK	temperature sensor read		1	$\mu\text{s}$
		All other registers		100	ns
$t_{d(\text{Data})}$	Data output delay after falling edge of SCLK			25	ns
$t_{\text{RESET}}$	Minimum $\overline{\text{RESET}}$ pulse width			25	ns
<b>ANALOG OUTPUT</b>					
$t_{s(\text{DAC})}$	Output settling time to 0.1%			1	ns
$t_r$	Output rise time 10% to 90%			50	ns
$t_f$	Output fall time 90% to 10%			50	ns
<b>LATENCY</b>					
RX SerDes AnalogDelay				250	ps
DAC wake-up time		$I_{\text{OUT}}$ current settling to 1% of $I_{\text{OUTFS}}$ from deep sleep		90	$\mu\text{s}$
DAC sleep time		$I_{\text{OUT}}$ current settling to less than 1% of $I_{\text{OUTFS}}$ in deep sleep		90	$\mu\text{s}$

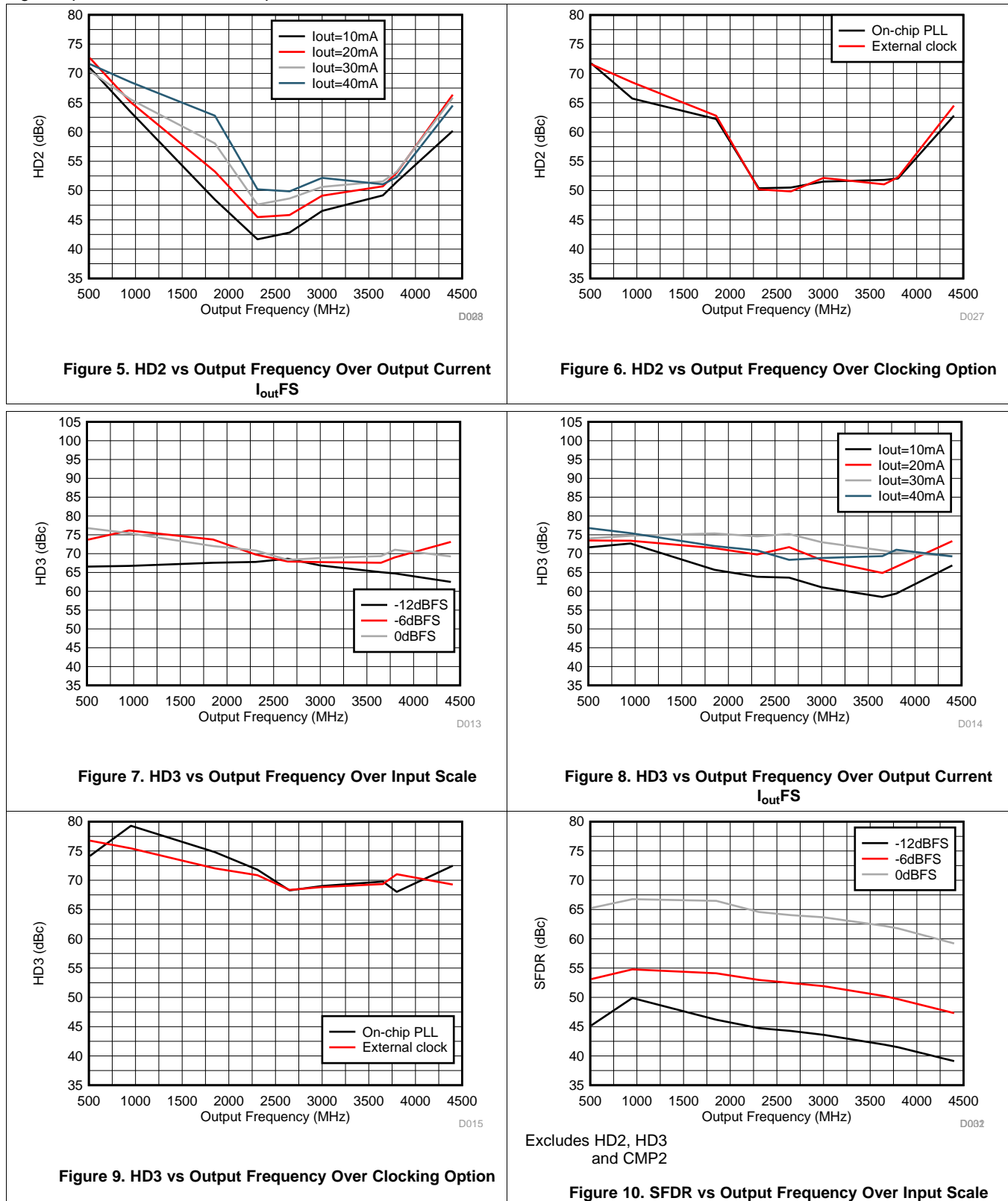
## 7.9 Typical Characteristics

Unless otherwise noted, all plots are at  $T_A = 25^\circ\text{C}$ , nominal supply voltages,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , 12x interpolation, 0dBFS digital input, 40 mA full scale output current, LMFSHd = 84111 and PLL is disabled.



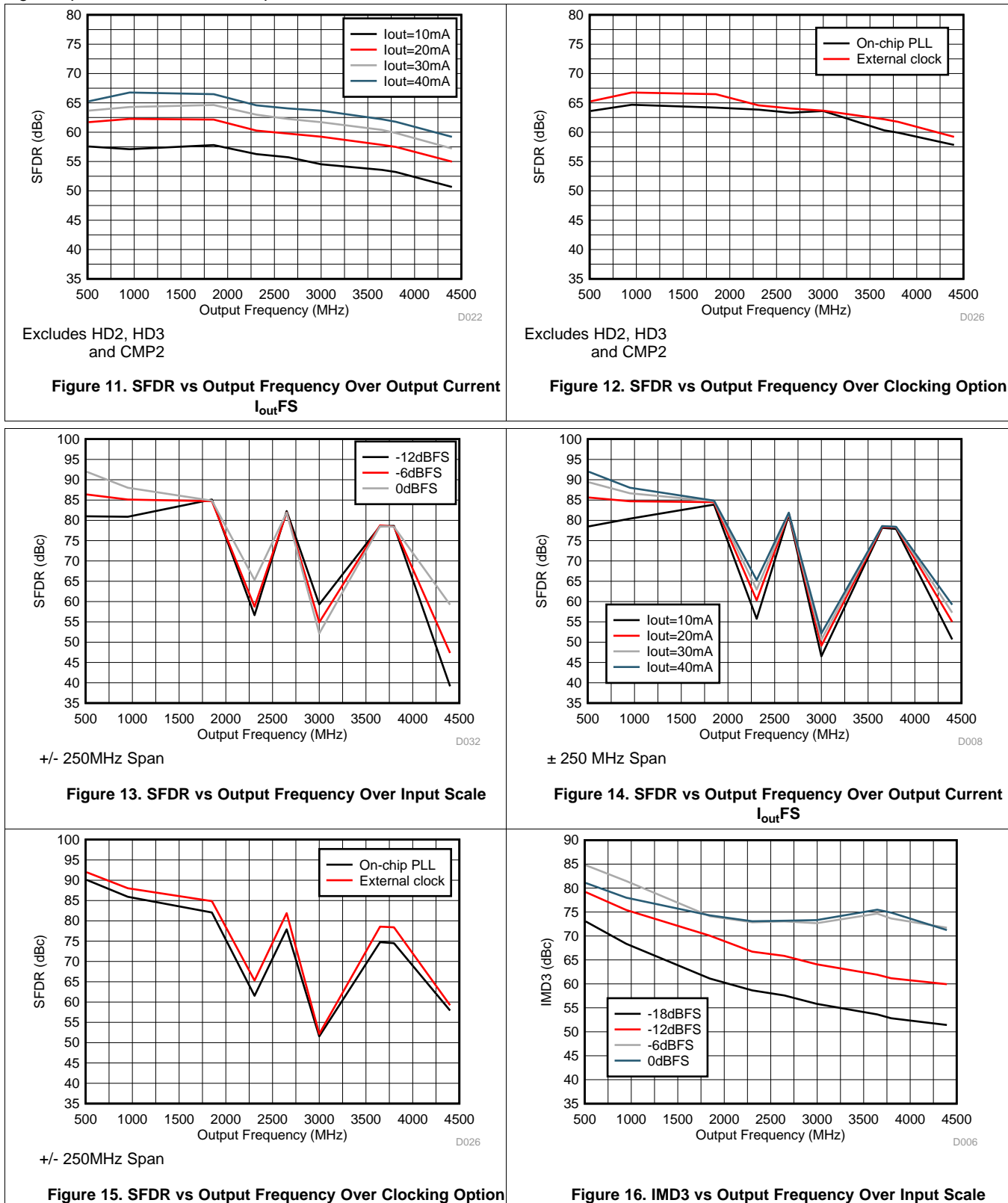
### Typical Characteristics (continued)

Unless otherwise noted, all plots are at  $T_A = 25^\circ\text{C}$ , nominal supply voltages,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , 12x interpolation, 0dBFS digital input, 40 mA full scale output current, LMFShd = 84111 and PLL is disabled.



## Typical Characteristics (continued)

Unless otherwise noted, all plots are at  $T_A = 25^\circ\text{C}$ , nominal supply voltages,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , 12x interpolation, 0dBFS digital input, 40 mA full scale output current, LMFSHd = 84111 and PLL is disabled.



### Typical Characteristics (continued)

Unless otherwise noted, all plots are at  $T_A = 25^\circ\text{C}$ , nominal supply voltages,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , 12x interpolation, 0dBFS digital input, 40 mA full scale output current,  $\text{LMFSHd} = 84111$  and PLL is disabled.

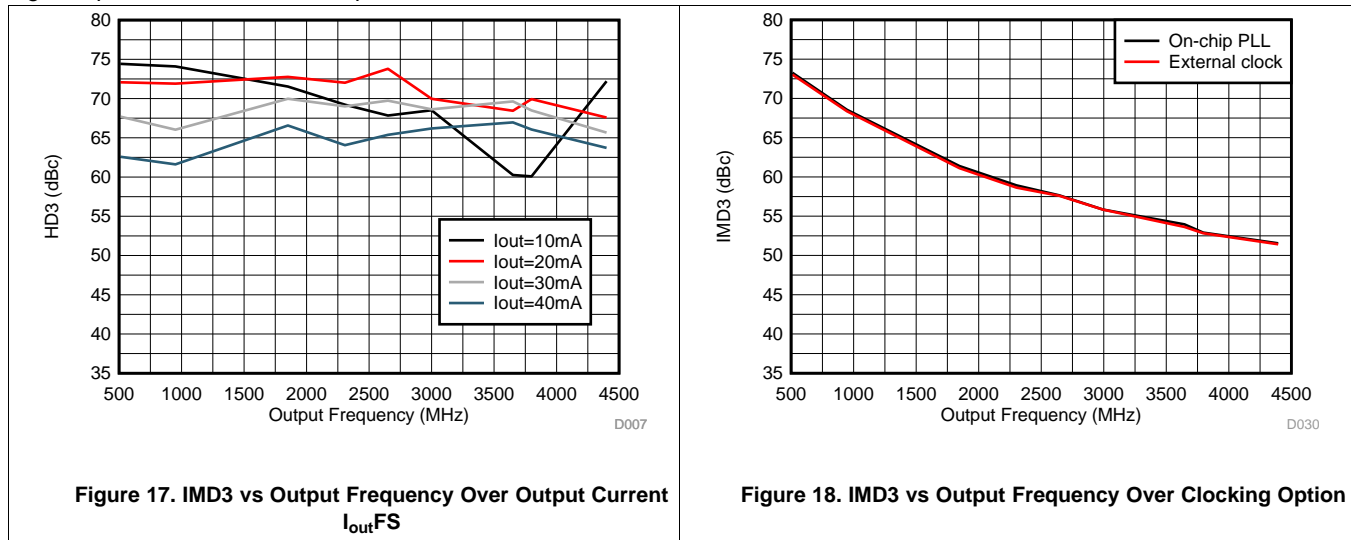


Figure 17. IMD3 vs Output Frequency Over Output Current  $I_{\text{outFS}}$

Figure 18. IMD3 vs Output Frequency Over Clocking Option

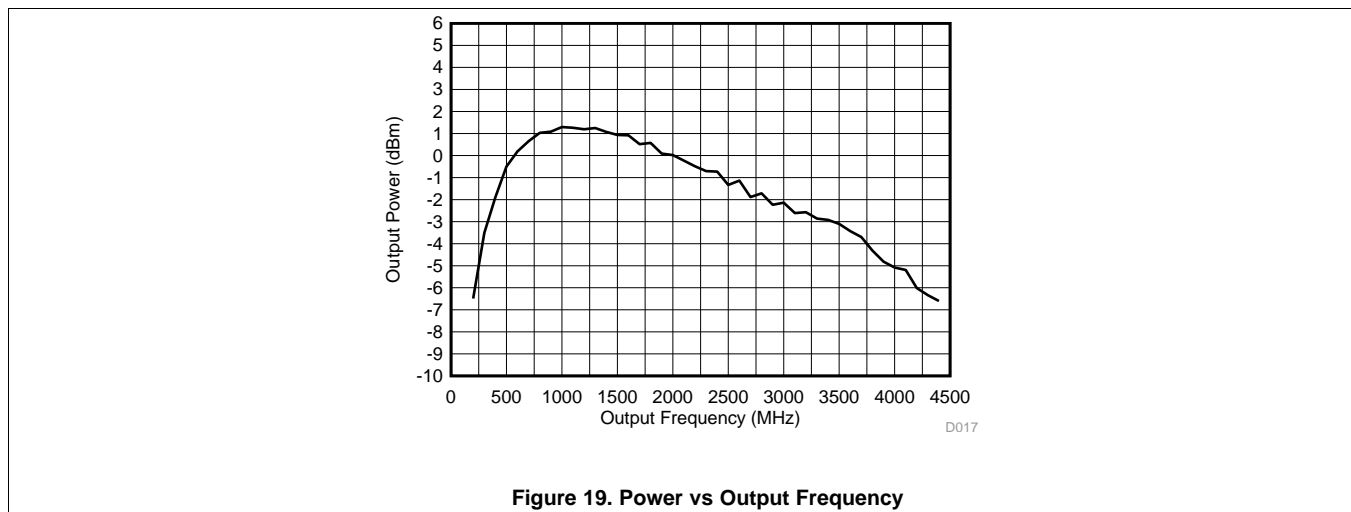


Figure 19. Power vs Output Frequency

### Typical Characteristics (continued)

Unless otherwise noted, all plots are at  $T_A = 25^\circ\text{C}$ , nominal supply voltages,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , 12x interpolation, 0dBFS digital input, 40 mA full scale output current, LMFSHd = 84111 and PLL is disabled.

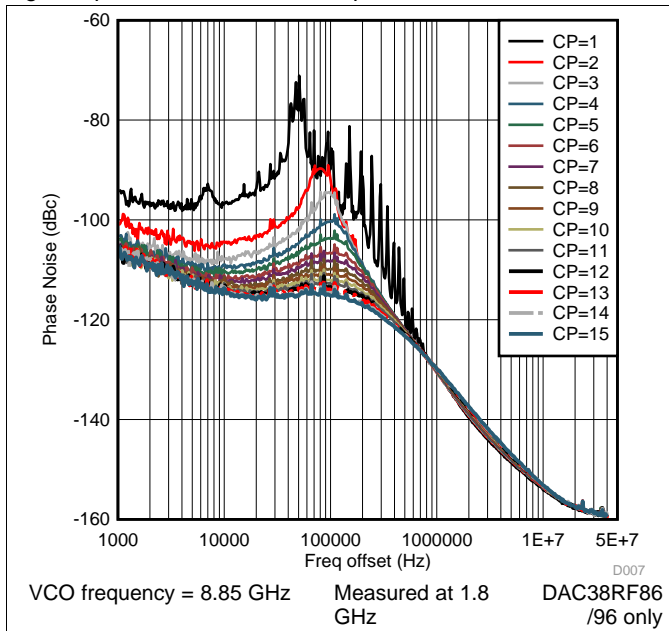


Figure 20. VCO Phase Noise vs Offset Frequency Over Charge pump current

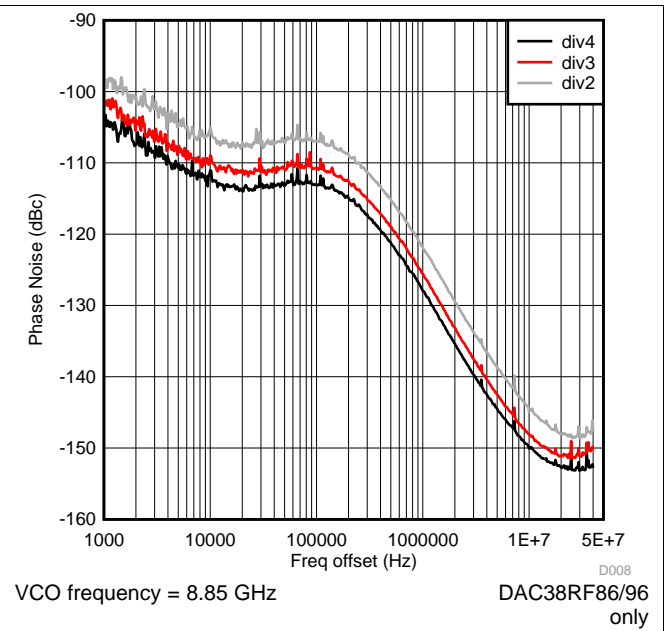


Figure 21. VCO1 Output Clock Phase Noise vs Offset frequency Over Divider Ratio

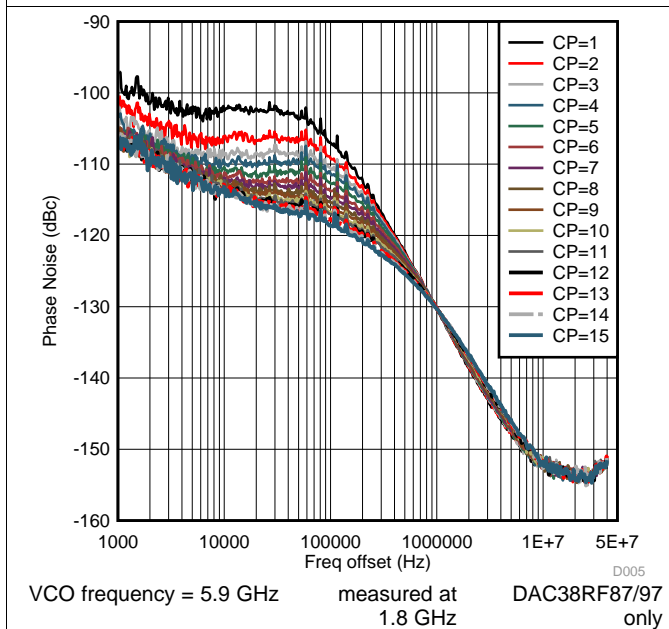


Figure 22. VCO Phase Noise vs Offset Frequency Over Charge Pump Current

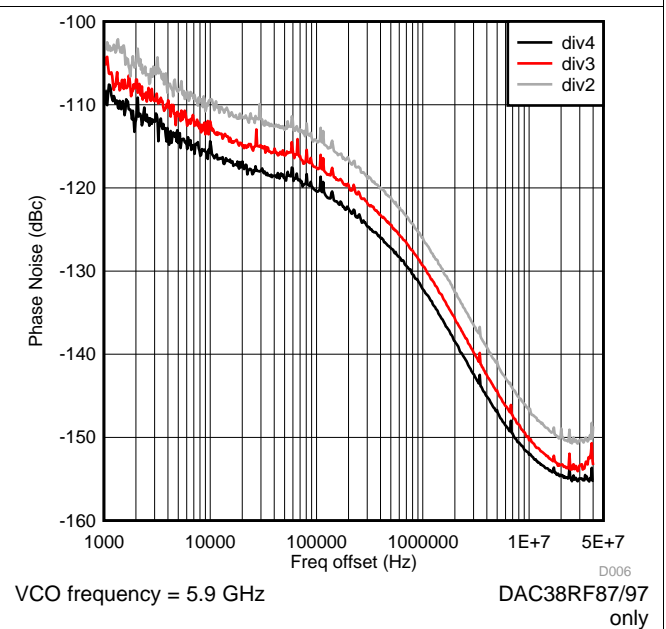


Figure 23. VCO Output clock Phase Noise vs Offset Frequency Over Divider Ratio

## 8 Detailed Description

### 8.1 Overview

The DAC38RFxx are a family of high performance 14-bit, 9 GSPS interpolating digital-to-analog converter (DACs), capable of synthesizing wideband signals from 0 to 4 GHz in 1st Nyquist zone and up to 6 GHz in 2nd Nyquist zone. A high dynamic range allows the DAC38RFxx to generate 2G/3G/4G signals for wireless basestations for all 3GPP bands, including simultaneous generation of multiple bands.

The devices have a low power 8 lane JESD204B Interface, with a maximum bit rate of 12.5 Gbps. The full output rate is achieved by use of the interpolation filters, after which the signal can be upconverted to RF using a digital NCO and digital quadrature modulator. Two signals can be tuned to different frequencies and digitally combined, allowing wide output spectrums. An optional low jitter PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency reference clock.

### 8.2 Functional Block Diagrams

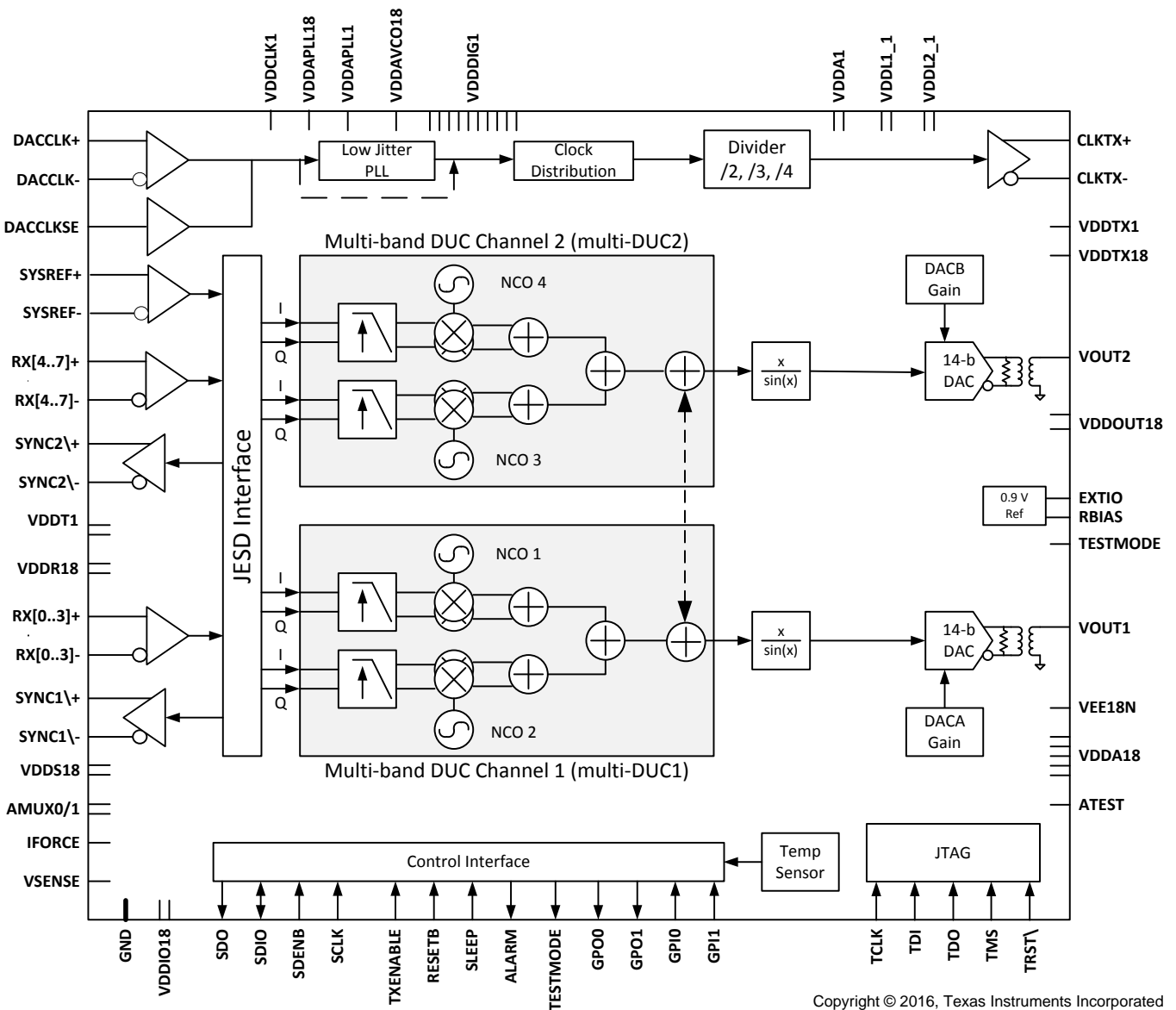
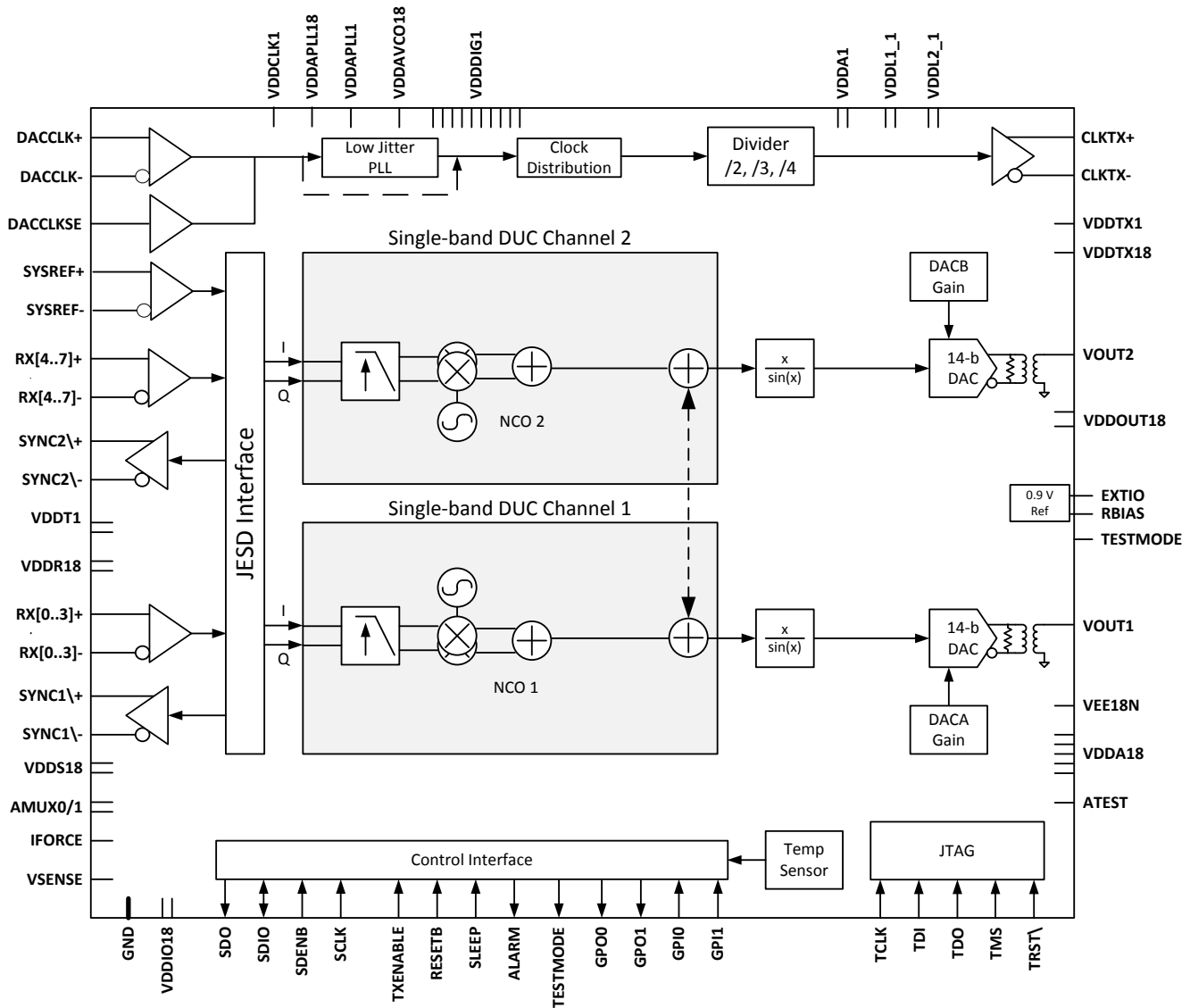


Figure 24. DAC38RF86, DAC38RF87 Block Diagram

Functional Block Diagrams (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 25. DAC38RF96, DAC38RF97 Block Diagram



### 8.3 Feature Description

#### 8.3.1 Serdes Inputs

The DAC38RFxx RX [0..7]+/- differential inputs are each internally terminated to a common point via 50 Ω, as shown in Figure 26.

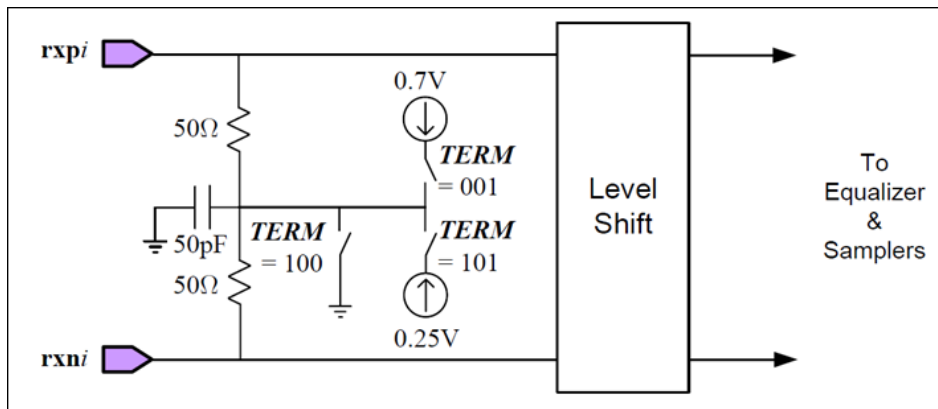


Figure 26. Serial Lane Input Termination

Common mode termination is via a 50 pF capacitor to GND. The common mode voltage and termination of the differential signal can be controlled in a number of ways to suit a variety of applications via field TERM in register SRDS\_CFG2 (8.5.87), as described in Table 1.

**NOTE**

AC coupling is recommended for JESD204B compliance.

Table 1. Receiver Termination Selection

TERM	EFFECT
000	Reserved
001	Common point set to 0.7 V. This configuration is for AC coupled systems. The transmitter has no effect on the receiver common mode, which is set to optimize the input sensitivity of the receiver. Note: this mode is not compatible with JESD204B.
01x	Reserved
100	Common point set to GND. This configuration is for applications that require a 0 V common mode.
101	Common point set to 0.25 V. This configuration is for applications that require a low common mode.
110	Reserved
111	Common point floating. This configuration is for DC coupled systems in which the common mode voltage is set by the attached transmit link partner to 0 and 0.6 V. Note: this mode is not compatible with JESD204B

Input data is sampled by the differential sensing amplifier using clocks derived from the clock recovery algorithm. The polarity of RX+ and RX- can be inverted by setting the bit of the corresponding lane in field INVPAIR in register SRDS\_POL (8.5.88) to “1”. This can potentially simplify PCB layout and improve signal integrity by avoiding the need to swap over the differential signal traces.

Due to processing effects, the devices in the RX+ and RX- differential sense amplifiers will not be perfectly matched and there will be some offset in switching threshold. The DAC38RFxx contains circuitry to detect and correct for this offset. This feature can be enabled by setting ENOC in register SRDS\_CFG1 (8.5.86) to “1”. It is anticipated the most users will enable this feature. During the compensation process, LOOPBACK in register SRDS\_CFG1 (8.5.86) must be set to “00”.

### 8.3.2 Serdes Rate

The DAC38RFxx has eight configurable JESD204B serial lanes. The highest speed of each SerDes lane is 12.5 Gbps. Because the primary operating frequency of the SerDes is determined by its reference clock and PLL multiplication factor, there is a limit on the lowest SerDes rate supported. To support lower speed application, each receiver should be configured to operate at half, quarter or eighth of the full rate via field RATE in register SRDS\_CFG2 (8.5.87). Refer to Table 2 for details.

Table 2. Lane Rate Selection

RATE	EFFECT
00	Full rate. Four data samples taken per SerDes PLL output clock cycle.
01	Half rate. Two data samples taken per SerDes PLL output clock cycle.
10	Quarter rate. One data samples taken per SerDes PLL output clock cycle.
11	Eighth rate. One data samples taken every two SerDes PLL output clock cycles.

### 8.3.3 Serdes PLL

The DAC38RFxx has two integrated PLLs, one PLL is to provide the clocking of DAC; the other PLL is to provide the clocking for the high speed SerDes. The reference frequency of the SerDes PLL can be in the range of 100-800 MHz nominal, and 300-800 MHz optimal. The reference frequency is derived from DACCLK divided down by the value in field SERDES\_REFCLK\_DIV in register SRDS\_CLK\_CFG (8.5.84), as shown in Figure 27. Field SERDES\_CLK\_SEL in register SRDS\_CLK\_CFG (8.5.84) determines if the DACCLK input or DAC PLL output is used as the source of the Serdes PLL reference. If the DACCLK input is used, a pre-divider set by field SERDES\_REFCLK\_PREDIV in register SRDS\_CLK\_CFG (8.5.84) should be used to reduce the frequency of the DACCLK.

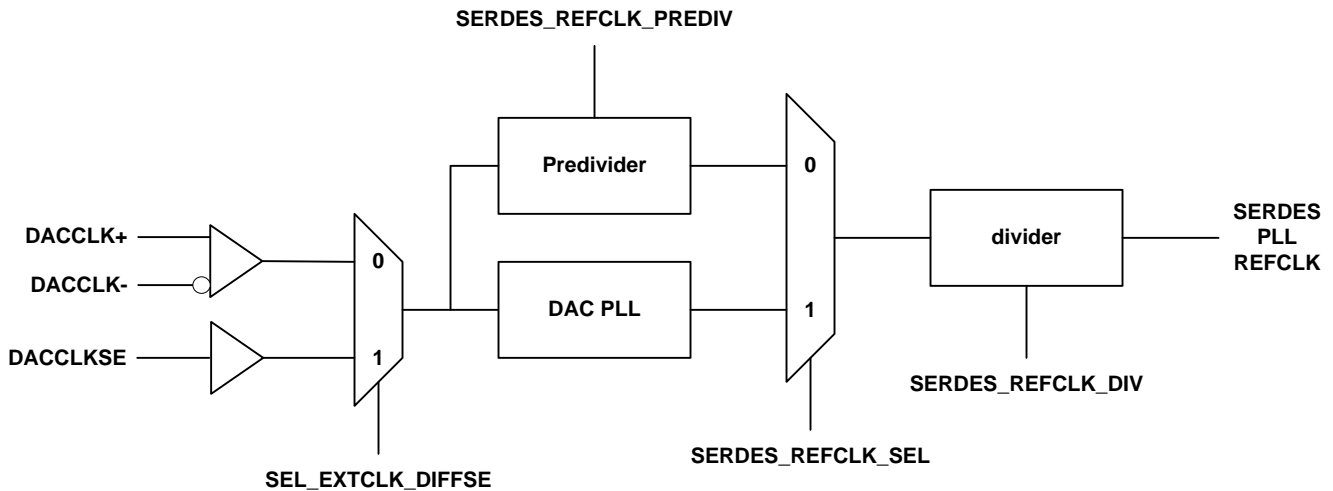


Figure 27. Reference Clock of SerDes PLL

During normal operation, the clock generated by PLL is 4-25 times the reference frequency, according to the multiply factor selected via the field MPY] in register SRDS\_PLL\_CFG (8.5.85). In order to select the appropriate multiply factor and reference clock frequency, it is first necessary to determine the required PLL output clock frequency. The relationship between the PLL output clock frequency and the lane rate is determined by field RATE in register SRDS\_CFG2 (8.5.87) is shown in Table 3. Having computed the PLL output frequency, the reference frequency can be obtained by dividing this by the multiply factor specified via MPY.

**Table 3.**

RATE	LINE RATE	PLL OUTPUT FREQUENCY
00	x Gbps	0.25x GHz
01	x Gbps	0.5x GHz
10	x Gbps	1x GHz
11	x Gbps	2x GHz

**Table 4. SerDes PLL Modes Selection**

MPY	EFFECT
00010000	4x
00010100	5x
00011000	6x
00100000	8x
00100001	8.25x
00101000	10x
00110000	12x
00110010	12.5x
01000000	15x
01000010	16x
01010000	20x
01011000	22x
01100100	25x
Other codes	Reserved

The wide range of multiply factors combined with the different rate modes means it is often possible to achieve a given line rate from multiple different reference frequencies. The configuration which utilizes the highest reference frequency achievable is always preferable.

The SerDes PLL VCO must be in the nominal range of 1.5625 - 3.125 GHz. It is necessary to adjust the loop filter depending on the operating frequency of the VCO. If the PLL output frequency is below 2.17 GHz, VRANGE in register SRDS\_PLL\_CFG (8.5.84) should be set high.

Performance of the integrated PLL can be optimized according to the jitter characteristics of the reference clock by setting the appropriate loop bandwidth via field LB in register SRDS\_PLL\_CFG (8.5.84). The loop bandwidth is obtained by dividing the reference frequency by BWSCALE, where the BWSCALE is a function of both LB and PLL output frequency as shown in Table 5.

**Table 5. SerDes PLL Loop Bandwidth Selection**

LB	EFFECT	BWSCALE vs PLL OUTPUT FREQUENCY		
		3.125 GHz	2.17 GHz	1.5625 GHz
00	Medium loop bandwidth	13	14	16
01	Ultra high loop bandwidth	7	8	8
10	Low loop bandwidth	21	23	30
11	High loop bandwidth	10	11	14

An approximate loop bandwidth of 8 – 30 MHz is suitable and recommended for most systems where the reference clock is via low jitter clock input buffer. For systems where the reference clock is via a low jitter input cell, but of low quality, an approximate loop bandwidth of less than 8 MHz may offer better performance. For systems where the reference clock is cleaned via an ultra-low jitter LC-based cleaner PLL, a high loop bandwidth up to 60 MHz is more appropriate. Note that the use of ultra-high loop bandwidth setting is not recommended for PLL multiply factor of less than 8.

A free running clock output is available when field ENDIVCLK in register SRDS\_PLL\_CFG (8.5.85) is set high. It runs at a fixed divided-by-80 of the PLL output frequency and can be output on the ALARM pin by setting field DTEST to “0001” (lanes 0 – 3) or “0010” (lanes 4 – 7) in register DTEST (8.5.76).

### 8.3.4 Serdes Equalizer

All channels of the DAC38RFxx incorporate an adaptive equalizer, which can compensate for channel insertion loss by attenuating the low frequency components with respect to the high frequency components of the signal, thereby reducing inter-symbol interference. Figure 28 shows the response of the equalizer, which can be expressed in terms of the amount of low frequency gain and the frequency up to which this gain is applied (i.e., the frequency of the 'zero'). Above the zero frequency, the gain increases at 6 dB/octave until it reaches the high frequency gain.

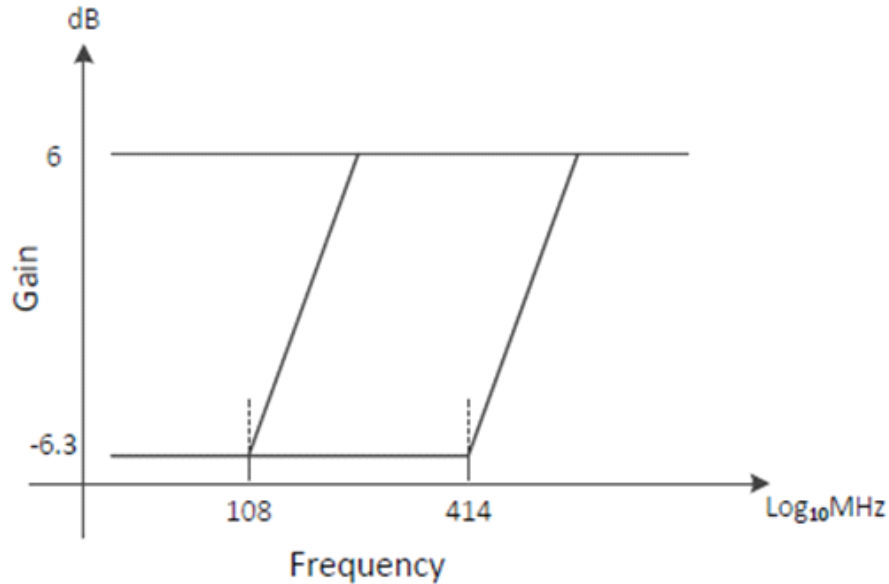


Figure 28. Equalizer Frequency Response

The equalizer can be configured via fields EQ and EQHLD in register SRDS\_CFG1 (8.5.86). Table 6 and Table 7 summarize the options. When enabled, the receiver equalization logic analyzes data patterns and transition times to determine whether the low frequency gain should be increased or decreased. The decision logic is implemented as a voting algorithm with a relatively long analysis interval. The slow time constant that results reduces the probability of incorrect decisions but allows the equalizer to compensate for the relatively stable response of the channel. The lock time for the adaptive equalizer is data dependent, and so it is not possible to specify a generally applicable absolute limit. However, assuming random data, the maximum lock time will be  $6 \times 10^6$  divided by the CDR activity level. For field CDR in register SRDS\_CFG1 (8.5.86) = 110, the activity level is  $1.5 \times 10^6$  UI.

When EQ = 0, finer control of gain boost is available using the EQBOOST IEEE1500 tuning chain field, as shown in Table 8.

Table 6. Receiver Equalization Configuration

EQ		EFFECT
[1-0]	00	No equalization. The equalizer provides a flat response at the maximum gain. This setting may be appropriate if jitter at the receiver occurs predominantly as a result of crosstalk rather than frequency dependent loss.
	01	Fully adaptive equalization. The zero position is determined by the selected operating rate, and the low frequency gain of the equalizer is determined algorithmically by analyzing the data patterns and transition positions in the received data. This setting should be used for most applications.
	10	Precursor equalization analysis. The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less precursor equalization than necessary.
	11	Postcursor equalization analysis. The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less post-cursor equalization than necessary.

**Table 6. Receiver Equalization Configuration (continued)**

EQ		EFFECT
[2]	0	Default
	1	Boost. Equalizer gain boosted by 6 dB, with a 20% reduction in bandwidth, and an increase of 5mW power consumption. May improve performance over long links.

**Table 7. Receiver Equalizer Hold**

EQHOLD	EFFECT
0	Equalizer adaption enabled. The equalizer adaption and analysis algorithm is enabled. This should be the default state.
1	Equalizer adaption held. The equalizer is held in its current state. Additionally, the adaption and analysis algorithm is reset.

**Table 8. Relationship Between Lane Rate and SerDes PLL Output Frequency**

EQBOOST	GAIN BOOST (dB)	BANDWIDTH CHANGE (%)	POWER INCREASE (mW)
00	0	0	0
01	2	-30	0
01	4	10	5
11	6	-20	5

When EQ is set to 010 or 011, the equalizer is reconfigured to provide analytical data about the amount of pre and post cursor equalization respectively present in the received signal. This can in turn be used to adjust the equalization settings of the transmitting link partner, where a suitable mechanism for communicating this data back to the transmitter exists. Status information is provided by setting field DTEST in register DTEST (8.5.76) to "0111" for EQOVER and "0110" for EQUNDER. The procedure is as follows:

1. Enable the equalizer by setting fields EQHLD low and EQ to "001" (register SRDS\_CFG1 8.5.86). Allow sufficient time for the equalizer to adapt;
2. Set EQHLD to 1 to lock the equalizer and reset the adaption algorithm. This also causes both EQOVER and EQUNDER to become low;
3. Wait at least 48 UI, and proportionately longer if the CDR activity is less than 100%, to ensure the 1 on EQHLD is sampled and acted upon;
4. Set EQ to "010" or "011", and EQHLD to 0. The equalization characteristics of the received signal are analysed (the equalizer response will continue to be locked);
5. Wait at least  $150 \times 10^3$  UI to allow time for the analysis to occur, proportionately longer if the CDR activity is less than 100%;
6. Examine EQOVER and EQUNDER for results of analysis
  - If EQOVER is high, it indicates the signal is over equalized;
  - If EQUNDER is high, it indicates the signal is under equalized;
7. Set EQHLD to 1;
8. Repeat items 3–7 if required;
9. Set EQ to "001", and EQHLD to 0 to exit analysis mode and return to normal adaptive equalization.

#### NOTE

When changing EQ from one non-zero value to another, EQHLD must already be 1. If this is not the case, there is a chance the equalizer could be reset by a transitory input state (i.e., if EQ is momentarily 000). EQHLD can be set to 0 at the same time as EQ is changed.

As the equalizer adaption algorithm is designed to equalize the post cursor, EQOVER or EQUNDER will only be set during post cursor analysis if the amount of post cursor equalization required is more or less than the adaptive equalizer can provide.

### 8.3.5 JESD204B Descrambler

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial  $1 + x^{14} + x^{15}$ . From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. Each multi-DUC has a separate descrambler that can be enabled independently. The descrambler is enabled by field SCR in the multi-DUC paged register JESD\_N\_HD\_SCR (8.5.49).

### 8.3.6 JESD204B Frame Assembly

The DAC38RFxx may be programmed as a single or dual DAC device, with one JESD RX block designated for each DAC. The two JESD RX blocks can be programmed to operate as two separate links or as a single link.

The JESD204B defines the following parameters:

- L is the number of lanes
- M is the number of I or Q streams per device (2 = 1 IQ pair, 4 = 2 IQ pairs, 8 = 4 IQ pairs)
- F is the number of octets per frame clock period
- S is the number of samples per frame
- HD is the High-Density bit which controls whether a sample may be divided over more lanes
- N = NPRIME is the number of bits per sample (12 or 16 - bits)

Fields K and L are found in multi-DUC paged register JESD\_K\_L (8.5.46), M and S in multi-DUC paged register JESD\_M\_S (8.5.48), and N, NPRIME and HD in multi-DUC paged register JESD\_N\_HD\_SCR (8.5.49).

Table 9 lists the available JESD204B formats, interpolation rates and sample rate limits for the DAC38RFxx. The ranges are limited by the Serdes PLL VCO frequency range, the Serdes PLL reference clock range, the maximum Serdes line rate, and the maximum DAC sample frequency. Table 10 through Table 22 lists the frame formats for each mode. In the frame format tables, i CH (N) [x:y] and q CH (N) [x:y] are bits x through y of the I and Q samples at time N of DUC channel CH. If [x..y] is not listed, the full sample is assumed. For example, i0(0)[15:8] are bits 15 – 8 of the I sample at time 0 of DUC #0, and q1(1) is the full Q sample at time 1 of DUC #1.

**Table 9. JESD204B Formats for DAC38RFxx**

L-M-F-S-Hd 1 TX	L-M-F-S- Hd 2 TX	Frame Format	Input Resolutio n	IQ pairs per DAC	Interp	Input rate max (MSPS)	f <sub>DAC</sub> Max (MSPS)	DAC38RF86, DAC38RF87	DAC38RF96, DAC38RF97
82121	NA	1 TX: Table 10	16	1	6	1250	7500	x	
			16	1	8	1125	9000	x	
			16	1	12	750	9000	x	x
			16	1	16	562.5	9000	x	x
42111	84111	1 TX: Table 11 2 TX: Table 12	16	1	6	1250	7500	x	
			16	1	8	1125	9000	x	
			16	1	10	900	9000	x	
			16	1	12	750	9000	x	x
			16	1	16	562.5	9000	x	x
			16	1	18	500	9000	x	x
22210	44210	1 TX: Table 13 2 TX: Table 14	16	1	8	625	5000	x	
			16	1	12	625	7500	x	x
			16	1	16	562.5	9000	x	x
			16	1	18	500	9000	x	x
			16	1	20	450	9000	x	x
			16	1	24	375	9000	x	x

L-M-F-S-Hd 1 TX	L-M-F-S- Hd 2 TX	Frame Format	Input Resolutio n	IQ pairs per DAC	Interp	Input rate max (MSPS)	f <sub>DAC</sub> Max (MSPS)	DAC38RF86, DAC38RF87	DAC38RF96, DAC38RF97
12410	24410	1 TX: <a href="#">Table 15</a>	16	1	16	312.5	5000	x	x
		2 TX: <a href="#">Table 16</a>	16	1	24	312.5	7500	x	x
44210	88210	1 TX: <a href="#">Table 17</a>	16	2	8	625	5000	x	
		2 TX: <a href="#">Table 18</a>	16	2	12	625	7500	x	
			16	2	16	562.5	9000	x	
			16	2	24	375	9000	x	
24410	48410	1 TX: <a href="#">Table 19</a>	16	2	16	312.5	5000	x	
		2 TX: <a href="#">Table 20</a>	16	2	24	312.5	7500	x	
24310	48310	1 TX: <a href="#">Table 21</a> 2 TX: <a href="#">Table 22</a>	12	2	24	375	9000	x	

**Table 10. JESD204B Frame Format for LMFSHd = 82121**

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	i0[15:8]	
lane RX1	i0[7:0]	
lane RX2	i1[15:8]	
lane RX3	i1[7:0]	
lane RX4	q0[15:8]	
lane RX5	q0[7:0]	
lane RX6	q1[15:8]	
lane RX7	q1[7:0]	

**Table 11. JESD204B Frame Format for LMFSHd = 42111**

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	i0[15:8]	
lane RX1	i0[7:0]	
lane RX2	q0[15:8]	
lane RX3	q0[7:0]	

**Table 12. JESD204B Frame Format for LMFSHd = 84111**

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	i0[15:8]	
lane RX1	i0[7:0]	
lane RX2	q0[15:8]	
lane RX3	q0[7:0]	
lane RX4	i1[15:8]	
lane RX5	i1[7:0]	
lane RX6	q1[15:8]	

**Table 12. JESD204B Frame Format for LMFSHd = 84111 (continued)**

lane RX7	q1[7:0]
----------	---------

**Table 13. JESD204B Frame Format for LMFSHd = 22210**

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			

**Table 14. JESD204B Frame Format for LMFSHd = 44210**

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			
lane RX2	i1			
lane RX3	q1			

**Table 15. JESD204B Frame Format for LMFSHd = 12410**

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	i0				q0			

**Table 16. JESD204B Frame Format for LMFSHd = 24410**

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	i0				q0			
lane RX1	i1				q1			

**Table 17. JESD204B Frame Format for LMFSHd = 44210**

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			
lane RX2	i1			
lane RX3	q1			

**Table 18. JESD204B Frame Format for LMFSHd = 88210**

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			
lane RX2	i1			
lane RX3	q1			



**Table 18. JESD204B Frame Format for LMFSHd = 88210 (continued)**

lane RX4	i2
lane RX5	q2
lane RX6	i3
lane RX7	q3

**Table 19. JESD204B Frame Format for LMFSHd = 24410**

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	i0				q0			
lane RX1	i1				q1			

**Table 20. JESD204B Frame Format for LMFSHd = 48410**

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	i0				q0			
lane RX1	i1				q1			
lane RX2	i2				q2			
lane RX3	i3				q3			

**Table 21. JESD204B Frame Format for LMFSHd = 24310**

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30
Nibble	1	2	3	4	5	6
lane RX0	i0			q0		
lane RX1	i1			q1		

**Table 22. JESD204B Frame Format for LMFSHd = 48310**

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30
Nibble	1	2	3	4	5	6
lane RX0	i0			q0		
lane RX1	i1			q1		
lane RX2	i2			q2		
lane RX3	i3			q3		

### 8.3.7 SYNC Interface

The DAC38RFxx JESD204B interface has two differential  $\overline{\text{SYNC}}$  outputs called  $\overline{\text{SYNC0}}$  and  $\overline{\text{SYNC1}}$  to support one or two links. Alternatively, GPO0 and GPO1 can be used to output SYNC as a single-ended CMOS level. Each of the differential or CMOS outputs is enabled by a 2-bit register (fields GPO0\_SEL, GPO1\_SEL, SYNC0B\_SEL, SYNC1B\_SEL in register IO\_CONFIG 8.5.2), with bit 0 enabling multi-DUC1  $\overline{\text{SYNC}}$  and bit 1 enabling multi-DUC2  $\overline{\text{SYNC}}$ . If both are enabled, the SYNC\ signals are OR'ed.

The  $\overline{\text{SYNC}}$  signal can be asserted low by the receiver either to make a synchronization request to initialize/reinitialize the link or to report an error to the transmitter. Synchronization requests must have a minimum duration of five frames plus nine octets rounded up to the nearest whole number of frames. To report an error, the SYNC signal is asserted for exactly two frames. The transmitter interprets any negative edge of its  $\overline{\text{SYNC}}$  input as an error and any  $\overline{\text{SYNC}}$  assertion lasting four frames or longer as a synchronization request. See the following sections in the standard for more details.

- 7.6.3 Errors requiring re-initialization
- 7.6.4 Error reporting via  $\overline{\text{SYNC}}$  interface
- 8.4  $\overline{\text{SYNC}}$  signal decoding

### 8.3.8 Single or Dual Link Configuration

The DAC38RFxx JESD204B interface can be configured with one or two links. The advantage of using two links, one for each DAC, is that one link can be re-established without affecting the other link and DAC.

The configuration for each mode of operation are:

1. Dual DAC, dual link
  - (a) Program fields OCTETPATH0\_SEL to OCTETPATH7\_SEL in multi-DUC paged registers JESD\_CROSSBAR1 (8.5.57) and JESD\_CROSSBAR2 (8.5.58) so that each multi-DUC will pick data off of the appropriate SERDES lane.
  - (b) Appropriate bits in field LANE\_ENA in multi-DUC paged register JESD\_LN\_EN (8.5.45) must be set for each multi-DUC enable the lanes used.
  - (c) Field ONE\_DAC\_ONLY in register RESET\_CONFIG (8.5.1) should be '0' (default).
2. Dual DAC, single link
  - (a) Program OCTETPATH0\_SEL to OCTETPATH7\_SEL in multi-DUC paged registers JESD\_CROSSBAR1 (8.5.57) and JESD\_CROSSBAR2 (8.5.58) so that each multi-DUC will pick data off the appropriate SERDES lane.
  - (b) Appropriate bits in field LANE\_ENA in multi-DUC paged register JESD\_LN\_EN (8.5.45) must be set for each multi-DUC enable the lanes used.
  - (c) Set field ONE\_LINK\_ONLY to '1' to configure TXENABLE output.
3. Single DAC, single link
  - (a) Set Field ONE\_DAC\_ONLY in register RESET\_CONFIG (8.5.1) to '1' to gate clocks to unused multi-DUC2 for power savings.
  - (b) ONE\_LINK\_ONLY bit does not matter in this case.

### 8.3.9 Multi-Device Synchronization

In many applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that the latency across the link is deterministic and multiple DAC devices are completely synchronized such that their outputs are phase aligned. The DAC38RFxx achieves the deterministic latency using SYSREF (JESD204B Subclass 1).

SYSREF is generated from the same clock domain as DACCLK. After having resynchronized its local multiframe clock (LMFC) to SYSREF, the DAC will request a link re-initialization via SYNC interface. Processing of the signal on the SYSREF input can be enabled and disabled via the SPI interface.

The SYSREF capture circuit and the timing requirements relative to device clock are described in [SYSREF Capture Circuit](#).

### 8.3.10 SYSREF Capture Circuit

The JESD204B standard for Device Subclass 1 introduces a SYSREF signal that can be used as a global timing reference to align the phase of the internal local multiframe clock (LMFC) and frame clock across multiple devices. This allows the system to achieve deterministic latency and align data samples across several data converters. The SYSREF signal accomplishes this goal by identifying a device clock edge for each chip that can be used as an alignment reference. In particular, the LMFC and frame clock align to the device clock edge upon which the SYSREF transition from “0” to “1” is sampled. SYSREF may be periodic, one-shot, or “gapped” periodic and its period must be a multiple of the LMFC period.

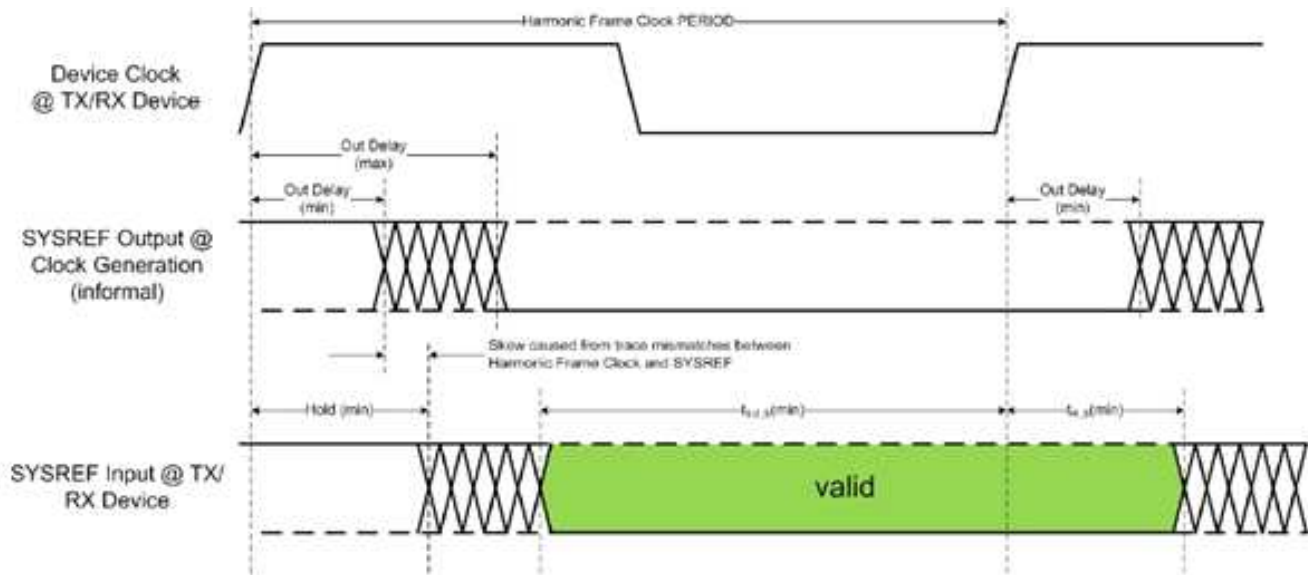


Figure 29. SYSREF Signal Timing

With high-speed device clocks, the phase of the SYSREF signals relative to the device clock must meet the setup/hold time requirements of each individual device clock. Historically, this has been done by controlling the board-level routing delay and/or employing commercial clock distribution capable of generating device clocks and SYSREF signals with programmable delays and with the option of splitting SYSREF into multiple SYSREFS, each with its own fine-tuned delay. Since the DAC38RFxx family supports device clock frequencies up to 9 GHz, a SYSREF capture circuit is included in the DAC38RFxx that allows a relaxation in meeting the device clock setup and hold.

The SYSREF capture circuit provides:

- tolerance to manufacturing and environmental variations in SYSREF phase
- immunity to sampling errors due to setup/hold/meta-stability
- information about phase of SYSREF relative to DAC clock inside the data converter
- software compensation for phase misalignment due to PCB design errors

The concepts behind the SYSREF capture scheme are illustrated in [Figure 30](#).

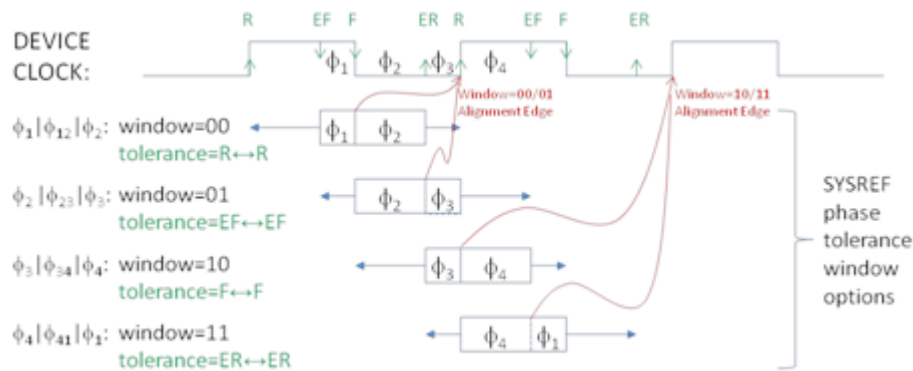


Figure 30. SYSREF Capture Strategy and Phase Tolerance Windows

To understand Figure 30, to begin with we'll ignore the SYSREF phase tolerance windows in the lower portion of the figure and focus on the blue clock waveform at the top of the figure. This waveform represents the device clock input to a particular DAC chip. The green arrows, labeled "R" and "F", correspond to the rising and falling edges of this clock (ignoring for the moment the additional arrows labeled "ER" and "EF"). Lower frequency devices captured SYSREF only on the rising edge of the device clock, the new scheme samples SYSREF on the falling edge as well, which provides more flexibility when optimizing the setup and hold time of the SYSREF capture path. Moreover, each time a rising SYSREF edge is captured, the chip remembers the clock phase during which the event occurred, and the system designer can later read back the phase information to observe the SYSREF timing relative to the device clock at the internal capture point. If SYSREF transitions close to the rising or falling clock edge sampling points the capture flop setup and hold time may not be met and the observed phase may be unreliable and subject to meta-stability phenomenon.

To reduce the sensitivity to setup/hold/meta-stability concerns an "early" version of the device clock is generated within the DAC and additional SYSREF samples are taken at the "early falling" and "early rising" edges of the clock (labeled "EF" and "ER", respectively, in Figure 30). The resulting set of four samples is used to narrow down the timing of the rising SYSREF edge to one of four possible clock phases. If the rising SYSREF transition takes place between the "EF" and "F" samples, then SYSREF is said to occur in phase 01. Similarly, if it takes place between the "F" and "ER" samples, then it is said to occur in phase 02. If SYSREF transitions between the "ER" and "R" samples, then it is said to occur in phase 03. And, finally, if the SYSREF rising edge event happens between the "R" and "EF" samples, then it is said to occur in phase 04. As mentioned before, the chip remembers all observed SYSREF phases and the user can later read them back. Since the delay between "early" and "on time" versions of the clock is intentionally chosen to be larger than the setup/hold/meta-stability window, at most one of the four samples can be affected even when the SYSREF transitions right at one of the four sampling points. Thus, the uncertainty in the observed SYSREF timing is limited to adjacent phases, and with twice as many sampling phases the resolution of the timing information is improved by a factor of two.

Referring to the lower portion of Figure 30, the user can now see how this information regarding the observed SYSREF phases is used to devise a reliable SYSREF capture methodology with a high degree of tolerance to manufacturing and environmental variations in SYSREF phase. Based on the SYSREF phases observed for a particular DAC chip during system characterization, the system designer can select one of four so-called "phase tolerance window" options (denoted "00", "01", "10", and "11") to maximize immunity to manufacturing and environmental variations. For example, consider the default phase tolerance window labeled "window=00" in the figure. If, during characterization, the system designer observes (by reading back the recorded phase observations) that the rising SYSREF edge nominally occurs in either 01 or 02 or both (i.e. 012) then he would program that particular DAC chip to use phase tolerance window "00". This mapping is indicated in the figure with the label "01|012|02: window=00". Having programmed the device to use window "00", all future SYSREF events that occur in 01 or 02 would trigger the LMFC and frame clock to be aligned using the following rising clock edge as the alignment reference (as indicated by the red arrow pointing to rising clock edge "R" and labeled "Window=00/01 alignment edge").

The full extent of each phase tolerance window is indicated in the figure using “box and whisker” plots. For the “window=00” example, the “box” portion of the plot indicates that the phase tolerance window is centered on  $\theta_{12}$  (to be precise on the boundary between  $\theta_1$  and  $\theta_2$ ) and the “whisker” portion indicates that even if the rising edge of SYSREF occurs as early as the preceding  $\theta_4$  or as late as the following  $\theta_3$  it still results in LMFC and frame clock alignment to the same rising clock edge indicated by the red arrow labeled “Window=00/01 alignment edge”. When programmed for phase tolerance window “00”, the DAC chip is tolerant to variations in the SYSREF timing ranging from a rising SYSREF edge that occurs just after one rising edge of clock to just before the next rising edge of the clock. The qualifying phrases “just after” and “just before” are used here to indicate that the SYSREF transition must occur far enough away from the rising edges of the clock to avoid setup/hold violations and prevent the device from concluding that the SYSREF transition has crossed out of the phase tolerance window when in fact it has not. The tolerance range for window “00” is from rising clock edge to rising clock edge and is indicated in the figure by the green text labeled “tolerance = R↔R”.

Following the above example, if characterization reveals SYSREF timing centered on  $\theta_{23}$  then phase tolerance window “01” (with tolerance for SYSREF rising edge events from EF to EF) should be chosen. Notice that this option is tolerant even to rising SYSREF edges that occur after the rising device clock edge (i.e. in  $\theta_4$ ) and will treat them just as if they had occurred in one of the earlier three phases, aligning to the same rising device clock edge indicated by the red arrow labeled “Window=00/01 Alignment Edge”. This allows the system designer to tolerate PCB design errors and/or environmental and manufacturing variations – achieving his intended alignment without having to make physical changes to the board to adjust the SYSREF timing.

Similarly, if characterization indicates that SYSREF timing is centered on  $\theta_{34}$  or  $\theta_{41}$  then phase tolerance window “10” or “11” can be selected, resulting in tolerance for “F↔F” or “ER↔ER” SYSREF timing, respectively. Note, however, that in these two cases the alignment reference edge is by default taken to be the subsequent rising edge of the device clock. Since this may not be the desired behavior, the DAC38Fxx allows the user to program in an optional alignment offset of  $\theta_1$  if the default offset of 0 does not achieve the desired alignment. This feature is illustrated in Figure 31 where the user can see that by setting the alignment offset to -1, phase tolerance windows “10” and “11” can be made to trigger alignment to the earlier rising device clock edge used by windows “00” and “01”. Alternatively, the window “00” and “01” alignment edge can be pushed one cycle later by setting their alignment offset to +1.

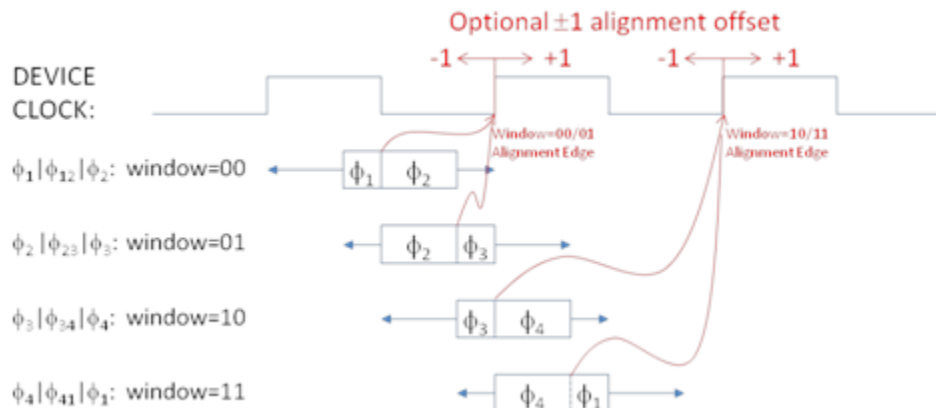


Figure 31. Optional SYSREF Alignment Offset

Several important controls related to SYSREF alignment and capture timing are contained in register SYSR\_CAPTURE (8.5.78). For example, as mentioned before, the device is capable of monitoring the observed phases of the rising SYSREF edge events; however, in order to avoid unwanted noise coupling from the SYSREF circuits into the DAC output, the SYSREF monitoring circuits are disabled by default. Field SYSR\_STATUS\_ENA enables SYSREF status monitoring. Field SYSR\_PHASE\_WDW contains the the phase tolerance window selected for normal operation, which is optimized during characterization. Field SYSR\_ALIGN\_DLY contains the control that allows the system designer to optionally offset the SYSREF alignment event by  $\pm 1$  device clock cycles. Field SYSR\_STATUS\_ENA enables the SYSREF capture alignment accumulation and will generate alarms when enabled. Writing a “1” to field SYSR\_ALIGN\_SYNC clears the accumulated SYSREF alignment statistics. The SYSREF alignment block can be bypassed completely by field SYSREF\_BYPASS\_ALIGN, in which case SYSREF is latched by the rising edge of DACCLK.

When field SYSR\_STATUS\_ENA is high the device records the phase associated with each SYSREF event for use in characterizing the SYSREF capture timing and selecting an appropriate phase tolerance window. The phase data is available in two forms. First, each of the four phases has a corresponding “sticky” alarm flag indicating which phases have been observed since the last time the register was cleared. In addition, the device also accumulates statistics on the relative number of occurrences of each phase spanning multiple SYSREF events using saturating 8-bit counters. These accumulated real-time SYSREF statistics allow us to account for time-varying effects during characterization such as potential timing differences between the 1st and Nth edges in a “gapped” SYSREF pulse train. The counters are fields PHASE1\_CNT and PHASE2\_CNT in register SYSREF12\_CNT (8.5.10), PHASE3\_CNT and PHASE4\_CNT in register SYSREF34\_CNT (8.5.11), and ALIGN\_TO\_R1\_CNT and ALIGN\_TO\_R3\_CNT in register SYSREF\_ALIGN\_R (8.5.9).

The accumulated SYSREF statistics can be cleared by writing ‘1’ to SYSR\_ALIGN\_SYNC. This sync signal affects only the SYSREF statistics monitors and does not cause a sync of any other portions of the design. Before collecting phase statistics, the user must first enable the SYSREF status monitoring logic by setting the SYSR\_STATUS\_ENA bit. The user must then generate a repeating SYSREF input before using SYSR\_ALIGN\_SYNC to clear the statistic counters. This is necessary to flush invalid data out of the status pipeline.

The “sticky” alarm flags indicating which of the four phases have been observed since the last SYSR\_ALIGN\_SYNC write of ‘1’ are fields ALM\_SYSRPHASE1 to ALM\_SYSRPHASE4 and are contained in the ALM\_SYSREF\_DET register (8.5.6).

### 8.3.11 JESD204B Subclass 0 support

Some functionality has been implemented to support Subclass 0 operation. Note that programming the SUBCLASSV configuration parameter has no functional impact on the logic. The value programmed for SUBCLASSV is only used in the initial lane alignment (ILA) sequence. The following configuration parameters are used to support Subclass 0 operation:

- Field SYSREF\_MODE in register JESD\_SYSR\_MODE (8.5.56) = 0
- Field DISABLE\_ERR\_RPT in register JESD\_ERR\_OUT (8.5.53) = 1
- Field MIN\_LATENCY\_ENA in register JESD\_MATCH (8.5.50) = 1

### 8.3.12 SerDes Test Modes through Serial Programming

The DAC38RFxx supports a number of basic pattern generation and verification of SerDes via the serial interface. Three pseudo random bit stream (PRBS) sequences are available, along with an alternating 0/1 pattern and a 20-bit user-defined sequence. The  $2^7 - 1$ ,  $2^{31} - 1$  or  $2^{23} - 1$  sequences implemented can often be found programmed into standard test equipment, such as a Bit Error Rate Tester (BERT). Pattern generation and verification selection is via field TESTPATT in register SRDS\_CFG1 (8.5.86), as shown in Table 23.

**Table 23. SerDes Test Pattern Selection**

TESTPATT	EFFECT
000	Test mode disabled.
001	Alternating 0/1 Pattern. An alternating 0/1 pattern with a period of 2 UI.
010	Verify $2^7 - 1$ PRBS. Uses a 7-bit LFSR with feedback polynomial $x^7 + x^6 + 1$ .
011	Verify $2^{23} - 1$ PRBS. Uses an ITU O.150 conformant 23-bit LFSR with feedback polynomial $x^{23} + x^{18} + 1$ .
100	Verify $2^{31} - 1$ PRBS. Uses an ITU O.150 conformant 31-bit LFSR with feedback polynomial $x^{31} + x^{28} + 1$ .
101	User-defined 20-bit pattern. Uses the USR PATT IEEE1500 Tuning instruction field to specify the pattern. The default value is 0x666666.
11x	Reserved.

Pattern verification compares the output of the serial to parallel converter with an expected pattern. When there is a mismatch, the TESTFAIL bit is driven high, which can be programmed to come out the ALARM terminal by setting field DTEST in register DTEST (8.5.76) to “0011”.

### 8.3.13 SerDes Test Modes through IEEE 1500 Programming

DAC38RFxx also provide a number of advanced diagnostic capabilities controlled by the IEEE 1500 interface. These are:

- Accumulation of pattern verification errors;
- The ability to map out the width and height of the receive eye, known as Eye Scan;
- Real-time monitoring of internal voltages and currents;

The SerDes blocks support the following IEEE1500 instructions:

**Table 24. IEEE1500 Instruction for SerDes Receivers**

INSTRUCTION	OPCODE	DESCRIPTION
ws_bypass	0x00	Bypass. Selects a 1-bit bypass data register. Use when accessing other macros on the same IEEE1500 scan chain.
ws_cfg	0x35	Configuration. Write protection options for other instructions.
ws_core	0x30	Core. Fields also accessible via dedicated core-side ports.
ws_tuning	0x31	Tuning. Fields for fine tuning macro performance.
ws_debug	0x32	Debug. Fields for advanced control, manufacturing test, silicon characterization and debug.
ws_unshadowed	0x34	Unshadowed. Fields for silicon characterization.
ws_char	0x33	Char. Fields used for eye scan.

The data for each SerDes instruction is formed by chaining together sub-components called head, body (receiver or transmitter) and tail. DAC38RFxx uses two SerDes receiver blocks R0 and R1, each of which contains 4 receive lanes (channels), the data for each IEEE1500 instruction is formed by chaining {head, receive lane 0, receive lane 1, receive lane 2, receive lane 3, tail}. A description of bits in head, body and tail for each instruction is given as follows:

#### NOTE

All multi-bit signals in each chain are packed with bits reversed e.g. mpy[7:0] in ws\_core head subchain is packed as {retime, enpll, mpy[0:7], vrangle, lb[0:1]}. All DATA REGISTER READS from SerDes Block R0 should read 1 bit more than the desired number of bits and discard the first bit received on TDO e.g., to read 40-bit data from R0 block, 41 bits should be read off from TDO and the first bit received should be discarded. Similarly, any data written to SerDes Block R0 Data Registers should be prefixed with an extra 0.

**Table 25. ws\_cfg Chain**

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
CORE_WE	Core chain write enable.
RECEIVER (FOR EACH LANE 0, 1, 2, 3)	
CORE_WE	Core chain write enable.
TUNING_WE	Tuning chain write enable.
DEBUG_WE	Reserved.
CHAR_WE	Char chain write enable.
UNSHADOWED_WE	Reserved.
TAIL (ENDING WITH THE LSB OF CHAIN)	
CORE_WE	Core chain write enable.
TUNING_WE	Tuning chain write enable.
DEBUG_WE	Reserved.
RETIME	No function.
CHAIN LENGTH = 26 BITS	

**Table 26. ws\_core Chain**

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
ENPLL	PLL enable.
MPY[7:0]	PLL multiply.
VRANGE	VCO range.
ENDIVCLK	Enable DIVCLK output
LB[1:0]	Loop bandwidth
RECEIVER (FOR EACH LANE 0,1,2,3)	
ENRX	Receiver enable.
SLEEPRX	Receiver sleep mode.
BUSWIDTH[2:0]	Bus width.
RATE[1:0]	Operating rate.
INVPAIR	Invert polarity.
TERM[2:0]	Termination.
ALIGN[1:0]	Symbol alignment.
LOS[2:0]	Loss of signal enable.
CDR[2:0]	Clock/data recovery.
EQ[2:0]	Equalizer.
EQHLD	Equalizer hold.
ENOC	Offset compensation.
LOOPBACK[1:0]	Loopback.
BSINRXP	Boundary scan initialization.
BSINRXN	Boundary scan initialization.
RESERVED	Reserved.
Testpatt[2:0]	Test pattern selection.
TESTFAIL	Test failure (real time).
LOSTDTC	Loss of signal detected (real time).
BSRXP	Boundary scan data.
BSRXN	Boundary scan data.
OCIP	Offset compensation in progress.
EQOVER	Receiver signal over equalized.
EQUUNDER	Receiver signal under equalized.
LOSTDTC	Loss of signal detected (sticky).
SYNC	Re-alignment done, or aligned comma output (sticky).
RETIME	No function.
TAIL (ENDING WITH THE LSB CHAIN)	
CLKBYP[1:0]	Clock bypass.
SLEEPPLL	PLL sleep mode.
RESERVED	Reserved.
LOCK	PLL lock (real time).
BSINITCLK	Boundary scan initialization clock.
ENBSTX	Enable TX boundary scan.
ENBSRX	Enable RX boundary scan.
ENBSPT	RX pulse boundary scan.
RESERVED	Reserved.
NEARLOCK	PLL near to lock.
UNLOCK	PLL lock (sticky).



**Table 26. ws\_core Chain (continued)**

FIELD	DESCRIPTION
CFG OVR	Configuration over-ride.
RETIME	No function.
CHAIN LENGTH = 196 BITS	

**Table 27. ws\_tuning Chain**

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
RECEIVER (FOR EACH LANE 0,1,2,3)	
PATTERRTHR[2:0]	Resync error threshold.
PATT TIMER	PRBS timer.
RXDSEL[3:0]	Status select.
ENCOR	Enable clear-on-read for error counter.
EQZERO[4:0]	EQZ OVRi Equalizer zero.
EQZ OVR	Equalizer zero over-ride.
EQLEVEL[15:0]	EQ OVRi Equalizer gain observe or set.
EQ OVR	Equalizer over-ride.
EQBOOST[1:0]	Equalizer gain boost.
RXASEL[2:0]	Selects amux output.
TAIL (ENDING WITH THE LSB CHAIN)	
ASEL[3:0]	Selects amux output.
USR PATT[19:0]	User-defined test pattern.
RETIME	No function.
CHAIN LENGTH = 174 BITS	

**Table 28. ws\_char Chain**

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
RECEIVER (FOR EACH LANE 0,1,2,3)	
TESTFAIL	Test failure (sticky).
ECOUNT[11:0]	Error counter.
ESWORD[7:0]	Eye scan word masking.
ES[3:0]	Eye scan.
ESPO[6:0]	Eye scan phase offset.
ES BIT SELECT[4:0]	Eye scan compare bit select.
ESVO[5:0]	Eye scan voltage offset.
ESVO OVR	Eye scan voltage offset override.
ESLEN[1:0]	Eye scan run length.
ESRUN	Eye scan run.
ESDONE	Eye scan done.
TAIL (ENDING WITH THE LSB CHAIN)	
RETIME	No function.
CHAIN LENGTH = 194 BITS	

### 8.3.14 Error Counter

All receive channels include a 12-bit counter for accumulating pattern verification errors. This counter is accessible via the ECOUNT IEEE1500 Char field. It is an essential part of the eye scan capability (see the [Eye Scan](#) section).

The counter increments once for every cycle that the TESTFAIL bit is detected. The counter does not increment when at its maximum value (i.e., all 1s). When an IEEE1500 capture is performed, the count value is loaded into the ECOUNT scan elements (so that it can be scanned out), and the counter is then reset, provided NCOR is set high.

ECOUNT can be used to get a measure of the bit error rate. However, as the error rate increases, it becomes less accurate due to limitations of the pattern verification capabilities. Specifically, the pattern verifier checks multiple bits in parallel (as determined by the Rx bus width), and it is not possible to distinguish between 1 or more errors.

### 8.3.15 Eye Scan

All receive channels provide features which facilitate mapping the received data eye or extracting a symbol response. A number of fields accessible via the IEEE1500 Char scan chain allow the required low level data to be gathered. The process of transforming this data into a map of the eye or a symbol response must then be performed externally, typically in software.

The basic principle used is as follows:

- Enable dedicated eye scan input samplers, and generate an error when the value sampled differs from the normal data sample;
- Apply a voltage offset to the dedicated eye scan input samplers, to effectively reduce their sensitivity;
- Apply a phase offset to adjust the point in the eye that the dedicated eye scan data samples are taken;
- Reset the error counter to remove any false errors accumulated as a result of the voltage or phase offset adjustments;
- Run in this state for a period of time, periodically checking to see if any errors have occurred;
- Change voltage and/or phase offset, and repeat.

Alternatively, the algorithm can be configured to optimize the voltage offset at a specified phase offset, over a specified time interval.

Eye scan can be used in both synchronous and asynchronous systems, while receiving normal data traffic. The IEEE1500 Char fields used to directly control eye scan and symbol response extraction are ES, ESWORD, ES BIT SELECT, ESLEN, ESPO, ESVO, ESVO OVR, ESRUN and ESDONE. Eye scan errors are accumulated in ECOUNT.

The required eyescan mode is selected via the ES field, as shown in [Table 29](#). When enabled, only data from the bit position within the 20-bit word specified via ES BIT SELECT is analyzed. In other words, only eye scan errors associated with data output at this bit position will accumulate in ECOUNT. The maximum legal ES BIT SELECT is 10011.

**Table 29. Eye Scan Mode Selection**

ES[3:0]	EFFECT
0000	Disabled. Eye scan is disabled.
0x01	Compare. Counts mismatches between the normal sample and the eye scan sample if ES[2] = 0, and matches otherwise.
0x10	Compare zeros. As ES = 0x01, but only analyses zeros, and ignores ones.
0x11	Compare ones. As ES = 0x01, but only analyses ones, and ignores zeroes.
0100	Count ones. Increments ECOUNT when the eye scan sample is a 1.
1x00	Average. Adjusts ESVO to the average eye opening over the time interval specified by ESLEN. Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.
1001 1110	Outer. Adjusts ESVO to the outer eye opening (i.e. lowest voltage zero, highest voltage 1) over the time interval specified by ESLEN. 1001 analyses zeroes, 1110 analyses ones.
1010 1101	Inner. Adjusts ESVO to the inner eye opening (i.e. highest voltage zero, lowest voltage 1) over the time interval specified by ESLEN. 1010 analyses zeroes, 1101 analyses ones.

**Table 29. Eye Scan Mode Selection (continued)**

ES[3:0]	EFFECT
1x11	Timed Compare. As ES = 001x, but analyses over the time interval specified by ESLEN. Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.

When ES[3] = 0, the selected analysis runs continuously. However, when ES[3] = 1, only the number of qualified samples specified by ESLED, as shown in [Table 30](#). In this case, analysis is started by writing a 1 to ESRUN (it is not necessary to set it back to 0). When analysis completes, ESDONE is set to 1.

**Table 30. Eye Scan Run Length**

ESLen	NUMBER OF SAMPLES ANALYZED
00	127
01	1023
10	8095
11	65535

When ESVO OVR = 1, the ESVO field determines the amount of offset voltage that is applied to the eye scan data samplers associated with rxpi and rxni. The amount of offset is variable between 0 and 300 mV in increments of ~10 mV, as shown [Table 31](#). When ES[3] = 1, ESVO OVR must be 0 to allow the optimized voltage offset to be read back via ESVO.

**Table 31. Eye Scan Voltage Offset**

ESVO	OFFSET (mV)
100000	-310
...	...
111110	-20
111111	-10
000000	0
000001	10
000010	20
...	...
011111	300

The phase position of the samplers associated with rxpi and rxni, is controlled to a precision of 1/32UI. When ES is not 00, the phase position can be adjusted forwards or backwards by more than one UI using the ESPO field, as shown in [Table 32](#). In normal use, the range should be limited to ±0.5 UI (+15 to -16 phase steps).

**Table 32. Eye Scan Phase Offset**

ESPO	OFFSET (1/32 UI)
011111	+63
...	...
000001	+1
000000	0
111111	-1
...	...
100000	-64

### 8.3.16 JESD204B Pattern Test

The DAC38RFxx supports the following test patterns for JESD204B:

- Link layer test pattern by setting field JESD\_TEST\_SEQ in register JESD\_LN\_EN (8.5.45) and monitoring the lane alarms (1 = fail, 0 = pass)
  - Verify repeating /D.21.5/ high frequency pattern for random jitter (RJ)
  - Verify repeating /K.28.5/ mixed frequency pattern for deterministic jitter (DJ)
  - Verify repeating initial lane alignment (ILA) sequence
- RPAT, JSPAT or JTSPAT pattern can be verified using errors counter of 8b/10b errors produced over an amount of time to get an estimate of BER.
- Transport layer test pattern: implements a short transport layer pattern check based on  $F = 1, 2, 4$  or  $8$ . The short test pattern has a duration of one frame period and is repeated continuously for the duration of the test. Each sample has a unique value that can be identified with the position of the sample in the user data format. The sample values are such that correct sample values will never be decoded at the receiver if there is a mismatch between the mapping formats being used at the transmitter and receiver devices. This can generally be accomplished by ensuring there are no repeating sub patterns within the stream of samples being transmitted. Refer to the JESD204B standard section 5.1.6 for more details.

The DAC38RFxx expects the test samples, in a frame, transmitted by an logic device as per [Table 33](#):

**Table 33. Short Test Patterns**

JESD Mode	i0	q0	i1	q1
82121	7CB8, F431, 6DA9, E520	7CB8, F431, 6DA9, E520	n/a	n/a
42111	7CB8, F431	6DA9, E520	F871, E962	DA53, CB40
22210	7CB8	6DA9	n/a	n/a
12410	7CB8	6DA9	n/a	n/a
44210	7CB8	6DA9	7CB8	6DA9
24410	7CB8	6DA9	7CB8	6DA9
41121	7CB8, F431, 6DA9, E520			
81180	7C00, B800, F400, 3100, 6D00, A900, E500, 2000, F800, 7100, E900, 6200, DA00, 5300, CB00, 4000	n/a	n/a	n/a
24310	87C0, F4B0	D310, A960	0E50, F820	9710, 62E0
41380	87C0, F4B0, D310, A960, 0E50, F820, 9710, 62E0	n/a	n/a	n/a

The short test pattern has duration of one frame period and is repeated continuously for the duration of the test. Each sample has a unique value that can be identified with the position of the sample in the user data format. The sample values are such that correct sample values will never be decoded at the receiver if there is a mismatch between the mapping formats being used at the transmitter and receiver devices. This can generally be accomplished by ensuring there are no repeating sub patterns within the stream of samples being transmitted.

Following are the steps required to execute the short test functionality in DAC38RFxx.

1. Configure other registers, make sure clocks are up and running.
2. Start driving short test patterns
3. Clear short test alarm by writing '0' to field ALM\_FROM\_SHORTTEST in register ALM\_SYSREF\_PAP (8.5.67). This is a paged register, one for each Multi-DUC.
4. Enable short test by writing a '1' to field SHORTTEST\_ENA in register MULTIDUC\_CFG2 (8.5.14).
5. Read the short test alarm from field ALM\_FROM\_SHORTTEST in register ALM\_SYSREF\_PAP (8.5.67). This is a paged register, one for each Multi-DUC

If the alarm read from the register is high, the short test has detected an error.

### 8.3.17 Multiband DUC (multi-DUC)

Each DAC output in the DAC38RFxx is supported by a dual band digital upconverter (DUC), which is called a multi-DUC. [Figure 32](#) shows the signal processing features of each of the two multi-DUCs. The two paths are identical and independent. The SPI interface registers for the multi-DUCs are addressed through paging, with page 0 supporting multi-DUC1 and page 1 supporting multi-DUC2. Register PAGE\_SET (8.5.8) is used to set the pages. Both pages can be selected at the same time to program both multi-DUCs simultaneously with the same settings.

Each multi-DUC has 2 DUC channels, called path AB and path CD. The output of one multi-DUC can be added to the signal of the other multi-DUC to allow a configuration with 4 total DUCs summed together for 1 DAC. After quadrature modulation is a  $\sin(x)/x$  compensation filter, followed by the multiband summation block. The multiband summation block had the ability to add the signals from the other multi-DUC for a combined 4 DUCs, each with independent frequency control. The final block is an output delay block with 0 – 15 sample range.

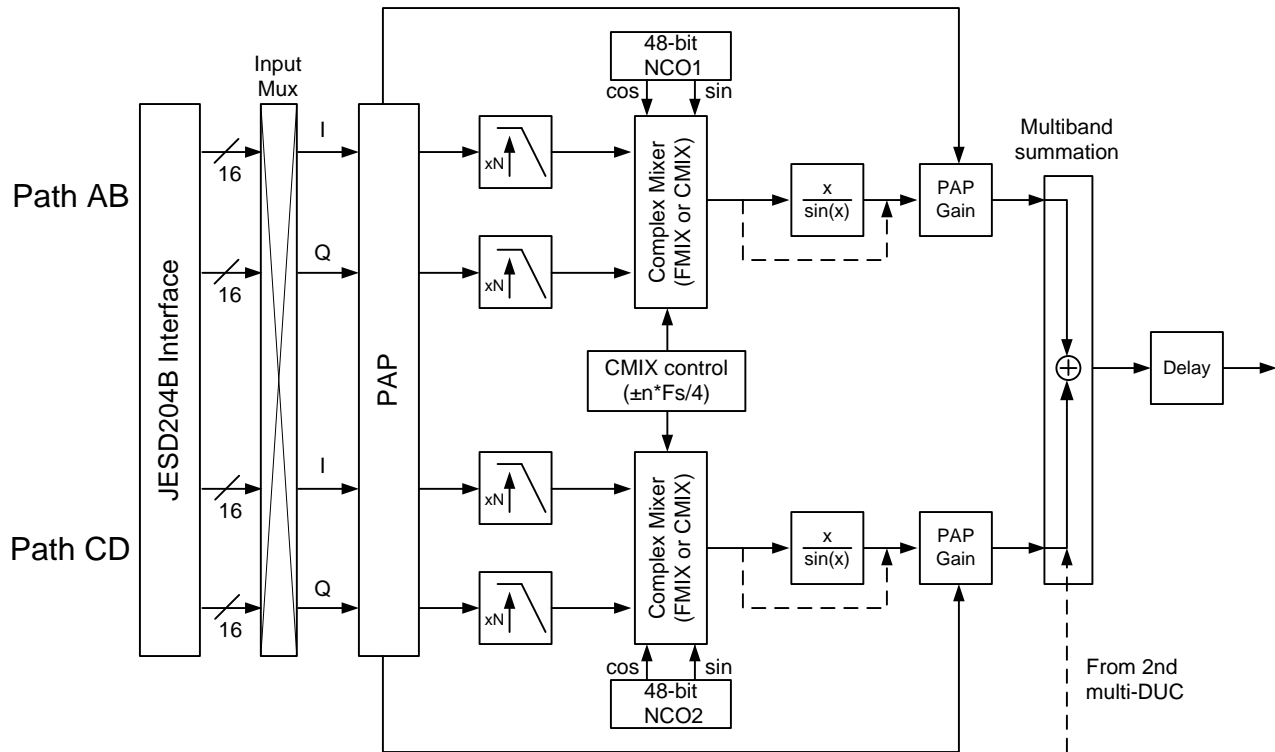


Figure 32. DAC38RFxx multi-DUC Signal Processing Block Diagram

### 8.3.17.1 Multi-DUC input

Each multi-DUC, accepts data from up to 8 Serdes lanes. A crossbar switch allows any Serdes lane to be mapped to any other Serdes lane. The crossbar switch is controlled by fields OCTETPATHx\_SEL (x = [0..7]) in Registers JESD\_CROSSBAR1 (8.5.57) and JESD\_CROSSBAR2 (8.5.58).

As shown in Table 9, the multiband DUC can be configured as either a single DUC with 1 IQ input, or a dual DUC with 2 IQ inputs, which is selected by asserting field DUAL\_IQ in register MULTIDUC\_CFG1 (8.5.13).

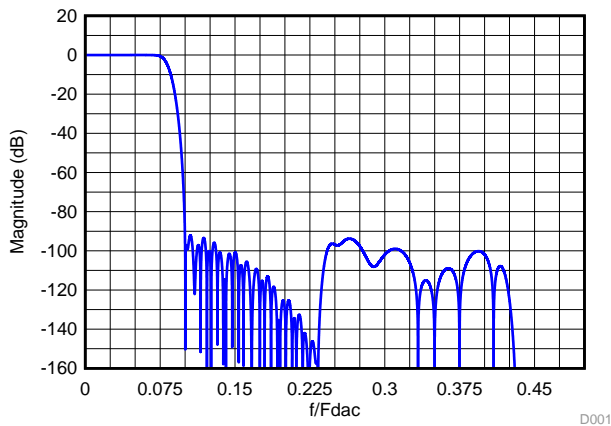
### 8.3.17.2 Interpolation Filters

The digital upconverter first increases the sample rate of the IQ signal from the input sample rate to the final DAC sample rate through a series of interpolation filters. Different sets of filters are used to achieve different rates, as shown in Table 34. The interpolation rate is selected by field INTERP in register MULTIDUC\_CFG1 (8.5.13).

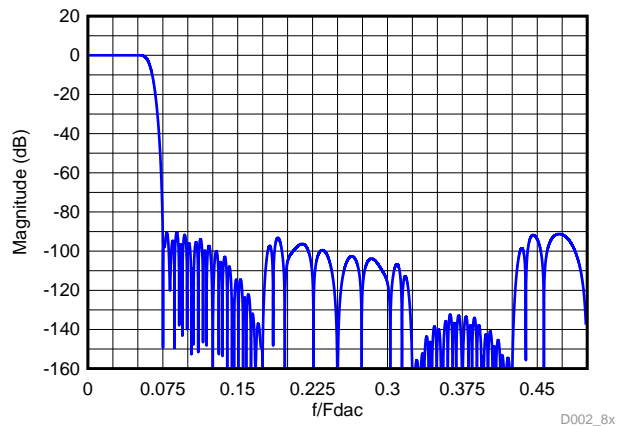
Table 34. FIR filters Used for Different Interpolation Rates

Interpolation Rate	FILTERS USED						
	FIR0 (2x)	FIR1 (2x)	LPFIR0_5X	FIR2 (2x)	LPFIR0_3X	FIR3 (2x)	LPFIR1_3X
6	x				x		
8	x	x		x		x	
10	x		x				
12	x	x					x
16	x	x		x		x	
18	x				x		x
20	x	x	x				
24	x	x		x			x

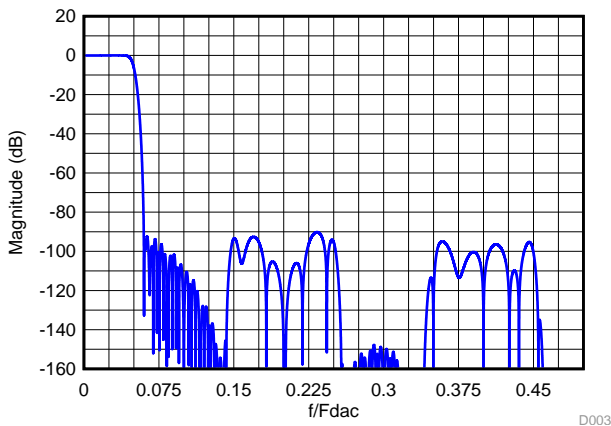
The FIR filter coefficients are shown in Table 35. The FIR filters are designed with a passband BW of  $0.4 \times f_{INPU,T}$ , a stopband attenuation of 90 dBc and ripple of  $< 0.001$  dB. The composite frequency response for each interpolation factor are shown in Figure 33 to Figure 40.



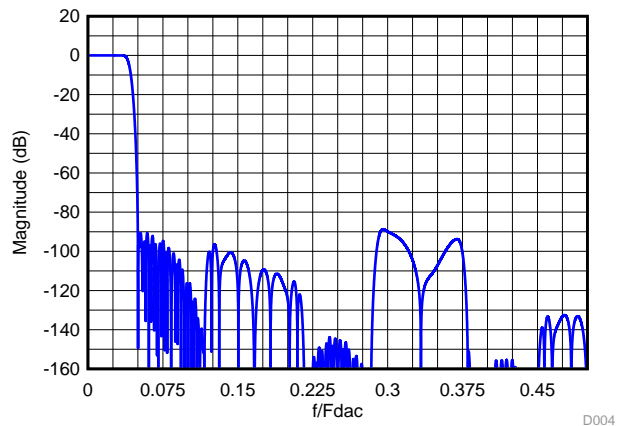
**Figure 33. Composite Magnitude Response for 6x Interpolation**



**Figure 34. Composite Magnitude Response for 8x Interpolation**



**Figure 35. Composite Magnitude Response for 10x Interpolation**



**Figure 36. Composite Magnitude Response for 12x Interpolation**

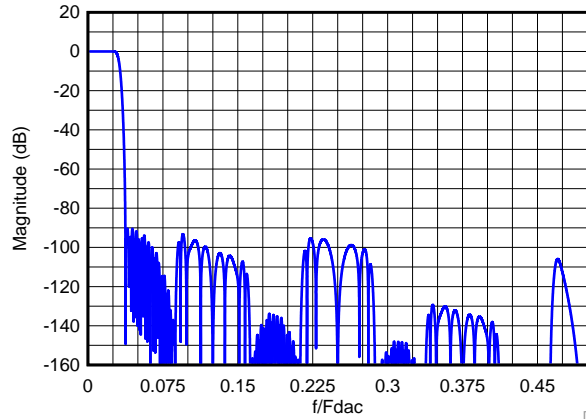


Figure 37. Composite Magnitude Response for 16x Interpolation

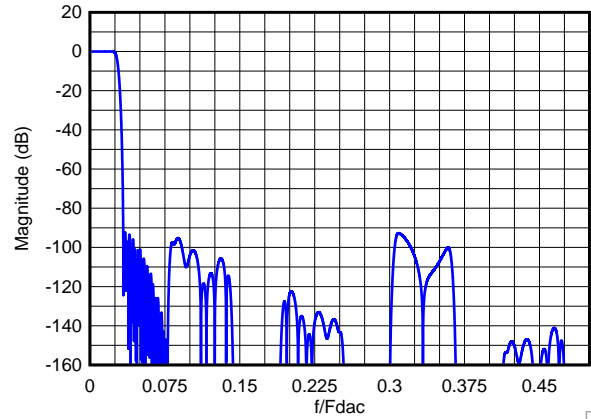


Figure 38. Composite Magnitude Response for 18x Interpolation

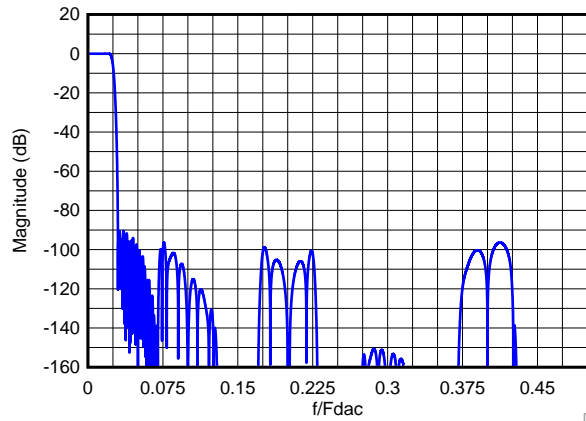


Figure 39. Composite Magnitude Response for 20x Interpolation

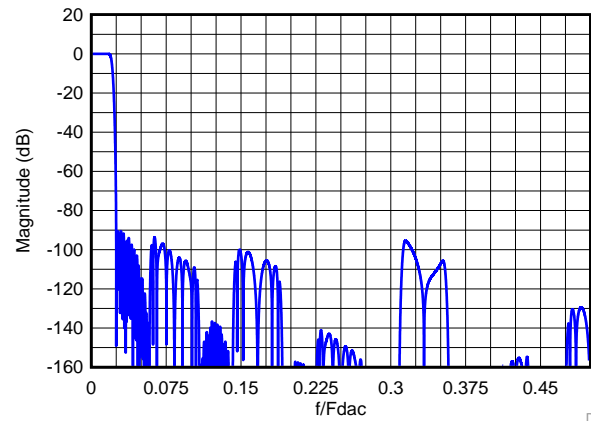


Figure 40. Composite Magnitude Response for 24x Interpolation

Table 35. FIR Filter Coefficients

tap	FIR0	FIR1	LPFIR0_5X	FIR2	LPFIR0_3X	FIR3	LPFIR1_3X	INVSINC
1	6	-12	-6	29	-14	3	25	1
2	0	0	-22	0	-61	0	88	-4
3	-19	84	-51	-214	-125	-25	22	13
4	0	0	-89	0	-95	0	-576	-50
5	47	-336	-117	1209	181	150	-1764	592
6	0	0	-106	2048	681	256	-2263	-50
7	-100	1006	-18	1209	972	150	491	13
8	0	0	171	0	347	0	8139	-4
9	192	-2691	449	-214	-1475	-25	18625	1
10	0	0	745	0	-3519	0	26365	
11	-342	10141	930	29	-3528	3	26365	
12	0	16384	841		707		18625	
13	572	10141	338		9337		8139	
14	0	0	-618		19445		491	
15	-914	-2691	-1892		26299		-2263	
16	0	0	-3147		26299		-1764	
17	1409	1006	-3872		19445		-576	



**Table 35. FIR Filter Coefficients (continued)**

tap	FIR0	FIR1	LPFIR0_5X	FIR2	LPFIR0_3X	FIR3	LPFIR1_3X	INVSINC
18	0	0	-3500		9337		22	
19	-2119	-336	-1564		707		88	
20	0	0	2121		-3528		25	
21	3152	84	7336		-3519			
22	0	0	13430		-1475			
23	-4729	-12	19426		347			
24	0		24231		972			
25	7420		26904		681			
26	0		26904		181			
27	-13334		24231		-95			
28	0		19426		-125			
29	41527		13430		-61			
30	65536		7336		-14			
31	41527		2121					
32	0		-1564					
33	-13334		-3500					
34	0		-3872					
35	7420		-3147					
36	0		-1892					
37	-4729		-618					
38	0		338					
39	3152		841					
40	0		930					
41	-2119		745					
42	0		449					
43	1409		171					
44	0		-18					
45	-914		-106					
46	0		-117					
47	572		-89					
48	0		-51					
49	-342		-22					
50	0		-6					
51	192							
52	0							
53	-100							
54	0							
55	47							
56	0							
57	-19							
58	0							
59	6							

### 8.3.17.3 JESD and Interpolation Programming

Table 36 lists the register field values required for each JESD and interpolation mode. The register field addresses are listed in Table 37.

**Table 36. Register Programming for JESD and Interpolation Mode**

Mode		Register Field Programming									
L-M-F-S-Hd 1 TX/2TX	Interp	CLKJESD_DIV	INTERP (4-0)	CLKJESD _DIV (3-0)	CLKJESD _OUT_DI V (3-0)	L_M1 (4-0)	F_M1 (7-0)	M_M1 (7-0)	S_M1 (4-0)	HD	N_M1/N' _M1 (4-0)
82121/NA	6	div24	00011	0110	0011	00111	0x00	0x01	00001	1	01111
	8	div32	00100	0111	0100						
	12	div48	00110	1010	0110						
	16	div64	01000	1011	0111						
42111/84111	6	div12	00011	0010	0011	00011	0x00	0x01	00000	1	01111
	8	div16	00100	0011	0100						
	10	div20	00101	0101	0101						
	12	div24	00110	0110	0110						
	16	div32	01000	0111	0111						
	18	div36	01001	1001	1000						
22210/44210	8	div8	00100	0001	0100	00001	0x01	0x01	00000	0	01111
	12	div12	00110	0010	0110						
	16	div16	01000	0011	0111						
	18	div18	01001	0100	1000						
	20	div20	01010	0101	1001						
12410/24410	16	div8	01000	0001	0111	00000	0x03	0x01	00000	0	01111
	24	div12	00110	0110	1010						
44210/88210	8	div8	00100	0001	0100	00011	0x01	0x03	00000	0	01111
	12	div12	00110	0010	0110						
	16	div16	01000	0011	0111						
	24	div24	01100	0110	1010						
24410/48410	16	div8	01000	0001	0111	00011	0x03	0x03	00000	0	01111
	24	div12	01100	0010	1010						
24310/48310	24	div16	01100	0011	1010	00011	0x02	0x03	00000	0	01011

**Table 37. Register Field Addresses for JESD and Interpolation Programming**

Register Field Name	Register	Register Address	Bit(s)	Hyperlink
INTERP	MULTIDUC_CFG1	0x0A	12-8	<a href="#">8.5.13</a>
CLKJESD_DIV	SERDES_CLK	0x25	15-12	<a href="#">8.5.28</a>
CLKJESD_OUT_DIV			11-8	
L_M1	JESD_K_L	0x4C	4-0	<a href="#">8.5.47</a>
F_M1	JESD_RBD_F	0x4B	7-0	<a href="#">8.5.46</a>
M_M1	JESD_M_S	0x4D	15-8	<a href="#">8.5.48</a>
S_M1			4-0	
HD	JESD_N_HD_SCR	0x4E	6	<a href="#">8.5.49</a>
N_M1			12-8	
N_M1' (NPRIME_M1)			4-0	

All registers are paged!

### 8.3.17.4 Digital Quadrature Modulator

Each DUC in the DAC38RFxx has digital quadrature modulator (DQM) blocks with independent Numerically Controlled Oscillators (NCO) that converts the complex input signal to a real signal with flexible frequency placement between 0 and  $f_{DAC}/2$ . The NCOs are enabled by fields NCOAB\_ENA and NCOCD\_ENA in register MULTIDUC\_CFG2 (8.5.14). The NCOs have 48-bit frequency registers (FREQ\_NCOAB (8.5.25) and FREQ\_NCOCD (8.5.26)) and 16-bit phase registers (PHASE\_NCOAB (8.5.23) and PHASE\_NCOCD (8.5.24)) that generate the sine and cosine terms for the complex mixing. The NCO block diagram is shown in Figure 41.

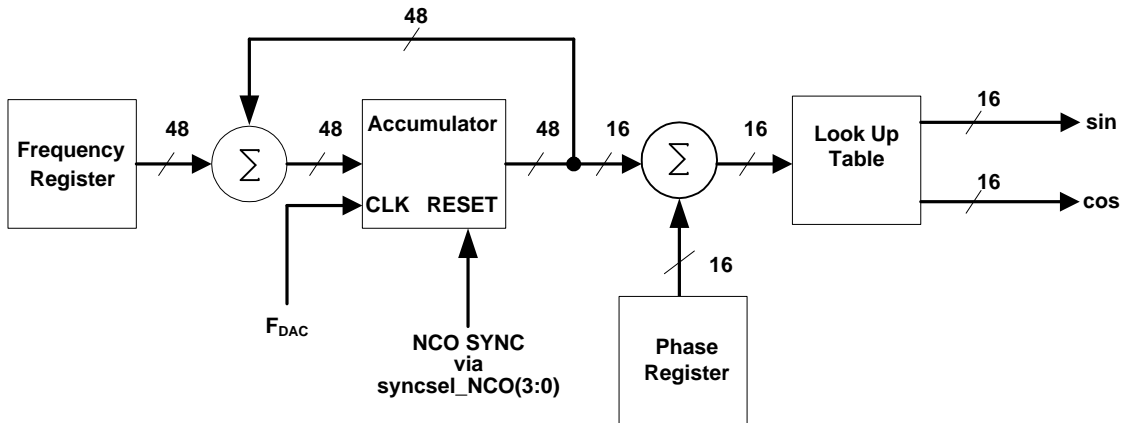


Figure 41. NCO Block Diagram

Synchronization of the NCOs occurs by resetting the NCO accumulators to zero. The synchronization source is selected by fields SYNCSEL\_NCOAB and SYNCSEL\_NCOCD in register SYNCSEL1 (8.5.29). The frequency word in the FREQ\_NCOAB and FREQ\_NCOCD registers are added to the accumulators every clock cycle,  $f_{DAC}$ .

The frequency and phase offset of the NCOs are:

$$f_{NCOAB(or CD)} = \frac{FREQ\_NCOAB(or CD) \times f_{DAC}}{2^{48}} \quad (1)$$

$$\delta_{AB(or CD)} = 2\pi \times \frac{PHASE\_NCOAB(or CD)}{2^{16}} \quad (2)$$

Treating the complex channels as complex vectors of the form  $I + jQ$ , the output of the DQM is:

$$Output_{AB} = \{I_{INPUTAB} \times \cos(2\pi f_{NCOAB}t + \delta_{AB}) - Q_{INPUTAB} \times \sin(2\pi f_{NCOAB}t + \delta_{AB})\} \times 2^{(MIXERAB\_GAIN-1)} \quad (3)$$

$$Output_{CD} = \{I_{INPUTCD} \times \cos(2\pi f_{NCOCD}t + \delta_{CD}) - Q_{INPUTCD} \times \sin(2\pi f_{NCOCD}t + \delta_{CD})\} \times 2^{(MIXERCD\_GAIN-1)} \quad (4)$$

Where  $t$  is the time since the last resetting of the NCO accumulator and the fields MIXERAB\_GAIN and MIXERCD\_GAIN in register MULTIDUC\_CFG2 (8.5.13) are either 0 or 1.

The maximum output amplitude of the DQM occurs if  $I_{IN}(t)$  and  $Q_{IN}(t)$  are simultaneously full scale amplitude and the sine and cosine arguments are equal to an integer multiple of  $\pi/4$ .

With MIXERAB\_GAIN or MIXERCD\_GAIN = 0, the gain through the DQM is  $\sqrt{2}/2$  or -3 dB. This loss in signal power is in most cases undesirable, and it is recommended that the gain function be used to increase the signal by 3 dB to compensate. With MIXERAB\_GAIN or MIXERCD\_GAIN = 1, the gain through the DQM is  $\sqrt{2}$  or +3 dB, which can cause clipping of the signal if  $I_{IN}(t)$  and  $Q_{IN}(t)$  are simultaneously near full scale amplitude and should therefore be used with caution.

### 8.3.17.5 Low Power Coarse Resolution Mixing Modes

In addition to the NCO the DAC38RFxx also has a coarse mixer block capable of shifting the input signal spectrum by the fixed mixing frequencies  $\pm N \times f_{DAC}/8$ . Using the coarse mixer instead of the full mixers will result in lower power consumption.

Treating the two complex channels as complex vectors of the form  $I(t) + jQ(t)$ , the outputs of the coarse mixer is equivalent to:

$$\text{Output}_{AB} = I_{\text{INPUTAB}} \times \cos(2\pi f_{\text{CMIX\_AB}} t) - Q_{\text{INPUTAB}} \times \sin(2\pi f_{\text{CMIX\_AB}} t) \quad (5)$$

$$\text{Output}_{CD} = I_{\text{INPUTCD}} \times \cos(2\pi f_{\text{CMIX\_CD}} t) - Q_{\text{INPUTCD}} \times \sin(2\pi f_{\text{CMIX\_CD}} t) \quad (6)$$

Where  $f_{\text{CMIX\_AB}}$  and  $f_{\text{CMIX\_CD}}$  and the fixed mixing frequency selected by fields CMIX\_AB or CMIX\_CD in register CMIX (8.5.21). The coarse mixer blocks are disabled by setting CMIX\_AB and CMIX\_CD to 0x0.

The NCO and coarse mixers can be enabled simultaneously, although this is not useful in most cases as the full frequency range can be covered by the NCO.

### 8.3.17.6 Inverse Sinc Filter

The DAC38RFxx have a 9-tap inverse Sinc filter (INVSINC) that runs at the DAC update rate ( $f_{\text{DAC}}$ ) that can be used to flatten the frequency response of the sample-and-hold output. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well known  $\sin(x)/x$  or Sinc(x) frequency response (Figure 42, red line). The inverse sinc filter response (Figure 42, blue line) has the opposite frequency response from 0 to  $0.4 \times f_{\text{DAC}}$ , resulting in the combined response (Figure 42, green line). Between 0 to  $0.4 \times f_{\text{DAC}}$ , the inverse sinc filter compensates the sample-and-hold roll-off with less than 0.03 dB error.

The inverse sinc filter has a gain  $> 1$  at all frequencies. Therefore, the signal input to INVSINC must be reduced from full scale to prevent saturation in the filter. The amount of back-off required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to INVSINC is at  $0.25 \times f_{\text{DAC}}$ , the response of INVSINC is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB to avoid saturation. The advantage of INVSINC having a positive gain at all frequencies is that the user is then able to optimize the back-off of the signal based on its frequency.

The inverse Sinc filters are enabled by fields ISFIRAB\_ENA and ISFIRCD\_ENA in register MULTIDUC\_CFG1 (9.5.9).

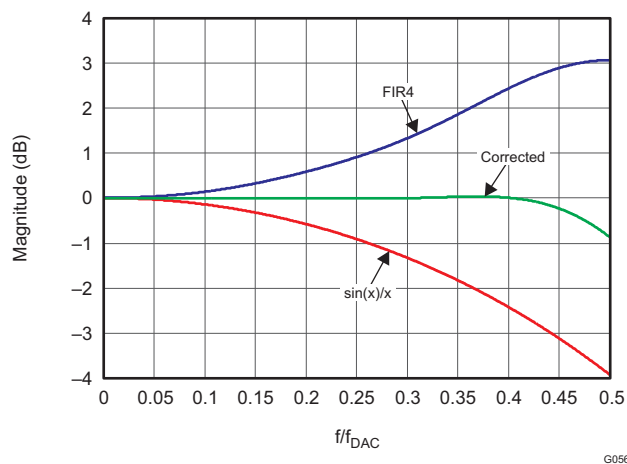


Figure 42. Composite Magnitude Spectrum for INVSINC

### 8.3.17.7 Summation Block for Dual DUC Modes

When using the dual DUC modes, the outputs of the two AQM blocks are summed together to form a composite signal for the DAC output, configured by field OUTSUM\_SEL in register OUTSUM (8.5.22). The input signals to the DUCs must be scaled such that the signal does not exceed fullscale during summation. This field can also be configured to add the signals from the adjacent multi-DUC to enable a four DUC signal.

### 8.3.18 PA Protection Block

The DAC38RFxx incorporates an optional power amplifier protection (PAP) block to monitor when the input signal is too large, for example when an interface error occurs, and reduces the output signal power of the DAC. The PAP block achieves the functionality of reducing the input signal that crosses the threshold through three main sub-blocks. These are PAP trigger generation block, PAP gain state machine and GAIN block.

The PAP block keeps track of the input signal power by maintaining a sliding window accumulation of last N samples. N is selectable to be 32, 64 or 128 based on the setting (Table 38) of fields PAPAB\_SEL\_DLY in register PAP\_CFG\_AB (8.5.35) and PAPCD\_SEL\_DLY in register PAP\_CFG\_CD (8.5.36). The average amplitude of input signal is computed by dividing accumulated value by the number of samples in the delay-line (N). The result is then compared against the threshold in fields PAPAB\_THRESH in register PAP\_CFG\_AB (8.5.35) and PAPCD\_THRESH in register PAP\_CFG\_CD (8.5.36). If the threshold is violated, gain state machine is triggered which generated gain value to ramp down the DAC output signal amplitude. After the input signal returns to normal value, the state machine ramps up the DAC output signal amplitude.

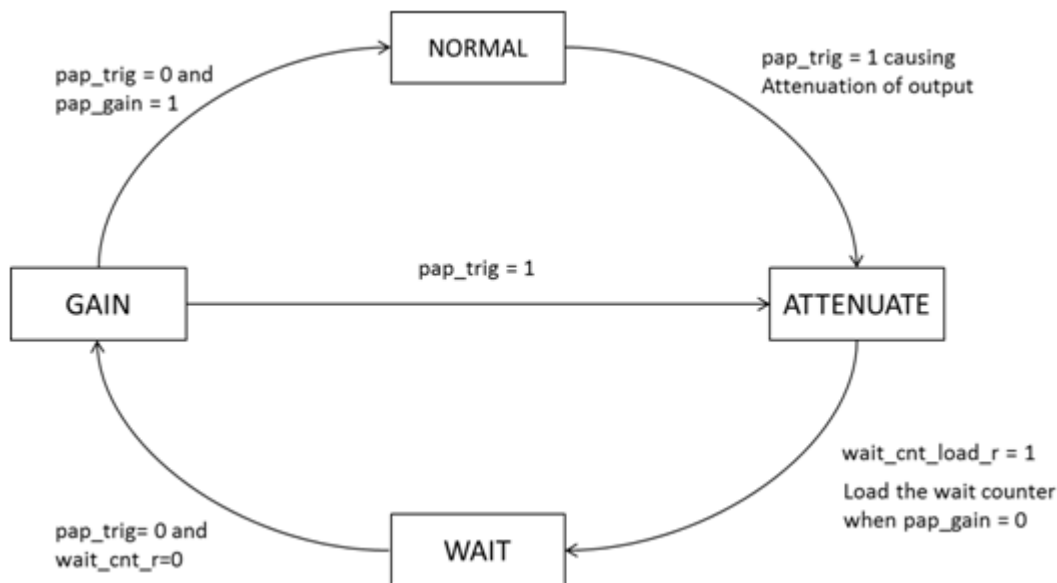
**Table 38. PAP Delay Line Selection**

pap_sel_dly[1:0]	# of samples averaged
00	32
01	64
10	128
11	Reserved

The generation of the PAP trigger as explained as follows:

- The I and Q samples are treated separately – either can trigger attenuation
- In dual DUC modes, each IQ pair is treated separately and has a separate gain block
- 8 samples at the input are put through an absolute value circuit (all 2's complement)
- Next these values are vector summed to get a 12 bit result
- Then 12 bit result is placed into the delay line and summed into the accumulator
- The accumulator is also subtracting out the delayed 12 bit word corresponding to N = 32, N = 64 or N = 128
- Finally the accumulator output is divided down by N and rounded to 13 bits. These 13 bits are compared to the threshold in the SPI registers. A pap\_trig occurs if the threshold is exceeded.

The PAP gain state machine generates the pap gain value to be applied on the output stream to reduce the output signal amplitude. The state machine below is used to control the attenuation of the DAC output and the gaining up of the signal again once the trigger is released.



**Figure 43. PAP Gain State Machine**

The normal operating condition for the PAP block is the NORMAL state in Figure 43. However, when the PAP block detects an error condition it sets the pap\_trig signal to '1' causing a state transition from NORMAL operation to the ATTENUATE state.

In the ATTENUATE state the data path gain is scaled from 1.0 down to 0.0 by a programmable step amount set by fields PAPAB\_GAIN\_STEP in register PAP\_GAIN\_AB (8.5.35) and PAPCD\_GAIN\_STEP in register PAP\_GAIN\_CD (8.5.33). This value is always positive with the decimal place located between the MSB and MSB-1. Unity is equal to “1000000000”. Each clock cycle (16 samples) the PAP\_GAIN is stepped down by PAPAB\_GAIN\_STEP and PAPCD\_GAIN\_STEP until the gain is 0.

After PAP\_GAIN is 0, the state machine moves on to the WAIT state. Here a programmable counter counts clock cycles to allow the condition for the pap\_trig to be fixed. Fields PAPAB\_WAIT in register PAP\_WAIT\_AB (8.5.32) and PAPCD\_WAIT in register PAP\_WAIT\_CD (8.5.34) are used to select the number of clock cycles (samples = 16 x PAPAB\_WAIT or 16 x PAPCD\_WAIT) to wait before moving to the next state. Once the WAIT counter equals zero and pap\_trig='0', the state machine moves on to the GAIN state. If the WAIT equals 0 but pap\_trig still equals '1' then the state machine stays in the WAIT state until pap\_trig = '0'.

### 8.3.19 Gain Block

The GAIN block also has additional output gain control through fields GAINAB in register GAINAB (8.5.35) and GAINCD in register GAINCD (8.5.40). Similar to PAP\_GAIN value, the output gain is always positive with unity when GAINAB or GAINCD = "010000000000".

To reduce the power the gain block clock has been gated whenever the pap is disabled and GAINAB or GAINCD is set to unity.

### 8.3.20 Output Summation

The OUTSUM block allows addition of samples from each DUC in the multi-DUC. It is also possible to add the output samples from the adjacent multi-DUC. Field OUTSUM\_SEL in register OUTSUM (8.5.22) controls the summation for each multi-DUC. The functionality of the block can be represented by the following equation:

$$OUTSUM_{output} = SAME_{AB} + SAME_{CD} + ADJ_{AB} + ADJ_{CD} \tag{7}$$

In order to avoid overflow, rounding operation is performed after the addition to reduce the word size back to 16-bits. Exact number of bits rounded depends on the number of channels added. Table 39 shows the description of round after the summation.

**Table 39. OUTSUM Scaling and Rounding**

# OF CHANNELS ADDED	# OF BITS ROUNDED
0	0, Use bits[15:0] from the result
1	Use bits[16:1] from the result and bit[0] used for rounding
2	Use bits[17:2] from the result and bits[1:0] used for rounding
3	Use bits[18:3] from the result and bit[2:0] used for rounding
4	Use bits[19:4] from the result and bit[3:0] used for rounding

### 8.3.21 Output Delay

The signal following output summation can be programmably delayed by 0-15 DACCLK cycles through field OUTPUT\_DELAY in register OUTSUM (8.5.20). The block takes 16 sample words (vec16) from both the A and B paths and shifts the them to 32 sample long delay line.

### 8.3.22 Polarity Inversion

The signal following the output delay can be inverted by a 2's complement conversion allowing the + and - DAC outputs to be swapped by asserting field DAC\_COMPLEMENT in register MULTIDUC\_CFG1 (8.5.13).

### 8.3.23 Temperature Sensor

The DAC38RFxx incorporates a temperature sensor block which monitors the die temperature by measuring the voltage across 2 transistors. The voltage is converted to an 8-bit digital word using a successive approximation (SAR) analog to digital conversion process. The result is scaled, limited and formatted as a twos complement value representing the temperature in degrees Celsius.

The sampling is controlled by the serial interface signals  $\overline{\text{SDEN}}$  and SCLK. If the temperature sensor is enabled by writing a 0 to field TSENSE\_SLEEP in register SLEEP\_CONFIG (8.5.70), a conversion takes place each time the serial port is written or read. The data is only read and sent out by the digital block when the temperature sensor is read in field TEMPDATA in register TEMP\_PLLVOLT (8.5.7). The conversion uses the first eight clocks of the serial clock as the capture and conversion clock, the data is valid on the falling eighth SCLK. The data is then clocked out of the chip on the rising edge of the ninth SCLK. No other clocks to the chip are necessary for the temperature sensor operation. As a result the temperature sensor is enabled even when the device is in sleep mode.

In order for the process described above to operate properly, the serial port read from register TEMP\_PLLVOLT must be done with an SCLK period of at least 1  $\mu\text{s}$ . If this is not satisfied the temperature sensor accuracy is greatly reduced.

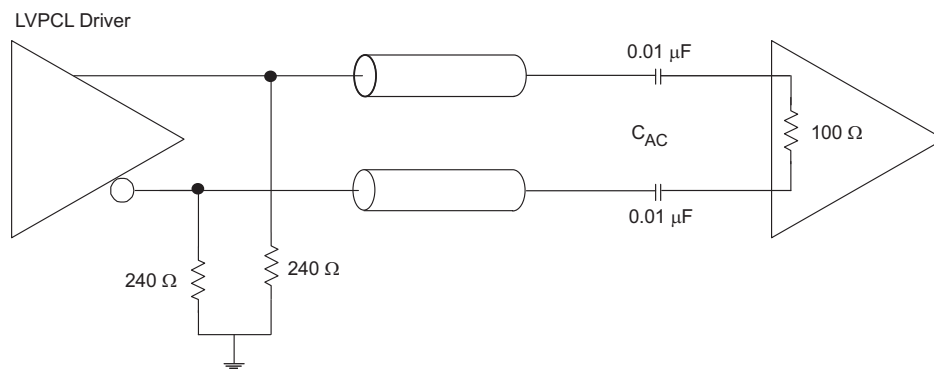
### 8.3.24 Alarm Monitoring

The DAC38RFxx includes a flexible set of alarm monitoring that can be used to alert of a possible malfunction scenario. All the alarm events can be accessed either through the SIP registers and/or through the ALARM output. Once an alarm is set, the corresponding alarm bit must be reset through the serial interface to allow further testing. The set of alarms includes the following conditions:

- JESD alarms
  - Fields ALM\_LANEx\_ERR in registers JESD\_ALM\_Lx (x = 0-7, 8.5.59 to 8.5.66):
    - multiframe alignment\_error. Occurs when multiframe alignment fails
    - frame alignment error. Occurs when multiframe alignment fails
    - link configuration error. Occurs when there is wrong link configuration
    - elastic buffer overflow. Occurs when bad RBD value is used
    - elastic buffer match error. Occurs when the first non-/K/ doesn't match the programmed data
    - code synchronization error
    - 8b/10b not-in-table decode error
    - 8b/10b disparity error
  - Field ALM\_FROM\_SHORTTEST in register ALM\_SYSREF\_PAP (8.5.67): Occurs when the short pattern test fails.
- SerDes alarms
  - Field ALM\_SD\_LOTDET in register ALM\_SD\_DET (8.5.5): Occurs when there are loss of signal detect from Serdes lanes.
  - Fields ALM\_FIFOx\_FLAGS in registers JESD\_ALM\_Lx (x = 0-7, 8.5.59 to 8.5.66):
    - FIFO write error. Occurs if write request and FIFO is full.
    - FIFO write full: Occurs if FIFO is full.
    - FIFO read error. Occurs if read request and FIFO is empty.
    - FIFO read empty: Occurs if FIFO is empty.
  - Field ALM\_SD0\_PLL in register ALM\_SYSREF\_DET (8.5.6): Occurs if the PLL in the Serdes block 0 goes out of lock.
  - Field ALM\_SD1\_PLL in register ALM\_SYSREF\_DET (8.5.6): Occurs if the PLL in the Serdes block 1 goes out of lock.
- SYSREF alarm
  - Field ALM\_SYSREF\_ERR in register ALM\_SYSREF\_PAP (8.5.67): Occurs when the SYSREF is received at an unexpected time. If too many of these occur it will cause the JESD to go into synchronization mode again.
- DAC PLL alarm
  - Field PLL\_LOCK in register ALM\_SYSREF\_DET (8.5.6). This register field is asserted when the PLL is locked. When used as an alarm output, this is inverted so a high signal indicated that the PLL is unlocked.
- PAP alarm
  - Field ALM\_PAP in register ALM\_SYSREF\_PAP (8.5.67): Occurs when the average power is above the threshold. While any alarm\_pap is asserted the attenuation for the appropriate data path is applied.

### 8.3.25 Differential Clock Inputs

Figure 44 shows the preferred configuration for driving the DACCLK+/- and SYSREF+/- with a differential ECL/PECL source.



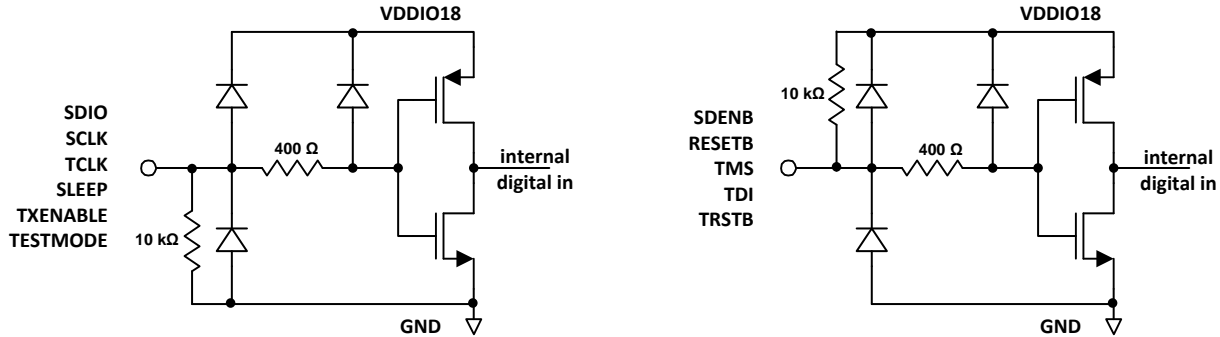
Copyright © 2016, Texas Instruments Incorporated

Figure 44. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source



### 8.3.26 CMOS Digital Inputs

Figure 45 shows a schematic of the equivalent CMOS digital inputs of the DAC38RFxx. SDIO, SCLK, TCLK, SLEEP, TESTMODE and TXENABLE have internal pull-down resistors while SDEN, RESET, TMS, TDI and TRST have internal pull-up resistors. See the Specifications table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 10 kΩ.



Copyright © 2016, Texas Instruments Incorporated

Figure 45. CMOS Digital Equivalent Input

### 8.3.27 DAC Fullscale Output Current

The DAC38RFxx uses a bandgap reference and control amplifier for biasing the full-scale output current. The DAC full scale output current is set by a combination of the fixed current through the external resistor R<sub>BIAS</sub> (connected to pin BIASJ) and current from course trim current sources:

$$I_{OUTFS} = I_{RBIAS} + I_{coarsetrim} \quad (8)$$

The bias current I<sub>BIAS</sub> through resistor R<sub>BIAS</sub> is defined by the on-chip bandgap reference voltage V<sub>BG</sub> (nominally 0.9 V) and control amplifier. For normal operation, it is recommended that R<sub>BIAS</sub> is set to 3.6 kΩ for a fixed current through R<sub>BIAS</sub> of 250 μA. This current is scaled 128x internally, giving:

$$I_{RBIAS} = 128 \times \frac{V_{BG}}{R_{BIAS}} = 128 \times \frac{0.9V}{3.6 k\Omega} = 32 mA \quad (9)$$

The course trim current sources are configured through SPI register field DACFS in register DACFS (9.5.69), as follows:

$$I_{coarsetrim} = 2mA \times (DACFS - 11) \quad (10)$$

From the discussion above, the DAC full scale output current can be configured from 40 mA (DACFS[3:0] = 1111) down to 10 mA (DACFS[3:0] = 0000).

An external decoupling capacitor C<sub>EXT</sub> of 0.1 μF should be connected externally to terminal EXTIO for compensation. R<sub>BIAS</sub> of 3.6 kΩ is recommended for setting the full-scale output current.

### 8.3.28 Current Steering DAC Architecture

The DACs in the DAC38RFxx consist of a segmented array of NMOS current sources, capable of sinking a full-scale output current up to 40 mA (see Figure 46). Differential current switches direct the current to either one of the complimentary output nodes VOUT1/2+ or VOUT1/2-. These complementary output nodes are internal to the device because of the integrated balun. Complimentary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of four.

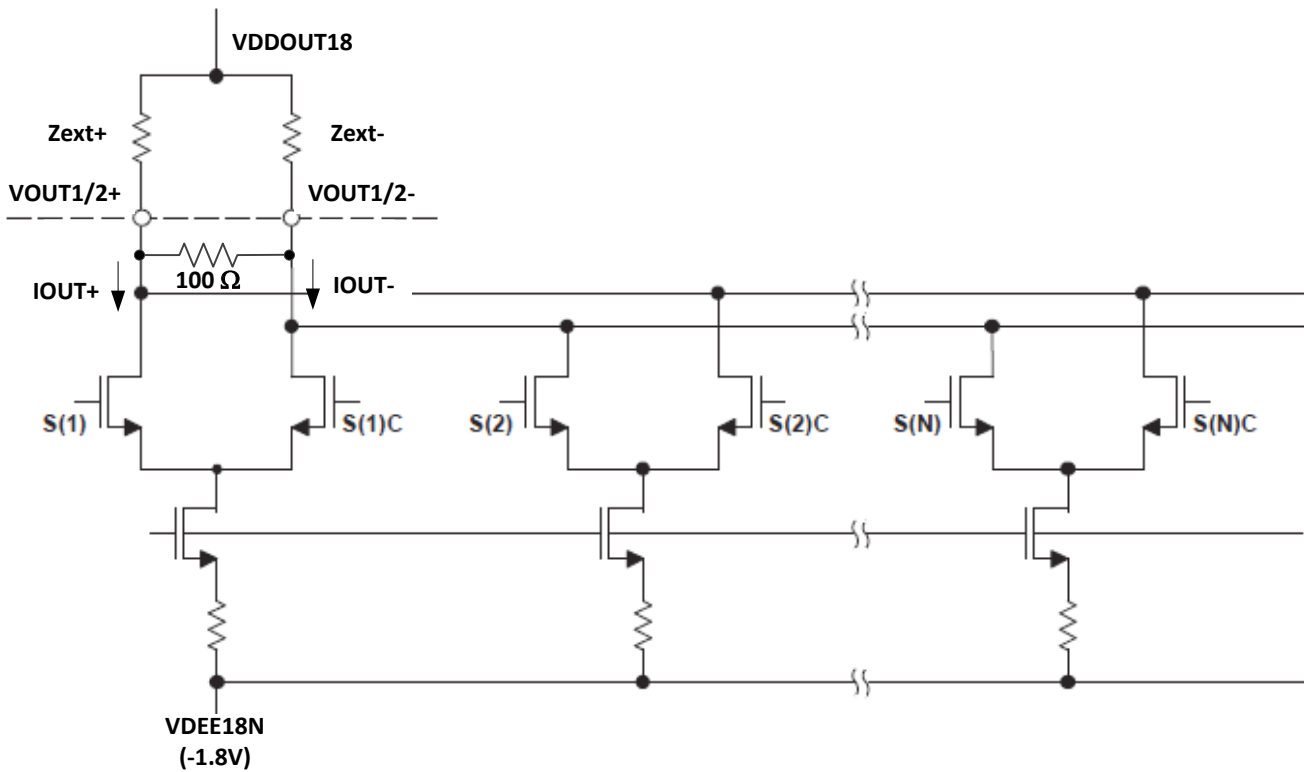


Figure 46. Current Steering DAC Architecture

Referring to Figure 46, the total output current  $IOUT_{FS}$  is fixed, and is switched to either the + or – output by switches  $S(N)$ :

$$IOUT_{FS} = IOUT_{++} + IOUT_{--} \quad (11)$$

Since the output stage is a current sinking architecture, we will denote current into the DAC as + current, and the current flows  $IOUT_{++}$  and  $IOUT_{--}$  into terminals  $VOUT1/2+$  and  $VOUT1/2-$  respectively.  $IOUT_{++}$  and  $IOUT_{--}$  can be expressed as:

$$IOUT_{++} = \frac{IOUT_{FS} \times CODE}{16384} \quad (12)$$

$$IOUT_{--} = \frac{IOUT_{FS} \times (16383 - CODE)}{16384} \quad (13)$$

where  $CODE$  is the decimal representation of the 14-bit DAC core data input word. Note the signal path up to the DAC is 16-bits and the 2 LSBs are truncated for the DAC core data input word.

### 8.3.29 DAC Transfer Function

The DAC38RFxx has a wide bandwidth integrated balun (nominally 700 MHz to 3.8 GHz passband) to convert the DAC core differential signal to a single ended signal. The single ended output is expected to drive a 50- $\Omega$  load (see Figure 47). With full-scale current of 40 mA, the theoretical output power delivered to a 50 ohms load is 4 dBm. However the actual power delivered will be less than the theoretical value and Figure 19 shows the output power across frequency.

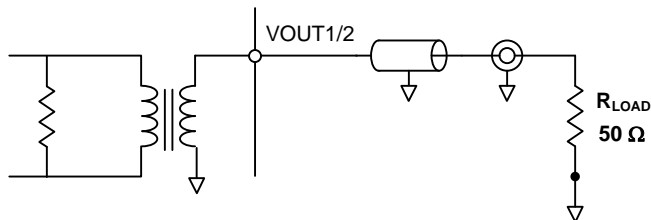


Figure 47. Driving a 50-Ω Load

## 8.4 Device Functional Modes

### 8.4.1 Clocking Modes

The DAC38RFxx has both a single ended clock input DACCLKSE and a differential clock input DACCLK+/- to clock the device. The clock input is selected by field SEL\_EXTCLK\_DIFFSE in register CLK\_PLL\_CFG (8.5.79). The DAC38RFxx can be clocked directly with a high frequency input clock at the DAC sample rate (PLL Bypass Mode), or an optional on-chip low-jitter phase-locked loop (PLL) can be used to generate the high frequency DAC sample clock internally from a lower frequency reference clock input (PLL Mode).

### 8.4.2 PLL Bypass Mode Programming

In PLL bypass mode a high quality clock is sourced to the DACCLK inputs. This clock is used to directly clock the DAC38RFxx DAC cores. This mode gives the device best performance and is recommended for extremely demanding applications.

The bypass mode is selected by setting the following:

1. Set field PLL\_ENA in register CLK\_PLL\_CFG (8.5.79) to “0” to bypass the PLL circuitry.
2. Set field PLL\_SLEEP in register SLEEP\_CONFIG (8.5.70) to “1” to put the PLL and VCO into sleep mode.

### 8.4.3 Internal PLL/VCO

The DAC38RFxx has an internal clock generation circuit consisting of a PLL and two identical VCOs connected in parallel, as shown in Figure 48.

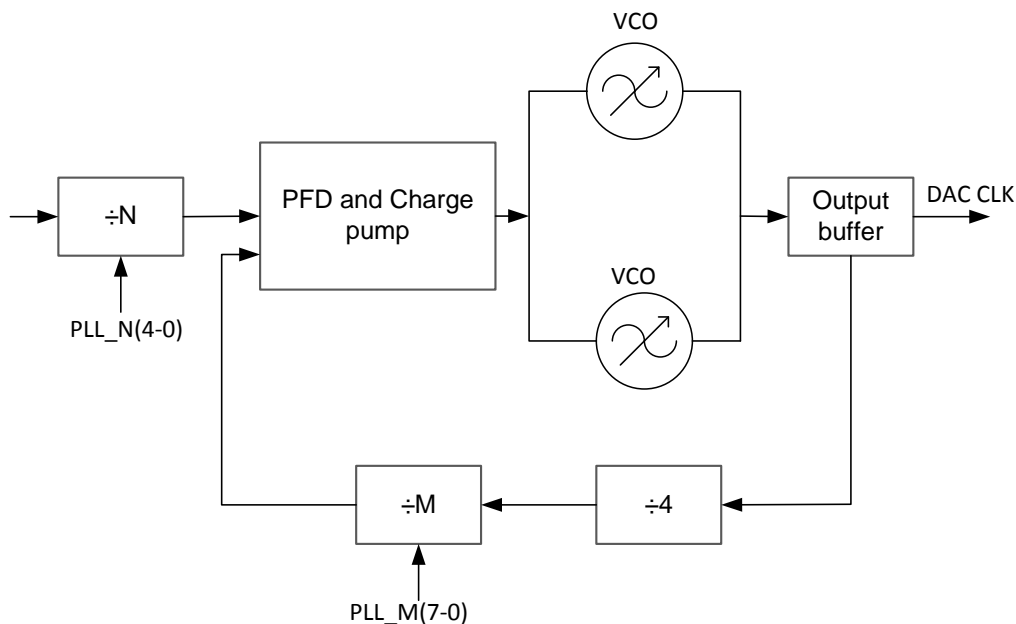


Figure 48. Internal PLL/VCO Block Diagram

## Device Functional Modes (continued)

The two parallel VCOs are tuned to a target center frequency of 5.9 GHz (low VCO) in DAC38RF87 and DAC38RF97. They are tuned to a target center frequency of 8.85 GHz (high VCO) in DAC38RF86 and DAC38RF96. The field PLL\_VCOSEL in register PLL\_CONFIG2 (8.5.81) must always be set to 0 in DAC38RF87/97 and always set to '1' in DAC38RF86/96/88/81. Also GSMPLL\_ENA in register PLL\_CONFIG2 must always be set to '1' in all devices to ensure the two identical VCOs are connected in parallel. The 7 bit VCO tuning code in field PLL\_VCO in register PLL\_CONFIG2 is used to tune the VCO frequency in the range of 5.24 GHz to 6.72 GHz for the low VCO and 7.96 GHz to 9.0 GHz for the high VCO. For the low VCO the center VCO frequency is achieved with PLL\_VCO = 63<sub>decimal</sub> and for the high VCO the target VCO center frequency is also achieved with PLL\_VCO = 63<sub>decimal</sub>.

The supply current, and therefore, the analog signal amplitude in the VCO is controlled using the field PLL\_VCO\_RDAC in register PLL\_CONFIG1 (8.5.80). This control signal should be set 15<sub>decimal</sub> initially for 18 mA supply current in the VCO and ~1.4 V<sub>PP</sub> single ended oscillation amplitude.

The PLL has no prescaler, so the DAC sample rate is the VCO frequency. In the PLL feedback path a fixed ÷ 4 frequency divider block receives the VCO output clock and divides its frequency by 4. The maximum operating frequency of the phase-frequency detector (PFD) is approximately 550 MHz. The M (feedback) clock divider takes the output clock signal from the fixed ÷4 block and divides it by a programmable ratio set by the 8-bit field in field PLL\_M\_M1 in register PLL\_CONFIG1 (8.5.80). The programmable division ratio range is ÷1 to ÷256, and is the value of the 8 bit unsigned binary code + 1. Although it is possible to program the M divider to ÷1, ÷2 and ÷3, these values should not be used. As stated previously the PFD and CP have a finite maximum operating frequency, which is the VCO frequency divided by the fixed divider ratio multiplied by the minimum allowable M divider ratio.

$$PFD\_CP_{Fmax} = F_{vco} / (Fixed\_div \times Mdiv_{min}) \tag{14}$$

The N (reference) divider determines the ratio between the input reference clock frequency and the PFD operating frequency, and is set by the 5-bit field PLL\_N\_M1 in register CLK\_PLL\_CFG (8.5.79). The division ratio range is ÷1 to ÷32, and is the value of the 5-bit unsigned binary code + 1.

The charge pump output current amplitude is set using the 4-bit field PLL\_CP\_ADJ in register PLL\_CONFIG2 (8.5.81). The current amplitude is simply the digital code multiplied by the unit current amplitude of 100 µA. In a nominal condition, with the LF VCO running at 5.898 GHz, and with the M divider set to ÷4, the PFD will run at 368.625 MHz, and the change pump current should set to 6<sub>decimal</sub>, which gives 600 µA charge pump output current for a good phase margin of 69 degrees. If a higher M ratio (for lower PFD frequencies) are required the charge pump output current must be increased to maintain good loop stability and prevent excessive peaking in the phase noise response. The charge pump output current setting PLL\_CP\_ADJ should be adjusted in relation to the feedback (M) divider ratio PLL\_M\_M1 according to the following table to maintain a constant phase margin of 69 degrees.

**Table 40. M vs Kp for Maintaining Good Stability**

M	CP_ADJ
4	6
6	9
8	12
10	15

Similarly for the HF VCO running at 8.847 GHz, and with the M divider set to ÷4, the PFD will run at 552.9375 MHz as shown above. Here the change pump current should set to 6<sub>decimal</sub>, which gives 600 µA charge pump output current for a good phase margin of 69 degrees.

### 8.4.4 CLKOUT

The DAC38RFxx has a programmable output clock on CLKTX+/- balls that is a divided version of the internal DAC sample clock, either with or without PLL. Two frequency dividers, either DACCLK/3 or DACCLK/4, are available by programming field CLK\_TX\_DIV4 in register CLK\_OUT (8.5.71). The output swing voltage is programmable from approximately 125 to 1460 mV<sub>PP-DIFF</sub> through field CLK\_TX\_SWING in register CLK\_OUT (8.5.71).

Field CLK\_TX\_IDLE in register CLK\_OUT (8.5.71) enables an idle state, in which the pins are driven to the proper common-mode levels in order to charge the external AC coupling caps but the clock output is disabled. The output clock circuit can be put to sleep by field CLK\_TX\_SLEEP in register SLEEP\_CONFIG (8.5.70).

### 8.4.5 Serial Peripheral Interface (SPI)

The serial port of the DAC38RFxx is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC38RFxx. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 terminal interface by SIF4\_ENA in register IO\_CONFIG (8.5.2). In both configurations, SCLK is the serial interface input clock and SDEN is serial interface enable. For 3 terminal configuration, SDIO is a bidirectional terminal for both data in and data out. For 4 terminal configuration, SDIO is bidirectional and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK.

The SPI registers are reset by writing a 1 to SPI\_RESET in register RESET\_CONFIG (8.5.1).

Each read/write operation is framed by signal SDEN (Serial Data Enable Bar) asserted low. The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 7-bit address to be accessed. Figure 49 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. The data transfer cycle consists of two bytes.

Figure 49. Instruction Byte of the Serial Interface

Bit	7 (MSB)	6	5	4	3	2	1	0
Description	R/W	A6	A5	A4	A3	A2	A1	A0

R/W - Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC38RFxx and a low indicates a write operation to DAC38RFxx

A6:A0 - Identifies the address of the register to be accessed during the read or write operation.

Figure 50 shows the serial interface timing diagram for a DAC38RFxx write operation. SCLK is the serial interface clock input to DAC38RFxx. Serial data enable SDEN is an active low input to DAC38RFxx. SDIO is serial data input. Input data to DAC38RFxx is clocked on the rising edges of SCLK.

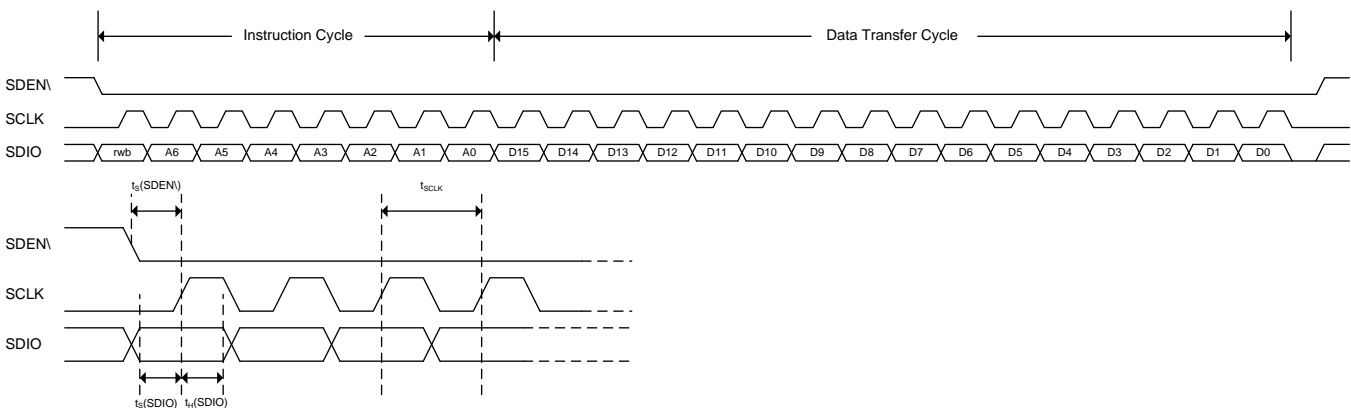
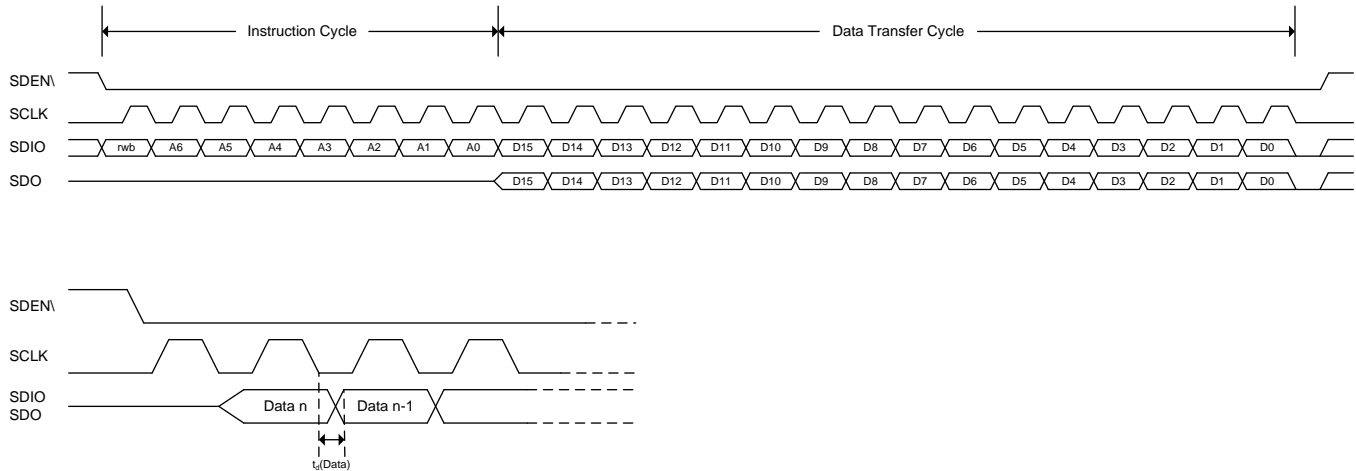


Figure 50. Serial Interface Write Timing Diagram

Figure 51 shows the serial interface timing diagram for a DAC38RFxx read operation. SCLK is the serial interface clock input to DAC38RFxx. Serial data enable SDEN is an active low input to DAC38RFxx. SDIO is serial data input during the instruction cycle. In 3 pin configuration, SDIO is data out from the DAC38RFxx during the data transfer cycle, while SDO is in a high-impedance state. In 4 pin configuration, both SDIO and SDO are data out from the DAC38RFxx during the data transfer cycle. At the end of the data transfer, SDIO and SDO will output low on the final falling edge of SCLK until the rising edge of SDEN when they will 3-state.



**Figure 51. Serial Interface Read Timing Diagram**

In the SIF interface there are four types of registers:

#### 8.4.5.1 NORMAL (RW)

The NORMAL register type allows data to be written and read from. All 16-bits of the data are registered at the same time. There is no synchronizing with an internal clock thus all register writes are asynchronous with respect to internal clocks. There are three subtypes of NORMAL:

1. AUTOSYNC: A NORMAL register that causes a sync to be generated after the write is finished. These are used when it is desirable to synchronize the block after writing the register or for a single field that spans across multiple registers. For instance, the NCO requires three 16-bit register writes to set the frequency. Upon writing the last of these registers an autosync is generated to deliver the entire field to the NCO block at once, rather than in pieces after each individual register write. For a field that spans multiple registers, all non-AUTOSYNC registers for the field must be written first before the actual AUTOSYNC register.
2. No RESET Value: These are NORMAL registers, but the reset value cannot be specified. This could be because the register has some read\_only bits or some internal logic partially controls the bit values.
3. READ\_ONLY (R): Registers that can only be read.

#### 8.4.5.2 WRITE\_TO\_CLEAR (W0C)

These registers are just like NORMAL registers with one exception. They can be written and read, however, when the internal logic asynchronously sets a bit high in one of these registers, that bit stays high until it is written to '0'. This way interrupts will be captured and stay constant until cleared by the user.

### 8.5 Register Maps

**Table 41. Register Summary**

Address	Reset	Acronym	Register Name	Section
<b>General Configuration Registers (PAGE_SET[2:0] = 000)</b>				
0x00	0x5803	RESET_CONFIG	Chip Reset and Configuration	<a href="#">8.5.1</a>
0x01	0x1800	IO_CONFIG	IO Configuration	<a href="#">8.5.2</a>
0x02	0xFFFF	ALM_SD_MASK	Lane Signal Detect Alarm Mask	<a href="#">8.5.3</a>
0x03	0xFFFF	ALM_CLK_MASK	Clock Alarms Mask	<a href="#">8.5.4</a>
0x04	0x0000	ALM_SD_DET	SERDES Loss of Signal Detection Alarms	<a href="#">8.5.5</a>
0x05	0x0000	ALM_SYSREF_DET	SYSREF Alignment Circuit Alarms	<a href="#">8.5.6</a>
0x06	variable	TEMP_PLLVOLT	Temperature Sensor and PLL Loop Voltage	<a href="#">8.5.7</a>
0x07-0x08	0x0000	Reserved	Reserved	
0x09	0x0000	PAGE_SET	Page Set	<a href="#">8.5.8</a>

**Register Maps (continued)**
**Table 41. Register Summary (continued)**

Address	Reset	Acronym	Register Name	Section
0x0A-0x77	0x0000	Reserved	Reserved	
0x78	0x0000	SYSREF_ALIGN_R	SYSREF Align to r1 and r3 Count	<a href="#">8.5.9</a>
0x79	0x0000	SYSREF12_CNT	SYSREF Phase Count 1 and 2	<a href="#">8.5.10</a>
0x7A	0x0000	SYSREF34_CNT	SYSREF Phase Count 3 and 4	<a href="#">8.5.11</a>
0x7B-0x7E	0x0000	Reserved	Reserved	
0x7F	0x0008	VENDOR_VER	Vendor ID and Chip Version	<a href="#">8.5.12</a>
<b>Multi-DUC Configuration Registers (PAGE_SET[0] = 1 for multi-DUC1, PAGE_SET[1] = 1 for multi-DUC2)</b>				
0x0A	0x02B0	MULTIDUC_CFG1	Multi-DUC Configuration (PAP, Interpolation)	<a href="#">8.5.13</a>
0x0B	0x0000	Reserved	Reserved	
0x0C	0x2402	MULTIDUC_CFG2	Multi-DUC Configuration (Mixers)	<a href="#">8.5.14</a>
0x0D	0x8300	JESD_FIFO	JESD FIFO Control	<a href="#">8.5.15</a>
0x0E	0x00FF	ALM_MASK1	Alarm Mask 1	<a href="#">8.5.16</a>
0x0F	0x1F83	ALM_MASK2	Alarm Mask 2	<a href="#">8.5.17</a>
0x10	0xFFFF	ALM_MASK3	Alarm Mask 3	<a href="#">8.5.18</a>
0x11	0xFFFF	ALM_MASK4	Alarm Mask 4	<a href="#">8.5.19</a>
0x12	0x0000	JESD_LN_SKEW	JESD Lane Skew	<a href="#">8.5.20</a>
0x13-0x16	0x0000	Reserved	Reserved	
0x17	0x0000	CMIX	CMIX Configuration	<a href="#">8.5.21</a>
0x18	0x0000	Reserved	Reserved	
0x19	0x0000	OUTSUM	Output Summation and Delay	<a href="#">8.5.22</a>
0x1A-0x1B	0x0000	Reserved	Reserved	
0x1C	0x0000	PHASE_NCOAB	Phase offset for AB path NCO	<a href="#">8.5.23</a>
0x1D	0x0000	PHASE_NCOCD	Phase offset for CD path NCO	<a href="#">8.5.24</a>
0x1E-0x20	0x0000	FREQ_NCOAB	Frequency for AB path NCO	<a href="#">8.5.25</a>
0x21-0x23	0x0000	FREQ_NCOCD	Frequency for CD path NCO	<a href="#">8.5.26</a>
0x24	0x0010	SYSREF_CLKDIV	SYSREF Use for Clock Divider	<a href="#">8.5.27</a>
0x25	0x7700	SERDES_CLK	Serdes Clock Control	<a href="#">8.5.28</a>
0x26	0x0000	Reserved	Reserved	
0x27	0x1144	SYNCSEL1	Sync Source Selection	<a href="#">8.5.29</a>
0x28	0x0000	SYNCSEL2	Sync Source Selection	<a href="#">8.5.30</a>
0x29	0x0000	PAP_GAIN_AB	PAP path AB Gain Attenuation Step	<a href="#">8.5.31</a>
0x2A	0x0000	PAP_WAIT_AB	PAP path AB Wait Time at Gain = 0	<a href="#">8.5.32</a>
0x2B	0x0000	PAP_GAIN_CD	PAP path CD Gain Attenuation Step	<a href="#">8.5.33</a>
0x2C	0x0000	PAP_WAIT_CD	PAP path CD Wait Time at Gain = 0	<a href="#">8.5.34</a>
0x2D	0x1FFF	PAP_CFG_AB	PAP path AB Configuration	<a href="#">8.5.35</a>
0x2E	0x1FFF	PAP_CFG_CD	PAP path CD Configuration	<a href="#">8.5.36</a>
0x2F	0x0000	SPIDAC_TEST1	Configuration for DAC SPI Constant	<a href="#">8.5.37</a>
0x30	0x0000	SPIDAC_TEST2	DAC SPI Constant	<a href="#">8.5.38</a>
0x31	0x0000	Reserved	Reserved	
0x32	0x0800	GAINAB	Gain for path AB	<a href="#">8.5.39</a>
0x33	0x0800	GAINCD	Gain for path CD	<a href="#">8.5.40</a>
0x34-0x40	0x0000	Reserved	Reserved	
0x41	0x0000	JESD_ERR_CNT	JESD Error Counter	<a href="#">8.5.41</a>
0x42-0x45	0x0000	Reserved	Reserved	
0x46	0x0044	JESD_ID1	JESD ID 1	<a href="#">8.5.42</a>
0x47	0x190A	JESD_ID2	JESD ID 2	<a href="#">8.5.43</a>
0x48	0x31C3	JESD_ID3	JESD ID 3 and Subclass	<a href="#">8.5.44</a>
0x49	0x0000	Reserved	Reserved	
0x4A	0x0003	JESD_LN_EN	JESD Lane Enable	<a href="#">8.5.45</a>
0x4B	0x1300	JESD_RBD_F	JESD RBD Buffer and Frame Octets	<a href="#">8.5.46</a>

Register Maps (continued)

Table 41. Register Summary (continued)

Address	Reset	Acronym	Register Name	Section
0x4C	0x1303	JESD_K_L	JESD K and L Parameters	<a href="#">8.5.47</a>
0x4D	0x0100	JESD_M_S	JESD M and S Parameters	<a href="#">8.5.48</a>
0x4E	0x0F4F	JESD_N_HD_SCR	JESD N, HD and SCR Parameters	<a href="#">8.5.49</a>
0x4F	0x1CC1	JESD_MATCH	JESD Character Match and Other	<a href="#">8.5.50</a>
0x50	0x0000	JESD_LINK_CFG	JESD Link Configuration Data	<a href="#">8.5.51</a>
0x51	0x00FF	JESD_SYNC_REQ	JESD Sync Request	<a href="#">8.5.52</a>
0x52	0x00FF	JESD_ERR_OUT	JESD Error Output	<a href="#">8.5.53</a>
0x53	0x0100	JESD_ILA_CFG1	JESD Configuration Value used for ILA Check	<a href="#">8.5.54</a>
0x54	0x8E60	JESD_ILA_CFG2	JESD Configuration Value used for ILA Check	<a href="#">8.5.55</a>
0x55-0x5B	0x0000	Reserved	Reserved	
0x5C	0x0001	JESD_SYSR_MODE	JESD SYSREF Mode	<a href="#">8.5.56</a>
0x5D-0x5E	0x0000	Reserved	Reserved	
0x5F	0x0123	JESD_CROSSBAR1	JESD Crossbar Configuration 1	<a href="#">8.5.57</a>
0x60	0x4567	JESD_CROSSBAR2	JESD Crossbar Configuration 2	<a href="#">8.5.58</a>
0x61-0x63	0x0000	Reserved	Reserved	
0x64	0x0000	JESD_ALM_L0	JESD Alarms for Lane 0	<a href="#">8.5.59</a>
0x65	0x0000	JESD_ALM_L1	JESD Alarms for Lane 1	<a href="#">8.5.60</a>
0x66	0x0000	JESD_ALM_L2	JESD Alarms for Lane 2	<a href="#">8.5.61</a>
0x67	0x0000	JESD_ALM_L3	JESD Alarms for Lane 3	<a href="#">8.5.62</a>
0x68	0x0000	JESD_ALM_L4	JESD Alarms for Lane 4	<a href="#">8.5.63</a>
0x69	0x0000	JESD_ALM_L5	JESD Alarms for Lane 5	<a href="#">8.5.64</a>
0x6A	0x0000	JESD_ALM_L6	JESD Alarms for Lane 6	<a href="#">8.5.65</a>
0x6B	0x0000	JESD_ALM_L7	JESD Alarms for Lane 7	<a href="#">8.5.66</a>
0x6C	0x0000	ALM_SYSREF_PAP	SYSREF and PAP Alarms	<a href="#">8.5.67</a>
0x6D	0x0000	ALM_CLKDIV1	Clock Divider Alarms 1	<a href="#">8.5.68</a>
0x6E-0x77	0x0000	Reserved	Reserved	
<b>Miscellaneous Configuration Registers (PAGE_SET[1:0] = 00, PAGE_SET[2] = 1)</b>				
0x0A	0xFC03	CLK_CONFIG	Clock Configuration	<a href="#">8.5.69</a>
0x0B	0x0022	SLEEP_CONFIG	Sleep Configuration	<a href="#">8.5.70</a>
0x0C	0xA002	CLK_OUT	Divided Output Clock Configuration	<a href="#">8.5.71</a>
0x0D	0xF000	DACFS	DAC Fullscale Current	<a href="#">8.5.72</a>
0x0E-0x0F	0x0000	Reserved	Reserved	
0x10	0x0000	LCMGEN	Internal sysref generator	<a href="#">8.5.73</a>
0x11	0x0000	LCMGEN_DIV	Counter for internal sysref generator	<a href="#">8.5.74</a>
0x12	0x0000	LCMGEN_SPISYSREF	SPI SYSREF for internal sysref generator	<a href="#">8.5.75</a>
0x13-0x1A	0x0000	Reserved	Reserved	
0x1B	0x0000	DTEST	Digital Test Signals	<a href="#">8.5.76</a>
0x1C-0x22	0x0000	Reserved	Reserved	
0x23	0x03F3	SLEEP_CNTL	Sleep Pin Control	<a href="#">8.5.77</a>
0x24	0x1000	SYSR_CAPTURE	SYSREF Capture Circuit Control	<a href="#">8.5.78</a>
0x25-0x30	0x0000	Reserved	Reserved	
0x31	0x0200	CLK_PLL_CFG	Clock Input and PLL Configuration	<a href="#">8.5.79</a>
0x32	0x0308	PLL_CONFIG1	PLL Configuration 1	<a href="#">8.5.80</a>
0x33	0x4018	PLL_CONFIG2	PLL Configuration 2	<a href="#">8.5.81</a>
0x34	0x0000	LVDS_CONFIG	LVDS Output Configuration	<a href="#">8.5.82</a>
0x35	0x0018	PLL_FDIV	Fuse farm clock divider	<a href="#">8.5.83</a>
0x36-0x3A	0x0000	Reserved	Reserved	
0x3B	0x0002	SRDS_CLK_CFG	Serdes Clock Configuration	<a href="#">8.5.84</a>



**Register Maps (continued)**
**Table 41. Register Summary (continued)**

Address	Reset	Acronym	Register Name	Section
0x3C	0x8228	SRDS_PLL_CFG	Serdes PLL Configuration	<a href="#">8.5.85</a>
0x3D	0x0088	SRDS_CFG1	Serdes Configuration 1	<a href="#">8.5.86</a>
0x3E	0x0909	SRDS_CFG2	Serdes Configuration 2	<a href="#">8.5.87</a>
0x3F	0x0000	SRDS_POL	Serdes Polarity Control	<a href="#">8.5.88</a>
0x40-0x75	0x0000	Reserved	Reserved	
0x76	0x0000	SYNCBOUT	JESD204B SYNCB Output	<a href="#">8.5.89</a>

### 8.5.1 Chip Reset and Configuration Register (address = 0x00) [reset = 0x5803]

Figure 52. Chip Reset and Configuration Register (RESET\_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
RW	RW	RW	RW	RW	RW	RW	RW
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. RESET\_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_RESET	RW	0	This will reset all the SPI registers once programmed.
14	ALM_OUT_POL	RW	1	Changes the polarity of the alarm output. 0= active low 1= active high
13	ALM_OUT_ENA	RW	0	Turn on the alarm pin
12	SYSCLK_ENA	RW	1	Turns on the dividers for the SYSCLK to the Fusefarm
11	AUTOLOAD_TRIG	RW	1	Causes a Fuse AUTOLOAD to be executed.
10:7	Reserved	RW	0000	Reserved
6	ONE_DAC_ONLY	RW	0	When set high only the SLICE0 is available.
5	ONE_LINK_ONLY	RW	0	This needs to be set high when a single link setup is being programmed to get the correct TXENABLE signal generation
4:2	Reserved	RW	000	Reserved
1	INIT_SLICE1	RW	1	Puts the multi-DAC2 JESD into initialization state
0	INIT_SLICE0	RW	1	Puts the multi-DAC1 JESD into initialization state

**8.5.2 IO Configuration Register (address = 0x01) [reset = 0x1800]**
**Figure 53. IO Configuration Register (IO\_CONFIG)**

15	14	13	12	11	10	9	8
0	0	0	1	1	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 43. IO\_CONFIG Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPO0_SEL	RW	00	Selects the JESD SYNC_N signal coming out the GPO0 pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
13:12	SYNC0B_SEL	RW	01	Selects the JESD SYNC_N signal coming out the SYNC0B pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
11:10	SYNC1B_SEL	RW	10	Selects the JESD SYNC_N signal coming out the SYNC1B pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
9:8	GPO1_SEL	RW	00	Selects the JESD SYNC_N signal coming out the GPO1 pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
7	SPI4_ENA	RW	0	When set to a '1' the chip is in 4 pin SPI interface mode.
6	Reserved	RW	0	Reserved
5:0	ATEST	RW	000000	Select the analog test points: 000000: ATEST is off (ATEST Must be off during normal operation) 000001, 010001, 000110: VSSCLK 000010: VDDPLL1 000101: VDDCLK 000111, 001010, 010000: VDDAPLL18 001011: VDDAVCO18 001101: VDDS18 001110: VDDE1 001111, 111010, 111011, 111100: DGND 010011: VDDTX1 101001, 110001: AGND 101111, 111101, 111110, 111111: VDDDIG1 110000: VDDA18

### 8.5.3 Lane Single Detect Alarm Mask Register (address = 0x02) [reset = 0xFFFF]

Figure 54. Lane Single Detect Alarm Mask Register (ALM\_SD\_MASK)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. ALM\_SD\_MASK Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_SD_MASK	R/W	0xFFFF	Used to mask alarms bit 15 - bit 8 : Reserved bit7 : lane 7 loss of signal detect bit6 : lane 6 loss of signal detect bit5 : lane 5 loss of signal detect bit4 : lane 4 loss of signal detect bit3 : lane 3 loss of signal detect bit2 : lane 2 loss of signal detect bit1 : lane1 loss of signal detect bit0 : lane 0 loss of signal detect

### 8.5.4 Clock Alarms Mask Register (address = 0x03) [reset = 0xFFFF]

Figure 55. Clock Alarms Mask Register (ALM\_CLK\_MASK)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. ALM\_CLK\_MASK Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_CLK_MASK	R/W	0xFFFF	Used to mask alarms bit 15 - bit 8 : Reserved bit 7 : alarm_sysrefphase4 bit 6 : alarm_sysrefphase3 bit 5 : alarm_sysrefphase2 bit 4 : alarm_sysrefphase1 bit 3 : alarm_align_to_r3 bit 2 : alarm_align_to_r1 bit 1 : alarm_sd0_pll bit 0 : alarm_sd1_pll

**8.5.5 SERDES Loss of Signal Detection Alarms Register (address = 0x04) [reset = 0x0000]**
**Figure 56. SERDES Loss of Signal Detection Alarms Register (ALM\_SD\_DET)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset

**Table 46. ALM\_SD\_DET Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	Reserved	W0C	0x00	Reserved
7:0	ALM_SD_LOSDET	W0C	0x00	Loss of signal detect outputs from the SERDES lanes: bit 7 = lane7 loss of signal bit 6 = lane6 loss of signal bit 5 = lane5 loss of signal bit 4 = lane4 loss of signal bit 3 = lane3 loss of signal bit 2 = lane2 loss of signal bit 1 = lane1 loss of signal bit 0 = lane0 loss of signal

**8.5.6 SYSREF Alignment Circuit Alarms Register (address = 0x05) [reset = 0x0000]**

**Figure 57. SYSREF Alignment Circuit Alarms Register (ALM\_SYSREF\_DET)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset

**Table 47. ALM\_SYSREF\_DET Field Descriptions**

Bit	Field	Type	Reset	Description
15:9	Reserved	W0C	0000000	Reserved
8	ALM_SYSRPHASE4	W0C	0	If high the sysrefphase4 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
7	ALM_SYSRPHASE3	W0C	0	If high the sysrefphase3 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
6	ALM_SYSRPHASE2	W0C	0	If high the sysrefphase2 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
5	ALM_SYSRPHASE1	W0C	0	If high the sysrefphase1 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
4	ALM_ALIGN_TO_R3	W0C	0	If high the align_to_r3 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync. TI Internal use only.
3	ALM_ALIGN_TO_R1	W0C	0	If high the align_to_r1 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync. TI Internal use only.
2	ALM_SD0_PLL	W0C	0	Driven high if the PLL in the Serdes 0 block goes out of lock. A false alarm is generated at startup when the PLL is locking. User will have to reset this bit after start to monitor accurately.
1	ALM_SD1_PLL	W0C	0	Driven high if the PLL in the Serdes 1 block goes out of lock. A false alarm is generated at startup when the PLL is locking. User will have to reset this bit after start to monitor accurately.
0	PLL_LOCK	W0C	0	Asserted when PLL is unlocked.

### 8.5.7 Temperature Sensor and PLL Loop Voltage Register (address = 0x06) [reset = variable]

**Figure 58. Temperature Sensor and PLL Loop Voltage Register (TEMP\_PLLVOLT)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 48. TEMP\_PLLVOLT Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	TEMPDATA	R	0x00	8 bits of data from the temperature sensor
7:5	PLL_LFVOLT	R	0b000	PLL Loop filter voltage
4:2	Reserved	R	0b000	Reserved
1	TITEST_VOH	R	1	A fixed '1' that can be used to test the VOH condition on SDO/SDIO.
0	TITEST_VOL	R	0	A fixed '0' that can be used to test the VOL condition on SDO/SDIO.

### 8.5.8 Page Set Register (address = 0x09) [reset = 0x0000]

**Figure 59. Page Set Register (PAGE\_SET)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 49. PAGE\_SET Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	PAGE_SET	R/W	0x0000	Each bit selects a page that is active. Multiple pages can be selected at the same time. No bits asserted means that MASTER is the only page selected. bit 0 = page0 : multi-DUC1 bit 1 = page1 : multi-DUC2 bit 2 = page2 : DIG_MISC bit 3-15: Reserved

### 8.5.9 SYSREF Align to r1 and r3 Count Register (address = 0x78) [reset = 0x0000]

Figure 60. SYSREF Align to r1 and r3 Count Register (SYSREF\_ALIGN\_R)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. SYSREF\_ALIGN\_R Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALIGN_TO_R1_CNT	R	0x00	Part of the SYSREF Align block
7:0	ALIGN_TO_R3_CNT	R	0x00	Part of the SYSREF Align block

### 8.5.10 SYSREF Phase Count 1 and 2 Register (address = 0x79) [reset = 0x0000]

Figure 61. SYSREF Phase Count 1 and 2 Register (SYSREF12\_CNT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. SYSREF12\_CNT Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE2_CNT	R	0x00	Part of the SYSREF Align block
7:0	PHASE1_CNT	R	0x00	Part of the SYSREF Align block



### 8.5.11 SYSREF Phase Count 3 and 4 Register (address = 0x7A) [reset = 0x0000]

**Figure 62. SYSREF Phase Count 3 and 4 Register (SYSREF34\_CNT)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 52. SYSREF34\_CNT Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	PHASE4_CNT	R	0x00	Part of the SYSREF Align block
7:0	PHASE3_CNT	R	0x00	Part of the SYSREF Align block

### 8.5.12 Vendor ID and Chip Version Register (address = 0x7F) [reset = 0x0008]

**Figure 63. Vendor ID and Chip Version Register (VENDOR\_VER)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 53. VENDOR\_VER Field Descriptions**

Bit	Field	Type	Reset	Description
15	AUTOLOAD_DONE	R	0	Asserted when the Fusefarm Autoload sequence is done
14:10	EFC_ERR	R	00000	The error output from the fuse farm.
9:5	Reserved	R	00000	Reserved
4:3	VENDORID	R	01	TI identification
2:0	VERSION	R	001	Bits to determine what version of build for the chip.

### 8.5.13 Multi-DUC Configuration (PAP, Interpolation) Register (address = 0x0A) [reset = 0x02B0]

Figure 64. Multi-DUC Configuration (PAP, Interpolation) Register (MULTIDUC\_CFG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. MULTIDUC\_CFG1 Field Descriptions

Bit	Field	Type	Reset	Description
15	DUAL_IQ	R/W	0	When asserted the SLICE uses both IQ paths
14	ISFIR_ENA	R/W	0	Turns on the inverse sync filter for the AB and CD paths when programmed to 1.
13	Not used	R/W	0	Not used
12:8	INTERP	R/W	00010	Determines the interpolation amount. 00000: 1x 00001: 2x 00010: 4x 00011: 6x 00100: 8x 00101: 10x 00110: 12x 01000: 16x 01001: 18x 01010: 20x 01100: 24x
7	ALM_ZEROS_TXEN	R/W	1	When asserted any alarm that isn't masked will mid-level the DAC output by setting the txenable_from_dig to '0'
6	DAC_COMPLEMENT	R/W	0	When asserted the DAC output will be 2's complemented. This helps with hookup at the board level.
5	ALM_ZEROS_JESD	R/W	1	When asserted any alarm that isn't masked will zero the data coming out of the JESD block.
4	ALM_OUT_ENA	R/W	1	When asserted the output from the selected SLICE will be passed on to the MASTER alarm control if it is also turned on then the alarm will be sent to the pad_alarm pin.
3	PAPA_ENA	R/W	0	Turns on the Power Amp Protection logic for path A.
2	PAPB_ENA	R/W	0	Turns on the Power Amp Protection logic for path B.
1	PAPC_ENA	R/W	0	Turns on the Power Amp Protection logic for path C.
0	PAPD_ENA	R/W	0	Turns on the Power Amp Protection logic for path D.

**8.5.14 Multi-DUC Configuration (Mixers) Register (address = 0x0C) [reset = 0x2402]**
**Figure 65. Multi-DUC Configuration (Mixers) Register (MULTIDUC\_CFG2)**

15	14	13	12	11	10	9	8
0	0	0	0	0	1	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 55. MULTIDUC\_CFG2 Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	DAC_BITWIDTH	R/W	0b00	Determines the bit width of the data going to the DAC 00: 14 bits 01: 14 bits 10: 12 bits 11: 11 bits
13	ZERO_INVLD_DATA	R/W	1	When asserted; the data from the JESD block is zeroed in the mapper to prevent goofy output from the DAC. For test purposes this bit should be desasserted
12	SHORTTEST_ENA	R/W	0	Turns on the JESD SHORT pattern test (5.1.6.2)
11	BIST_ENA	R/W	0	Turns on the BIST blocks in the SLICE.
10	BIST_ZERO	R/W	1	Zeros out the bists captures.
9	MIXERAB_ENA	R/W	0	Turns on the mixer for the A and B streams
8	MIXERCD_ENA	R/W	0	Turns on the mixer for the C and D streams
7	MIXERAB_GAIN	R/W	0	Adds 6dB of gain when asserted
6	MIXERCD_GAIN	R/W	0	Adds 6dB of gain when asserted
5	NCOAB_ENA	R/W	0	When high the full NCO block is turned on.
4	NCOCD_ENA	R/W	0	When high the full NCO block is turned on.
3:2	Reserved	R/W	00	Reserved
1	TWOS	R/W	1	When asserted the chip is expecting 2's complement data is arriving through the JESD; otherwise offset binary is expected
0	Reserved	R/W	0	Reserved

### 8.5.15 JESD FIFO Control Register (address = 0x0D) [reset = 0x1300]

Figure 66. JESD FIFO Control Register (JESD\_FIFO)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. JESD\_FIFO Field Descriptions

Bit	Field	Type	Reset	Description
15	FIFO_ZEROS_DATA	R/W	1	When asserted FIFO errors zero the data out of the JESD block. For test purposes this could be turned off to allow test patterns in the FIFO.
14:13	NOT USED	R/W	000	Not Used
12	SRDS_FIFO_ALM_CLR	R/W	0	Set to 1 to clear FIFO errors. Must be set to 0 for proper FIFO operation
11	Not used	R/W	0	Not used
10:8	FIFO_OFFSET	R/W	0000	Used to set the difference between read and write pointers in the JESD FIFO.
7:1	Reserved	R/W	0	Reserved
0	SPI_TXENABLE	R/W	0	When asserted the internal value of txenable = '1'

### 8.5.16 Alarm Mask 1 Register (address = 0x0E) [reset = 0x00FF]

Figure 67. Alarm Mask 1 Register (ALM\_MASK1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. ALM\_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_MASK1	R/W	0x00FF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask lane7 lane errors bit 14 = mask lane6 lane errors bit 13 = mask lane5 lane errors bit 12 = mask lane4 lane errors bit 11 = mask lane3 lane errors bit 10 = mask lane2 lane errors bit 9 = mask lane1 lane errors bit 8 = mask lane0 lane errors bit 7 = mask lane7 FIFO flags bit 6 = mask lane6 FIFO flags bit 5 = mask lane5 FIFO flags bit 4 = mask lane4 FIFO flags bit 3 = mask lane3 FIFO flags bit 2 = mask lane2 FIFO flags bit 1 = mask lane1 FIFO flags bit 0 = mask lane0 FIFO flags

**8.5.17 Alarm Mask 2 Register (address = 0x0F) [reset = 0xFFFF]**
**Figure 68. Alarm Mask 2 Register (ALM\_MASK2)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 58. ALM\_MASK2 Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK2	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = not used bit 14 = not used bit 13 = not used bit 12 = mask SYSREF errors on link0 bit 11 = mask alarm from JESD shorttest bit 10 = mask alarm from PAPD bit 9 = mask alarm from PAPC bit 8 = mask alarm from PAPB bit 7 = mask alarm from PAPA bit 6 = not used bit 5 = not used bit 4 = not used bit 3 = not used bit 2 = not used bit 1 = mask alarm_clkdiv192_eq_zero bit 0 = mask alarm_clkdiv192_eq_mult1

**8.5.18 Alarm Mask 3 Register (address = 0x10) [reset = 0xFFFF]**

**Figure 69. Alarm Mask 3 Register (ALM\_MASK3)**

15	14	13	12	11	10	9	8
	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 59. ALM\_MASK3 Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK3	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask alarm_clkdiv8_eq_zero bit 14 = mask alarm_clkdiv12_eq_zero bit 13 = mask alarm_clkdiv16_eq_zero bit 12 = mask alarm_clkdiv18_eq_zero bit 11 = mask alarm_clkdiv20_eq_zero bit 10 = mask alarm_clkdiv32_eq_zero bit 9 = mask alarm_clkdiv36_eq_zero bit 8 = mask alarm_clkdiv40_eq_zero bit 7 = mask alarm_clkdiv48_eq_zero bit 6 = mask alarm_clkdiv64_eq_zero bit 5 = mask alarm_clkdiv72_eq_zero bit 4 = mask alarm_clkdiv80_eq_zero bit 3 = mask alarm_clkdiv96_eq_zero bit 2 = mask alarm_clkdiv128_eq_zero bit 1 = mask alarm_clkdiv144_eq_zero bit 0 = mask alarm_clkdiv160_eq_zero

**8.5.19 Alarm Mask 4 Register (address = 0x11) [reset = 0xFFFF]**
**Figure 70. Alarm Mask 4 Register (ALM\_MASK4)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 60. ALM\_MASK4 Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK4	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask alarm_clkdiv8_eq_mult1 bit 14 = mask alarm_clkdiv12_eq_mult1 bit 13 = mask alarm_clkdiv16_eq_mult1 bit 12 = mask alarm_clkdiv18_eq_mult1 bit 11 = mask alarm_clkdiv20_eq_mult1 bit 10 = mask alarm_clkdiv32_eq_mult1 bit 9 = mask alarm_clkdiv36_eq_mult1 bit 8 = mask alarm_clkdiv40_eq_mult1 bit 7 = mask alarm_clkdiv48_eq_mult1 bit 6 = mask alarm_clkdiv64_eq_mult1 bit 5 = mask alarm_clkdiv72_eq_mult1 bit 4 = mask alarm_clkdiv80_eq_mult1 bit 3 = mask alarm_clkdiv96_eq_mult1 bit 2 = mask alarm_clkdiv128_eq_mult1 bit 1 = mask alarm_clkdiv144_eq_mult1 bit 0 = mask alarm_clkdiv160_eq_mult1

### 8.5.20 JESD Lane Skew Register (address = 0x12) [reset = 0x0000]

Figure 71. JESD Lane Skew Register (JESD\_LN\_SKEW)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. JESD\_LN\_SKEW Field Descriptions

Bit	Field	Type	Reset	Description
15:5	NOT USED	R	0x0000	Not used
4:0	MEMIN_LANE_SKEW	R	0b00000	Measure of the lane skew for each link only. Bits are READ_ONLY

### 8.5.21 CMIX Configuration Register (address = 0x17) [reset = 0x0000]

Figure 72. CMIX Configuration Register (CMIX)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. CMIX Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CMIX_AB	R/W	0x0	These bits turn on the different coarse mixing options. Combining the different options together can result in every possible $n \times Fs/8$ [ $n=0->7$ ]. Below is the valid programming table: cmix=(mem_fs8; mem_fs4; mem_fs2; mem_fsm4) 0000 : no mixing 0001 : -fs/4 0010 : fs/2 0100 : fs/4 1000 : fs/8 1100 : 3fs/8 1010 : 5fs/8 1110 : 7fs/8
11:4	Reserved	R/W	00000000 0	Reserved
3:0	CMIX_CD	R/W	0x0	These bits turn on the different coarse mixing options. Combining the different options together can result in every possible $n \times Fs/8$ [ $n=0->7$ ]. Below is the valid programming table: cmix=(mem_fs8; mem_fs4; mem_fs2; mem_fsm4) 0000 : no mixing 0001 : -fs/4 0010 : fs/2 0100 : fs/4 1000 : fs/8 1100 : 3fs/8 1010 : 5fs/8 1110 : 7fs/8



### 8.5.22 Output Summation and Delay Register (address = 0x19) [reset = 0x0000]

**Figure 73. Output Summation and Delay Register (OUTSUM)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 63. OUTSUM Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	OUTPUT_DELAY	R/W	0x0	Delays the output to the DAC 0 to 15 clock cycles
11:4	Reserved	R/W	0x00	Reserved
3:0	OUTSUM_SEL	R/W	0x0	Selects the output summing functions. Each bit selects another sample to sum. Multiple bits can be selected. bit 0 = add the isfirab bit 1 = add the isfircb bit 2 = add adjacent slice AB sample bit 3 = add adjacent slice CD sample

### 8.5.23 NCO Phase Path AB Register (address = 0x1C) [reset = 0x0000]

**Figure 74. NCO Phase Path AB Register (PHASE\_NCOAB)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 64. PHASE\_NCOAB Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	PHASE_NCO1	Auto Sync	0x0000	The phase offset for the FULL NCO1 in the AB datapath.

### 8.5.24 NCO Phase Path CD Register (address = 0x1D) [reset = 0x0000]

**Figure 75. NCO Phase Path CD Register (PHASE\_NCOCD)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 65. PHASE\_NCOCD Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	PHASE_NCO12	Auto Sync	0x0000	The phase offset for the FULL NCO2 in the CD datapath.

**8.5.25 NCO Frequency Path AB Register (address = 0x1E-0x20) [reset = 0x0000 0000 0000]**

**Figure 76. NCO Frequency Path AB Register (FREQ\_NCOAB)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 66. FREQ\_NCOAB Field Descriptions**

Bit	Field	Type	Reset	Description
47:0	FREQ_NCOAB	R/W	0x0000 0000 0000	NCO frequency word for AB data path.

**8.5.26 NCO Frequency Path CD Register (address = 0x21-0x23) [reset = 0x0000 0000 0000]**

**Figure 77. NCO Frequency Path CD Register (FREQ\_NCOCD)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 67. FREQ\_NCOCD Field Descriptions**

Bit	Field	Type	Reset	Description
47:0	FREQ_NCOCD	R/W	0x0000 0000 0000	NCO frequency word for CD data path.

**8.5.27 SYSREF Use for Clock Divider Register (address = 0x24) [reset = 0x0010]**
**Figure 78. SYSREF Use for Clock Divder Register (SYSREF\_CLKDIV)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 68. SYSREF\_CLKDIV Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	CDRVSER_SYSREF_DLY	R/W	000	Programmable delay the SYSREF by N dacclk cycles to the CDRV_SER clock dividers. By offsetting the clock to the different multi-DUC blocks, clock mixing could potentially be reduced.
11:7	Not used	R/W	00000	Not used
6:4	SYSREF_MODE	R/W	001	Determines how SYSREF is used to sync the clock dividers in the CDRV_SER block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses.
3:2	SYSREF_DLY	R/W	00	Delays the SYSREF into the CDRV_SER capture FF through 1 of 4 choices. This allows for extra delay in case the timing of the clock or SYSREF path isn't as good as we think.
1:0	Reserved	R/W	00	Reserved

**8.5.28 Serdes Clock Control Register (address = 0x25) [reset = 0x7700]**

**Figure 79. Serdes Clock Control Register (SERDES\_CLK)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 69. SERDES\_CLK Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	CLKJESD_DIV	R/W	0x7	This controls the selection of the clk_jesd output 0000 = div4 0001 = div8 0010 = div12 0011 = div16 0100 = div18 0101 = div20 0110 = div24 0111 = div32 1001 = div36 1010 = div48 1011 = div64 1100 = div5.333 1101 = div10.666 1110 = div21p333
11:8	CLKJESD_OUT_DIV	R/W	0x7	This controls the selection of the clk_jesd_out output 0000 = div8 0001 = div16 0010 = div32 0011 = div48 0100 = div64 0101 = div80 0110 = div96 0111 = div128 1000 = div144 1001 = div160 1010 = div192
7:0	Reserved	R/W	0x0	Reserved

**8.5.29 Sync Source Control 1 Register (address = 0x27) [reset = 0x1144]**
**Figure 80. Sync Source Control 1 Register (SYNCSEL1)**

15		14		13		12		11		10		9		8	
0		0		0		0		0		0		0		x	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
7		6		5		4		3		2		1		0	
0		0		1		0		0		1		1		1	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 70. SYNCSEL1 Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	SYNCSEL_MIXERAB	R/W	0x1	Controls the syncing of the double buffered SPI registers for the mixerAB block. These bits are enables so a '1' in the bit place allows the sync to pass to the block. bit 0 = auto-sync from SPI register write bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
11:8	SYNCSEL_MIXERCD	R/W	0x1	Controls the syncing of the double buffered SPI registers for the mixerCD block. These bits are enables so a '1' in the bit place allows the sync to pass to the block. bit 0 = auto-sync from SPI register write bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
7:4	SYNCSEL_NCOAB	R/W	0x4	Controls the syncing of NCOAB accumulators. These bits are enables so a '1' in the bit place allows the sync to pass to the block. bit 0 = '0' bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
3:0	SYNCSEL_NCOCD	R/W	0x4	Controls the syncing of NCOCD accumulators. These bits are enables so a '1' in the bit place allows the sync to pass to the block. bit 0 = '0' bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync

### 8.5.30 Sync Source Control 2 Register (address = 0x28) [reset = 0x0000]

Figure 81. Sync Source Control 2 Register (SYNCSEL2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. SYNCSEL2 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Reserved	R/W	0x0	Reserved
11:8	SYNCSEL_PAPAB	R/W	0x0	Select the sync for the PAP A and B. bit 0 = '0' bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
7:4	SYNCSEL_PAPCD	R/W	0x0	Select the sync for the PAP C and D. bit 0 = '0' bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
3:2	Reserved	R/W	0b00	Reserved
1	SPI_SYNC	R/W	0	This is used to generate the SPI_SYNC signal
0	Reserved	R/W	0	Reserved

### 8.5.31 PAP path AB Gain Attenuation Step Register (address = 0x29) [reset = 0x0000]

Figure 82. PAP path AB Gain Attenuation Step Register (PAP\_GAIN\_AB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. PAP\_GAIN\_AB Field Descriptions

Bit	Field	Type	Reset	Description
15:10	NOT USED	RW	000000	Not Used
9:0	PAPAB_GAIN_STEP		0x000	Gain attenuation step

### 8.5.32 PAP path AB Wait Time Register (address = 0x2A) [reset = 0x0000]

**Figure 83. PAP path AB Wait Time Register (PAP\_WAIT\_AB)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 73. PAP\_WAIT\_AB Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	Reserved	000000	R/W	Reserved
9:0	PAPAB_WAIT	0x000	R/W	Number of clock cycles to wait after gain = 0

### 8.5.33 PAP path CD Gain Attenuation Step Register (address = 0x2B) [reset = 0x0000]

**Figure 84. PAP path CD Gain Attenuation Step Register (PAP\_GAIN\_CD)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 74. PAP\_GAIN\_CD Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	Not Used	R/W	000000	Not Used
9:0	PAPCD_GAIN_STEP	R/W	0x000	Gain attenuation step

### 8.5.34 PAP Path CD Wait Time Register (address = 0x2C) [reset = 0x0000]

**Figure 85. PAP path CD Wait Time Register (PAP\_WAIT\_CD)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 75. PAP\_WAIT\_CD Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000	Reserved
9:0	PAPCD_WAIT	R/W	0x000	Number of clock cycles to wait after gain = 0

### 8.5.35 PAP path AB Configuration Register (address = 0x2D) [reset = 0x0FFF]

Figure 86. PAP path AB Configuration Register (PAP\_CFG\_AB)

15	14	13	12	11	10	9	8
0	0	Reserved	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. PAP\_CFG\_AB Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PAPAB_SEL_DLY	R/W	00	Controls the length of the delayline in the PAP AB logic. 00 : N = 32 01 : N = 64 10 : N = 128 11 : Not Valid
13	Reserved	R/W	0	Reserved
12:0	PAPAB_THRESH	R/W	0xFFFF	The threshold for the PAP AB trigger.

### 8.5.36 PAP path CD Configuration Register (address = 0x2E) [reset = 0x0FFF]

Figure 87. PAP path CD Configuration Register (PAP\_CFG\_CD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. PAP\_CFG\_CD Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PAPCD_SEL_DLY	R/W	00	Controls the length of the delay line in the PAP CD logic. 00 : N = 32 01 : N = 64 10 : N = 128 11 : Not Valid
13	Reserved	R/W	0	Reserved
12:0	PAPCD_THRESH	R/W	0xFFFF	The threshold for the PAP CD trigger.



**8.5.37 DAC SPI Configuration Register (address = 0x2F) [reset = 0x0000]**
**Figure 88. DAC SPI Constant 1 Register (SPIDAC\_TEST1)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 78. SPIDAC\_TEST1 Field Descriptions**

Bit	Field	Type	Reset	Description
15	TITEST_SKIPJESD	R/W	0	Bypasses the JESD logic
14:1	Reserved	R/W	0x0000	Reserved
0	SPIDAC_ENA	R/W	0	When asserted the DAC output is set to the value in register SPIDAC. This can be used for trim setting and other static tests.

**8.5.38 DAC SPI Constant Register (address = 0x30) [reset = 0x0000]**
**Figure 89. DAC SPI Constant Register (SPIDAC\_TEST2)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 79. SPIDAC\_TEST2 Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPIDAC	R/W	0x0000	This value replaces the data at the output of the JESD so that the DAC value can be controlled

### 8.5.39 Gain for path AB Register (address = 0x32) [reset = 0x0000]

Figure 90. Gain for path AB Register (GAINAB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. GAINAB Field Descriptions

Bit	Field	Type	Reset	Description
15	GAINAB_ENA	R/W	0	Turns on the path AB gain block
14:12	Reserved	R/W	0x0	Reserved
11:0	GAINAB	R/W	0x400	Extra control of gain in the GAINAB block. This allows a fix gain to be added to the signal if needed.

### 8.5.40 Gain for path CD Register (address = 0x33) [reset = 0x0000]

Figure 91. Gain for path CD Register (GAINCD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. GAINCD Field Descriptions

Bit	Field	Type	Reset	Description
15	GAINCD_ENA	R/W	0	Turns on the Path CD gain block
14:12	Reserved	R/W	0x0	Reserved
11:0	GAINCD	R/W	0x400	Extra control of gain in the GAINCD block. This allows a fix gain to be added to the signal if needed.

**8.5.41 JESD Error Counter Register (address = 0x41) [reset = 0x0000]**
**Figure 92. JESD Error Counter Register (JESD\_ERR\_CNT)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 82. JESD\_ERR\_CNT Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	JESD_ERR_CNT	R	0x0000	This is the error count for the JESD link. This is a 16bit value that is not cleared until the JESD synchronization is required or errcnt_clr is programmed to '1'

**8.5.42 JESD ID 1 Register (address = 0x46) [reset = 0x0044]**
**Figure 93. JESD ID 1 Register (JESD\_ID1)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 83. JESD\_ID1 Field Descriptions**

Bit	Field	Type	Reset	Description
15:11	LID0	R/W	00000	JESD ID for lane 0
10:6	LID1	R/W	00001	JESD ID for lane 1
5:1	LID2	R/W	00010	JESD ID for lane 2
0	Reserved	R/W	0	Reserved

### 8.5.43 JESD ID 2 Register (address = 0x47) [reset = 0x190A]

Figure 94. JESD ID 2 Register (JESD\_ID2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. JESD ID 2 Register (JESD\_ID2)

Bit	Field	Type	Reset	Description
15:11	LID3	R/W	00011	JESD ID for lane 3
10:6	LID4	R/W	00100	JESD ID for lane 4
5:1	LID5	R/W	00101	JESD ID for lane 5
0	Reserved	R/W	0	Reserved

### 8.5.44 JESD ID 3 and Subclass Register (address = 0x48) [reset = 0x31C3]

Figure 95. JESD ID 3 Register (JESD\_ID3)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. JESD\_ID3 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	LID6	R/W	00110	JESD ID for lane 6
10:6	LID7	R/W	00111	JESD ID for lane 7
5:4	Reserved	R/W	00	Reserved
3:1	SUBCLASSV	R/W	001	Selects the JESD subclass supported. Note: "001" is subclass 1 and "000" is subclass 0 they are the only modes supported; not used for operation but used for configuration. See field MIN_LATENCY_ENA in register JESD_MATCH (9.5.46) for use in subclass0
0	JESDV	R/W	1	Selects the version of JESD support(0=A; 1=B) NOTE: JESD 204B is only supported version.

**8.5.45 JESD Lane Enable Register (address = 0x4A) [reset = 0x0003]**
**Figure 96. JESD Lane Enable Register (JESD\_LN\_EN)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 86. JESD\_LN\_EN Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	LANE_ENA		0x00	Turn on each lane as needed. Signal is active high. bit 15 : lane7 enable bit 14 : lane6 enable bit 13 : lane5 enable bit 12 : lane4 enable bit 11 : lane3 enable bit 10 : lane2 enable bit 9 : lane1 enable bit 8 : lane0 enable
7:6	JESD_TEST_SEQ		00	Set to select and verify link layer test sequences. The error for these sequences comes out the lane alarms bit0. 1= a fail and 0 = pass. 00 : test sequence disabled 01 : verify repeating D.21.5 high frequency pattern for random jitter 10 : verify repeating K.28.5 mixed frequency pattern for deterministic jitter 11 : verify repeating ILA sequence
5:2	Reserved		0x0	Reserved
1:0	JESD_PHASE_MODE		11	Used to tell the JESD block how many clock phases are being used for lanes. 00 = 1 phase 01 = 2 phases 10 = 4 phases 11 = 8 phases

### 8.5.46 JESD RBD Buffer and Frame Octets Register (address = 0x4B) [reset = 0x1300]

Figure 97. JESD RBD Buffer and Frame Octets Register (JESD\_RBD\_F)

15	14	13	12	11	10	9	8
			0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0		0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. JESD\_RBD\_F Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	00	Reserved
12:8	RBD	R/W	10011	This controls the amount of elastic buffers being used in the JESD. Larger numbers will mean more latency; but smaller numbers may not hold enough data to capture the input skew. This value must always be $\leq \text{mem\_k}$
7:0	F_M1	R/W	0x00	This is the number of octets in the frame - 1

### 8.5.47 JESD K and L Parameters Register (address = 0x4C) [reset = 0x1303]

Figure 98. JESD K and L Parameters Register (JESD\_K\_L)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. JESD\_K\_L Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12:8	K_M1	R/W	10011	The number of frames in a multi-frame - $1. 0 \leq k - 1 < 32$
7:5	Reserved	R/W	0	Reserved
4:0	L_M1	R/W	00011	The number of lanes used by the JESD - $1. 0 \leq L - 1 < 8$

**8.5.48 JESD M and S Parameters Register (address = 0x4D) [reset = 0x0100]**
**Figure 99. JESD M and S Parameters Register (JESD\_M\_S)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 89. JESD\_M\_S Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	M_M1	R/W	0x01	The number of streams per frame - 1. $0 \leq M - 1 < 256$
7:5	Reserved	R/W	000	Reserved
4:0	S_M1	R/W	00000	The number of samples per stream per frame - 1.

**8.5.49 JESD N, HD and SCR Parameters Register (address = 0x4E) [reset = 0x0F4F]**
**Figure 100. JESD N, HD and SCR Parameters Register (JESD\_N\_HD\_SCR)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 90. JESD\_N\_HD\_SCR Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12:8	NPRIME_M1	R/W	01111	The number of adjusted bits per sample - 1
7	Reserved	R/W	0	Reserved
6	HD	R/W	1	High density mode. Samples can cross the lane boundary
5	SCR	R/W	0	Turn on the scrambler
4:0	N_M1	R/W	01111	The number of bits per sample - 1

### 8.5.50 JESD Character Match and Other Register (address = 0x4F) [reset = 0x1CC1]

Figure 101. JESD Character Match and Other Parameters Register (JESD\_MATCH)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. JESD\_MATCH Field Descriptions

Bit	Field	Type	Reset	Description
15:8	MATCH_DATA	R/W	0x1C	The character to match for buffer release. Normally it is a /R/=/K28.0/-0x1C but with these bits the user can program the value.
7	MATCH_SPECIFIC	R/W	1	Match a specific charater to start the JESD buffering when asserted; otherwise the first non-K will start the buffering.
6	MATCH_CTRL	R/W	1	When asserted the match character is a CONTROL character instead of a DATA character.
5	NO_LANE_SYNC	R/W	0	Assert if the TX side does not support lane initialization. This way the RX won't flag errors in the configuration portion of the ILA.
4:2	Not Used	R/W	000	Not Used
1	MIN_LATENCY_ENA	R/W	0	Enable minimum latency when set. This is needed for subclass 0 support.
0	JESD_COMMAALIGN_ENA	R/W	1	When asserted the JESD block SERDES comma align signal will be added with the SERDES ALIGN bit(0) to control when to shut off comma alignment. When this bit is deasserted; then the programmed bit(spi_config62(11)) is the only control.



**8.5.51 JESD Link Configuration Data Register (address = 0x50) [reset = 0x0000]**
**Figure 102. JESD Link Configuration Data Register (JESD\_LINK\_CFG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 92. JESD\_Link\_CFG Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	ADJCNT	R/W	0x0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
11	ADJDIR	R/W	0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
10-7	BID	R/W	0x0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
6-2	CF	R/W	00000	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
1-0	CS	R/W	00	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.

**8.5.52 JESD Sync Request Register (address = 0x51) [reset = 0x00FF]**
**Figure 103. JESD Sync Request Register (JESD\_SYNC\_REQ)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 93. JESD\_SYNC\_REQ Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	DID	R/W	0x00	Lane configuration
7:0	SYNC_REQUEST	R/W	0xFF	These bits select which errors cause a sync request. Sync requests take priority over the error notification; so if sync request isn't desired; set these bits to a '0'. bit 7 = multi-frame alignment error bit 6 = frame alignment error bit 5 = link configuration error bit 4 = elastic buffer overflow (bad RBD value) bit 3 = elastic buffer end char mismatch (match_ctrl match_data) bit 2 = code synchronization error bit 1 = 8b/10b not-in-table code error bit 0 = 8b/10b disparity error

### 8.5.53 JESD Error Output Register (address = 0x52) [reset = 0x00FF]

Figure 104. JESD Error Output Register (JESD\_ERR\_OUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. JESD\_ERR\_OUT Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000	Reserved
9	DISABLE_ERR_RPT	R/W	0	Assertion means that errors will not be reported on the sync_n output.
8	PHADJ	R/W	0	Lane configuration
7:0	ERR_ENA	R/W	0xFF	These bits select the errors generated are counted in the err_c for the link. The bits also control what signals are sent out the pad_syncb pin for error notification. bit 7 = multi-frame alignment error bit 6 = frame alignment error bit 5 = link configuration error bit 4 = elastic buffer overflow (bad RBD value) bit 3 = elastic buffer end char mismatch (match_ctrl match_data) bit 2 = code synchronization error bit 1 = 8b/10b not-in-table code error bit 0 = 8b/10b disparity error

### 8.5.54 JESD ILA Check 1 Register (address = 0x53) [reset = 0x0100]

Figure 105. JESD ILA Check 1 Register (JESD\_ILA\_CFG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. JESD\_ILA\_CFG1 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ILA_M	R/W	0x01	JESD M-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
7:0	ILA_F	R/W	0x00	JESD F-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode

**8.5.55 JESD ILA Check 2 Register (address = 0x54) [reset = 0x8E60]**
**Figure 106. JESD ILA Check 2 Register (JESD\_ILA\_CFG2)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 96. JESD\_ILA\_CFG2 Field Descriptions**

Bit	Field	Type	Reset	Description
15	ILA_HD	R/W	1	JESD HD configuration value used only for ILA checking; may be set independently of the actual JESD mode
14:10	ILA_L	R/W	00011	JESD L-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
9:5	ILA_K	R/W	10011	JESD K-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
4:0	ILA_S	R/W	00000	JESD S-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode

**8.5.56 JESD SYSREF Mode Register (address = 0x5C) [reset = 0x0001]**
**Figure 107. JESD SYSREF Mode Register (JESD\_SYSR\_MODE)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 97. JESD\_SYSR\_MODE Field Descriptions**

Bit	Field	Type	Reset	Description
15:4	Reserved	R/W	0x000	Reserved
3	ERR_CNT_CLR	R/W	0	A transition from 0->1 causes the error_cnt to be cleared
2:0	SYSREF_MODE	R/W	001	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = skip two SYSREFs and then use one 110 = skip two SYSREFs and then use all

### 8.5.57 JESD Crossbar Configuration 1 Register (address = 0x5F) [reset = 0x0123]

Figure 108. JESD Crossbar Configuration 1 Register (JESD\_CROSSBAR1)

15	14	13	12	11	10	9	8
Reserved	0	0	0	Reserved	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. JESD\_CROSSBAR1 Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	OCTETPATH0_SEL	R/W	000	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
11	Reserved	R/W	0	Reserved
10:8	OCTETPATH1_SEL	R/W	001	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
7	Reserved	R/W	0	Reserved
6:4	OCTETPATH2_SEL	R/W	010	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
3	Reserved	R/W	0	Reserved
2:0	OCTETPATH3_SEL	R/W	011	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7

**8.5.58 JESD Crossbar Configuration 2 Register (address = 0x60) [reset = 0x4567]**
**Figure 109. JESD\_CROSSBAR2 Field DBits to Determine What Version of Build for the chip.escrptions**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 99. JESD\_CROSSBAR2 Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	OCTETPATH4_SEL	R/W	100	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
11	Reserved	R/W	0	Reserved
10:8	OCTETPATH5_SEL	R/W	101	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
7	Reserved	R/W	0	Reserved
6:4	OCTETPATH6_SEL	R/W	110	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
3	Reserved	R/W	0	Reserved
2:0	OCTETPATH7_SEL	R/W	111	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7

**8.5.59 JESD Alarms for Lane 0 Register (address = 0x64) [reset = 0x0000]**

**Figure 110. JESD Alarms for Lane 0 Register (JBits to determine what version of build for the chip.ESD\_ALM\_L0)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 100. JESD\_ALM\_L0 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE0_ERR	W0C	0x00	Lane0 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO0_FLAGS	W0C	0x0	Lane0 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

**8.5.60 JESD Alarms for Lane 1 Register (address = 0x65 01100101) [reset = 0x0000]**
**Figure 111. JESD Alarms for Lane 1 Register (JESD\_ALM\_L1)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 101. JESD\_ALM\_L1 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE1_ERR	W0C	0x00	Lane1 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO1_FLAGS	W0C	0x0	Lane1 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

**8.5.61 JESD Alarms for Lane 2 Register (address = 0x66) [reset = 0x0000]**

**Figure 112. JESD Alarms for Lane 2 Register (JESD\_ALM\_L2)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	1	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 102. JESD\_ALM\_L2 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE2_ERR	W0C	0x00	Lane2 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO2_FLAGS	W0C	0x0	Lane2 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty



**8.5.62 JESD Alarms for Lane 3 Register (address = 0x67) [reset = 0x0000]**
**Figure 113. JESD Alarms for Lane 3 Register (JESD\_ALM\_L3)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	1	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 103. JESD\_ALM\_L3 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE3_ERR	W0C	0x00	Lane3 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO3_FLAGS	W0C	0x0	Lane3 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

**8.5.63 JESD Alarms for Lane 4 Register (address = 0x68) [reset = 0x0000]**

**Figure 114. JESD Alarms for Lane 4 Register (JESD\_ALM\_L4)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 104. JESD\_ALM\_L4 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE4_ERR	W0C	0x00	Lane4 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO4_FLAGS	W0C	0x0	Lane4 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

**8.5.64 JESD Alarms for Lane 5 Register (address = 0x69) [reset = 0x0000]**
**Figure 115. 8.4.60 JESD Alarms for Lane 5 Register (address = 0x69) [reset = 0x0000]**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 105. JESD\_ALM\_L5 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE5_ERR	W0C	0x00	Lane5 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO5_FLAGS	W0C	0x0	Lane5 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

**8.5.65 JESD Alarms for Lane 6 Register (address = 0x6A [reset = 0x0000])**

**Figure 116. JESD Alarms for Lane 6 Register (JESD\_ALM\_L6)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 106. JESD\_ALM\_L6 Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	ALM_LANE6_ERR	W0C	0x00	Lane6 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO6_FLAGS	W0C	0x0	Lane6 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

8.5.66 JESD Alarms for Lane 7 Register (address = 0x6B) [reset = 0x0000]

Figure 117. JESD Alarms for Lane 7 Register (JESD\_ALM\_L7)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 107. JESD Alarms for Lane 7 Register (JESD\_ALM\_L7)

Bit	Field	Type	Reset	Description
15:8	ALM_LANE7_ERR	W0C	0x00	Lane7 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO7_FLAGS	W0C	0x0	Lane7 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

8.5.67 SYSREF and PAP Alarms Register (address = 0x6C) [reset = 0x0000]

Figure 118. SYSREF and PAP Alarms Register (ALM\_SYSREF\_PAP)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 108. ALM\_SYSREF\_PAP Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	W0C	0	Reserved
12	ALM_SYSREF_ERR	W0C		Alarm caused when the sysref is placed at an incorrect location
11	ALM_FROM_SHORTTEST	W0C		This is the alarm from JESD during the SHORT TEST checking.
10:7	ALM_PAP	W0C	0x0	The alarms from the PAP blocks indicated which PAP was triggered. bit0 = PAPA bit1 = PAPB bit2 = PAPC bit3 = PAPD
6:2	Reserved	W0C	0x0	Reserved
1	ALM_DIV192_ZERO	W0C	0	This is asserted if the clkdiv192 in the CDRV_SER shift register is all zeros.
0	Not Used	W0C	0	Not Used

**8.5.68 Clock Divider Alarms 1 Register (address = 0x6D) [reset = 0x0000]**

**Figure 119. Clock Divider Alarms 1 Register (ALM\_CLKDIV1)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

**Table 109. ALM\_CLKDIV1 Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALM_DIV8_ZERO	W0C	0	Asserted if the clkdiv8 in the CDRV_SER shift register is all zeros.
14	ALM_DIV12_ZERO	W0C	0	Asserted if the clkdiv12 in the CDRV_SER shift register is all zeros.
13	ALM_DIV16_ZERO	W0C	0	Asserted if the clkdiv16 in the CDRV_SER shift register is all zeros.
12	ALM_DIV24_ZERO	W0C	0	Asserted if the clkdiv24 in the CDRV_SER shift register is all zeros. (Connected to the div18 port)
11	ALM_DIV20_ZERO	W0C	0	Asserted if the clkdiv20 in the CDRV_SER shift register is all zeros.
10	ALM_DIV32_ZERO	W0C	0	Asserted if the clkdiv32 in the CDRV_SER shift register is all zeros.
9	ALM_DIV36_ZERO	W0C	0	Asserted if the clkdiv36 in the CDRV_SER shift register is all zeros.
8	ALM_DIV40_ZERO	W0C	0	Asserted if the clkdiv40 in the CDRV_SER shift register is all zeros.
7	ALM_DIV48_ZERO	W0C	0	Asserted if the clkdiv48 in the CDRV_SER shift register is all zeros.
6	ALM_DIV64_ZERO	W0C	0	Asserted if the clkdiv64 in the CDRV_SER shift register is all zeros.
5	ALM_DIV72_ZERO	W0C	0	Asserted if the clkdiv72 in the CDRV_SER shift register is all zeros.
4	ALM_DIV80_ZERO	W0C	0	Asserted if the clkdiv80 in the CDRV_SER shift register is all zeros.
3	ALM_DIV96_ZERO	W0C	0	Asserted if the clkdiv96 in the CDRV_SER shift register is all zeros.
2	ALM_DIV128_ZERO	W0C	0	Asserted if the clkdiv128 in the CDRV_SER shift register is all zeros.
1	ALM_DIV144_ZERO	W0C	0	Asserted if the clkdiv144 in the CDRV_SER shift register is all zeros.
0	ALM_DIV160_ZERO	W0C	0	Asserted if the clkdiv160 in the CDRV_SER shift register is all zeros.

**8.5.69 Clock Configuration Register (address = 0x0A) [reset = 0xF000]**
**Figure 120. Clock Configuration Register (CLK\_CONFIG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 110. CLK\_CONFIG Field Descriptions**

Bit	Field	Type	Reset	Description
15	RCLK_SYNC_ENA	RW	1	When asserted the sysref is used to sync the clock divider in the centralclkdiv. This should be disabled after initial syncing.
14	FRCLK_DIV_ENA	RW	1	When asserted the full rate clock divider that provides the DIV4 phases to the DACs is enabled
13	DACA_FRCLK_ENA	RW	1	When asserted the full rate clock to the DACA block is enabled
12	DACB_FRCLK_ENA	RW	1	When asserted the full rate clock to the DACB block is enabled
11	DACA_DUMDATA	RW	0	Enables dummy data generation for DACA when set high
10	DACB_DUMDATA	RW	0	Enables dummy data generation for DACB when set high
9:2	Reserved	RW	0x000	Reserved
1	QRCLOCK_DACA_ENA	RW	1	Turns on the quarter rate clock for DACA when '1'
0	QRCLOCK_DACB_ENA	RW	1	Turns on the quarter rate clock for DACB when '1'

**8.5.70 Sleep Configuration Register (address = 0x0B) [reset = 0x0022]**
**Figure 121. Clock Configuration Register (SLEEP\_CONFIG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 111. SLEEP\_CONFIG Field Descriptions**

Bit	Field	Type	Reset	Description
15:9	Reserved	RW	0000000	Reserved
8	VBGR_SLEEP	RW	0	Turns off the 'bandgap-over-R' bias
7	Reserved	RW	0	Reserved
6	TSENSE_SLEEP	RW	0	Turns off the temperature sensor
5	PLL_SLEEP	RW	1	Puts the PLL into sleep mode (FUSE Controlled)
4	CLKRECV_SLEEP	RW	0	When asserted the clock input receiver gets put into sleep mode. This also affects the FIFO_OSTR receiver as well.
3	DACA_SLEEP	RW	0	Puts the DACA into sleep mode
2	DACB_SLEEP	RW	0	Puts the DACB into sleep mode
1	CLK_TX_SLEEP	RW	1	When asserted the PLL TX clock output is in low power mode.
0	Reserved	RW	0	Reserved

### 8.5.71 Divided Output Clock Configuration Register (address = 0x0C) [reset = 0x8000]

Figure 122. Divided Output Clock Configuration Register (CLK\_OUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 112. CLK\_OUT Field Descriptions

Bit	Field	Type	Reset	Description
15	CLK_TX_IDLE	R/W	1	When high puts the CLK_TX circuitry in idle mode during which the CLKTX+ and CLKTX- output pins are driven to the proper common-mode levels in order to charge the external AC coupling caps. When low allows the divided clock to be driven onto the CLKTX+ and CLKTX- output pins.
14:13	CLK_TX_DIVSELECT	R/W	01	Selects either div2, div3 or div 4 output. 00 = divided by 3 01 = divided by 4 10 = divided by 2 11 = not valid
12	Reserved	R/W	0	Reserved
11:8	CLK_TX_SWING	R/W	0x0	Sets desired swing on CLKTX+ and CLKTX- outputs in mVpp-diff 0x0 125 0x1 232 0x2 337 0x3 440 0x4 540 0x5 639 0x6 736 0x7 831 0x8 924 0x9 1012 0xA 1097 0xB 1178 0xC 1255 0xD 1329 0xE 1398 0xF 1462
7:3	Reserved	R/W	00000	Reserved
2	CLK_TX_FLIP	R/W	0	Flips the polarity of CLKTX
1	TX_SYNC_ENA	R/W	1	Syncs the CLKTX with SYSREF when asserted
0	EXTREF_ENA	R/W	0	Allows the chip to use an external reference(1) or the internal reference(0)



### 8.5.72 DAC Fullscale Current Register (address = 0x0D) [reset = 0xF000]

**Figure 123. DAC Fullscale Current Register (DACFS)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 113. DACFS Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	DACFS	R/W	0xF	Scales the output current in 16 equal steps from 10-40mA (10mA + 2mA*DACFS)
10:0	Reserved	R/W	0x000	Reserved

### 8.5.73 Internal SYSREF Generator Register (address = 0x10) [reset = 0x0000]

**Figure 124. Internal SYSREF Register (LCMGEN)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 114. LCMGEN Field Descriptions**

Bit	Field	Type	Reset	Description
15:4	Reserved	R/W	0x00	Reserved
3	LCMGEN_ENA	R/W	0	Enables the LCM custom logic
2	LCMGEN_RESET	R/W	0	Reset the LCM custom logic
1	LCMGEN_SPI_SYSREF_ENA	R/W	0	TBD
0	LCM_SYSREF_OUTSEL	R/W	0	Chooses between internal and external SYSREF

### 8.5.74 Counter for Internal SYSREF Generator Register (address = 0x11) [reset = 0x0000]

**Figure 125. Counter for Internal SYSREF Generator Register (LCMGEN\_DIV)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 115. LCMGEN\_DIV Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	LCMGEN_DIV	R/W	0x00	Counter setting for the LCMGEN block

### 8.5.75 SPI SYSREF for Internal SYSREF Generator Register (address = 0x12) [reset = 0x0000]

Figure 126. SPI SYSREF for Internal SYSREF Generator Register (LCMGEN\_SPISYSREF)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 116. LCMGEN\_SPISYSREF Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	0x00	Reserved
0	LCMGEN_SPI_SYSREF	R/W	0	SPI SYSREF for the LCMGEN block

### 8.5.76 Digital Test Signals Register (address = 0x1B) [reset = 0x0000]

Figure 127. Digital Test Signals Register (DTEST)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 117. DTEST Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	DTEST_LANE	R/W	000	Selects the lane to check for the signals selected by field DTEST
11:8	DTEST	R/W	0x0	Allows digital test signals to come out the ALARM pin. 0000 : Test disabled; normal ALARM pin function 0001 : SERDES lanes 0 – 3 PLL clock/80 0010 : SERDES lanes 4 – 7 PLL clock/80 0011 : TESTFAIL (lane selected by field DTEST_LANE) 0100 : SYNC (lane selected by field DTEST_LANE) 0101 : OCIP (lane selected by field DTEST_LANE) 0110 : EQUNDER (lane selected by field DTEST_LANE) 0111 : EQOVER (lane selected by field DTEST_LANE) 1000 – 1111 : not used
7:0	Reserved	R/W	0x00	Reserved

### 8.5.77 Sleep Pin Control Register (address = 0x23) [reset = 0xFFFF]

These fields control the routing of the SLEEP signal to different blocks. Assertion means that the SLEEP signal will be sent to the block. These bits do not override the SPI bits; just the SLEEP signal from the PAD.

**Figure 128. Sleep Pin Control Register (SLEEP\_CNTL)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 118. SLEEP\_CNTL Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	11111	Reserved
9	CLKOUT_SLEEP	R/W	1	Allows the output clock to sleep
8	BG_SLEEP	R/W	1	Allows the band gap to sleep
7	TEMP_SLEEP	R/W	1	Allows the temp sensor to sleep
6	PLL_CP_SLEEP	R/W	1	Allows the PLL charge pump to sleep
5	PLL_SLEEP	R/W	1	Allows the PLL to sleep
4	CLK_RECV_SLEEP	R/W	1	Allows the clock receiver to sleep
3:2	Reserved	R/W	11	Reserved
1	DACB_SLEEP	R/W	1	Allows DACB to sleep
0	DACA_SLEEP	R/W	1	Allows DACA to sleep

### 8.5.78 SYSREF Capture Circuit Control Register (address = 0x24) [reset = 0x1000]

Figure 129. SYSREF Capture Circuit Control Register (SYSR\_CAPTURE)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 119. SYSR\_CAPTURE Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSR_PHASE_WDW	R/W	00	sysref phase alignment tolerance window Centers sysref capture window as follows: 00 = Centered on phase $\phi_{12}$ (**DEFAULT**) 01 = Centered on phase $\phi_{23}$ 10 = Centered on phase $\phi_{34}$ 11 = Centered on phase $\phi_{41}$
13:12	SYSR_ALIGN_DLY	R/W	01	sysref alignment offset delay Optional alignment offset that allows system designer to work around hardware (e.g. PCB) alignment errors by letting him specify that the sysref pulse should be treated as occurring one device clock earlier or later than its observed position. Legal settings are as follows: 00 = Offset by -1 device clock cycles. Treat sysref as if it were captured 1 cycle earlier. 01 = No offset (**DEFAULT**) 10 = Offset by +1 device clock cycles. Treat sysref as if it were captured 1 cycle later. 11 = Reserved
11	SYSR_STATUS_ENA	R/W	0	Enable alignment status monitoring Enable logic that generates sysref alignment status information and accumulates statistics that can be read by the user. 0 = Disable sysref alignment status outputs (**DEFAULT**). Used during normal operation. 1 = Enable sysref alignment status outputs. Used when characterizing sysref capture timing.
10:2	Reserved	R/W	0x000	Reserved
1	SYSR_ALIGN_SYNC	R/W	0	Write a '1' to this bit to clear accumulated sysref align statistics
0	SYSR_BYPS_ALIGN	R/W	0	Bypass sysref alignment logic. Bypass the 4x oversampled sysref alignment logic and instead capture the sysref signal using the legacy implementation of a flip-flop clocked directly by the rising edge of the device clock. 0 = Capture sysref using full-featured alignment circuit (**DEFAULT**) 1 = Bypass sysref alignment logic NOTE: When mem_sysref_bypass_align is enabled, the other sysref alignment controls have no effect.

**8.5.79 Clock Input and PLL Configuration Register (address = 0x31) [reset = 0x0200]**
**Figure 130. Clock Input and PLL Configuration Register (CLK\_PLL\_CFG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 120. Clock Input and PLL Configuration Register (CLK\_PLL\_CFG)**

Bit	Field	Type	Reset	Description
15:14	Reserved	R/W	00	Reserved
13	SEL_EXTCLK_DIFFSE	R/W	0	Selects the external differential or single ended clock for DACCLK. 0 = differential 1 = single ended
12	PLL_RESET	R/W	0	When set the M divider; N divider and PFD are held reset
11	PLL_NDIVSYNC_ENA	R/W	0	When asserted; the SYSREF input is used to sync the N dividers of the PLL.
10	PLL_ENA	R/W	0	Enables the PLL output as the DAC clock when set; the clock provided at the DACCLKP/N is used as the PLL reference clock. When cleared; the PLL is bypassed and the clock provided at the DACCLKP/N pins is used as the DAC clock
9	PLL_CP_SLEEP	R/W	1	Must be set to '0' for proper PLL operation. 1 = Charge pump is put to sleep and can be driven by external source through the ATEST pins.
8	Reserved	R/W	0	Reserved
7:3	PLL_N_M1	R/W	00000	Reference clock divider; divide by is N+1
2:0	LOCKDET_ADJ	R/W	000	Adjusts the lock detector sensitivity. Upper bit isn't used: x00 - highest sensitivity x11 - lowest sensitivity

### 8.5.80 PLL Configuration 1 Register (address = 0x32) [reset = 0x0308]

Figure 131. PLL Configuration 1 Register (PLL\_CONFIG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 121. CONFIG1 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PLL_M_M1	R/W	0x03	VCO feedback divider; divide by is 4(M+1)
7:4	Reserved	R/W	0x0	Reserved
3:0	PLL_VCO_RDAC	R/W	0x8	Controls the VCO amplitude

### 8.5.81 PLL Configuration 2 Register (address = 0x33) [reset = 0x4018]

Figure 132. PLL Configuration 2 Register (PLL\_CONFIG2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 122. PLL\_CONFIG2 Field Descriptions

Bit	Field	Type	Reset	Description
15	PLL_VCOSEL	R/W	0	Selects between two VCOs 0 = 5.9 GHz VCO(2 turn inductor in upper VCO) 1 = 8.9 GHz VCO (1 turn in the lower VCO)
14:8	PLL_VCO	R/W	1000000	VCO frequency range
7:6	Reserved	R/W	000	Reserved
5:2	PLL_CP_ADJ	R/W	0110	Adjusts the charge pump current; 0 to 1.55 mA in 50 µA steps. Setting to 0000 will hold the LPF pin at 0 V
1	Reserved	R/W	0	Reserved
0	GSMPLL_ENA	R/W	0	Enables the GSM PLL (coupled VCOs) if asserted

**8.5.82 LVDS Output Configuration Register (address = 0x34) [reset = 0x0000]**
**Figure 133. LVDS Output Configuration Register (LVDS\_CONFIG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 123. LVDS\_CONFIG Field Descriptions**

Bit	Field	Type	Reset	Description
15	LVDS_LOPW RB	R/W	0	LVDS Output current control LSB; allows output current to be scaled from ~2 mA to ~4 mA
14	LVDS_LOPW RA	R/W	0	LVDS Output current control MSB; allows output current to be scaled from ~2 mA to ~4 mA
13	LVDS_LPSEL	R/W	0	<p><math>\overline{\text{SYNC}}</math> LVDS output on chip termination control; 100 <math>\Omega</math> when cleared; 200 <math>\Omega</math></p> <p>Output current settings for the combination of bits 15:13</p> <p>110 = 4.00 mA  010 = 3.50 mA  100 = 3.00 mA  000 = 2.50 mA – Default current  111 = 4.00 mA  011 = 3.33 mA  101 = 2.66 mA  001 = 2.00 mA</p>
12	LVDS_EFUSE_SEL	R/W	0	Enable LVDS bias bandgap reference voltage to the ATEST multiplexer.
11:10	LVDS_TRIM	R/W	00	<p>Adjusts the LVDS 1.2 V reference. LVDS_TRIM_ENA must be set and LVDS_EFUSE_SEL must be cleared for these bits to have any effect.</p> <p>10 +70 mV  00 -70 mV  01 default  11 -20 mV.</p>
9	LVDS_TRIM_ENA	R/W	0	When set and LVDS_EFUSE_SEL is cleared; the LVDS_TRIM adjustment is enabled. When cleared; the LVDS_TRIM has no effect.
8	LVDS_SYNC0_PD	R/W	0	The $\overline{\text{SYNC0}}$ LVDS output is in power down.
7	Reserved	R/W	0	Reserved
6	LVDS_SYNC0_CM	R/W	0	$\overline{\text{SYNC0}}$ LVDS output common mode is 1.2 V when cleared; 0.9 V when set.
5:0	Reserved	R/W	0x00	Reserved

**8.5.83 Fuse Farm clock divider Register (address = 0x35) [reset = 0x0018]**

**Figure 134. Fuse Farm clock divider Register (PLL\_FDIV)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/1W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after rese1t

**Table 124. PLL\_FDIV Field Descriptions**

Bit	Field	Type	Reset	Description
15	SERDES_CLK_SEL	R/W	0	Select either the PLL output of the DACCLK from the pad. 0 = DACCLK pad 1 = PLL output
14:11	SERDES_REFCLK_DIV	R/W	0x0	The divide amount for the serdes REFCLK
10:2	Reserved	R/W	0x000	Reserved
1:0	SERDES_REFCLK_PREDIV	R/W	10	These bits select the pre-divide on the DACCLK input clock before the DACCLK is used in the dividers used in the SERDES PLL REFCLK and the Fusefarm SYSCLK. 00 = if DACCLK input ≤ 2 GHz; prediv is set to div1 01 = if DACCLK input is ≤ 4 GHz and > 2 GHz, prediv is set to div2 10 = if DACCLK input is ≤ 9 GHz and > 4 GHz, prediv is set to div4 11 = Not valid



**8.5.84 Serdes Clock Configuration Register (address = 0x3B) [reset = 0x0002]**
**Figure 135. Serdes Clock Configuration Register (SRDS\_CLK\_CFG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after rese1t

**Table 125. SRDS\_CLK\_CFG Field Descriptions**

Bit	Field	Type	Reset	Description
15	SERDES_CLK_SEL	R/W	0	Select either the PLL output of the DACCLK from the pad. 0 = DACCLK pad 1 = PLL output
14:11	SERDES_REFCLK_DIV	R/W	0x0	The divide amount for the serdes REFCLK
10:2	Reserved	R/W	0x000	Reserved
1:0	SERDES_REFCLK_PREDIV	R/W	10	These bits select the pre-divide on the DACCLK input clock before the DACCLK is used in the dividers used in the SERDES PLL REFCLK and the Fusefarm SYSCLK. 00 = if DACCLK input ≤ 2 GHz; prediv is set to div1 01 = if DACCLK input is ≤ 4 GHz and > 2 GHz, prediv is set to div2 10 = if DACCLK input is ≤ 9 GHz and > 4 GHz, prediv is set to div4 11 = Not valid

**8.5.85 Serdes PLL Configuration Register (address = 0x3C) [reset = 0x8228]**
**Figure 136. Serdes PLL Configuration Register (SRDS\_PLL\_CFG)**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 126. SRDS\_PLL\_CFG Field Descriptions**

Bit	Field	Type	Reset	Description
15	ENDIVCLK	R/W	1	Enable divided by 5 output clock
14:3	CLKBYP	R/W	00	Serdes clock bypass
12:11	LB	R/W	00	Serdes PLL loop bandwidth
10	SLEEPPLL	R/W	0	Serdes PLL Sleep
9	VRANGE	R/W	1	Serdes PLL loop filter range
8:1	MPY	R/W	00010100	Serdes reference clock multiply factor
0	CORRECT	R/W	0	AND'ed with LANE_ENA so it must be set to 1 for correct behavior

**8.5.86 Serdes Configuration 1 Register (address = 0x3D) [reset = 0x0x0088]**

**Figure 137. Serdes Configuration 1 Register (SRDS\_CFG1)**

15		14		13		12		11		10		9		8	
0		0		0		0		0		0		0		x	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
7		6		5		4		3		2		1		0	
0		0		1		1		1		1		0		1	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 127. RDS\_CFG1 Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	TESTPATT	R/W	000	Test pattern
11	BSINRXN	R/W	0	Enable boundary scan - pins
10	BSINRXP	R/W	0	Enable boundary scan + pins
9:8	LOOPBACK	R/W	00	Enable loopback
7	ENOC	R/W	1	Enable Serdes offset compensation
6	EQHLD	R/W	0	Equalizer hold
5:3	EQ	R/W	001	Serdes equalizer
2:0	CDR	R/W	000	Clock data recovery algorithm settings

**8.5.87 Serdes Configuration 2 Register (address = 0x3E) [reset = 0x0x0909]**
**Figure 138. Serdes Configuration 2 Register (SRDS\_CFG2)**

15		14		13		12		11		10		9		8	
0		0		0		0		0		0		0		x	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
7		6		5		4		3		2		1		0	
0		0		1		1		1		1		1		0	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 128. SRDS\_CFG2 Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	LOS	R/W	000	Enables loss of signal detection. 000 - Enable detection 100 - Disable detection other - reserved
12:11	ALIGN	R/W	01	Enables external or internal symbol alignment
10:8	TERM	R/W	001	Valid programming: 001 – AC coupling with common mode = 0.7 V 100 – 0 V common mode. 101 – 0.25 V common mode 111 – DC coupling with common mode of 0.6 V. (NOTE: This is not compatible with JESD)
7	Reserved	R/W	0	Reserved
6:5	RATE	R/W	00	Selects full, half, quarter or eighth rate operation.
4:2	BUSWIDTH	R/W	010	Selects the parallel interface width (16 or 20 bits)
1	SLEEPRX	R/W	0	Powers the receiver down into the sleep (fast power up) state when high.
0	Reserved	R/W	1	Reserved

### 8.5.88 Serdes Polarity Control Register (address = 0x3F) [reset = 0x0000]

Figure 139. Serdes Polarity Control Register (SRDS\_POL)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 129. SRDS\_POL Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R/W	0x00	Reserved
7:0	INVPAIR	R/W	0x00	Allows the PN pairs of the different lanes to be inverted. bit 7 = lane7 bit 6 = lane6 bit 5 = lane5 bit 4 = lane4 bit 3 = lane3 bit 2 = lane2 bit 1 = lane1 bit 0 = lane0

### 8.5.89 JESD204B SYNCB OUTPUT Register (address = 0x76) [reset = 0x0000]

Figure 140. JESD204B SYNCB OUTPUT Register (SYNCBOUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 130. SYNCBOUT Field Descriptions

Bit	Field	Type	Reset	Description
15:2	Reserved	R/W	0x00	Reserved
1	SYNCBOUT1	R/W	0	If the CMOS SYNC outputs are turned on, this bit will show the status of the JESD SYNCB1 signal
0	SYNCBOUT0	R/W	0	If the CMOS SYNC outputs are turned on, this bit will show the status of the JESD SYNCB0 signal

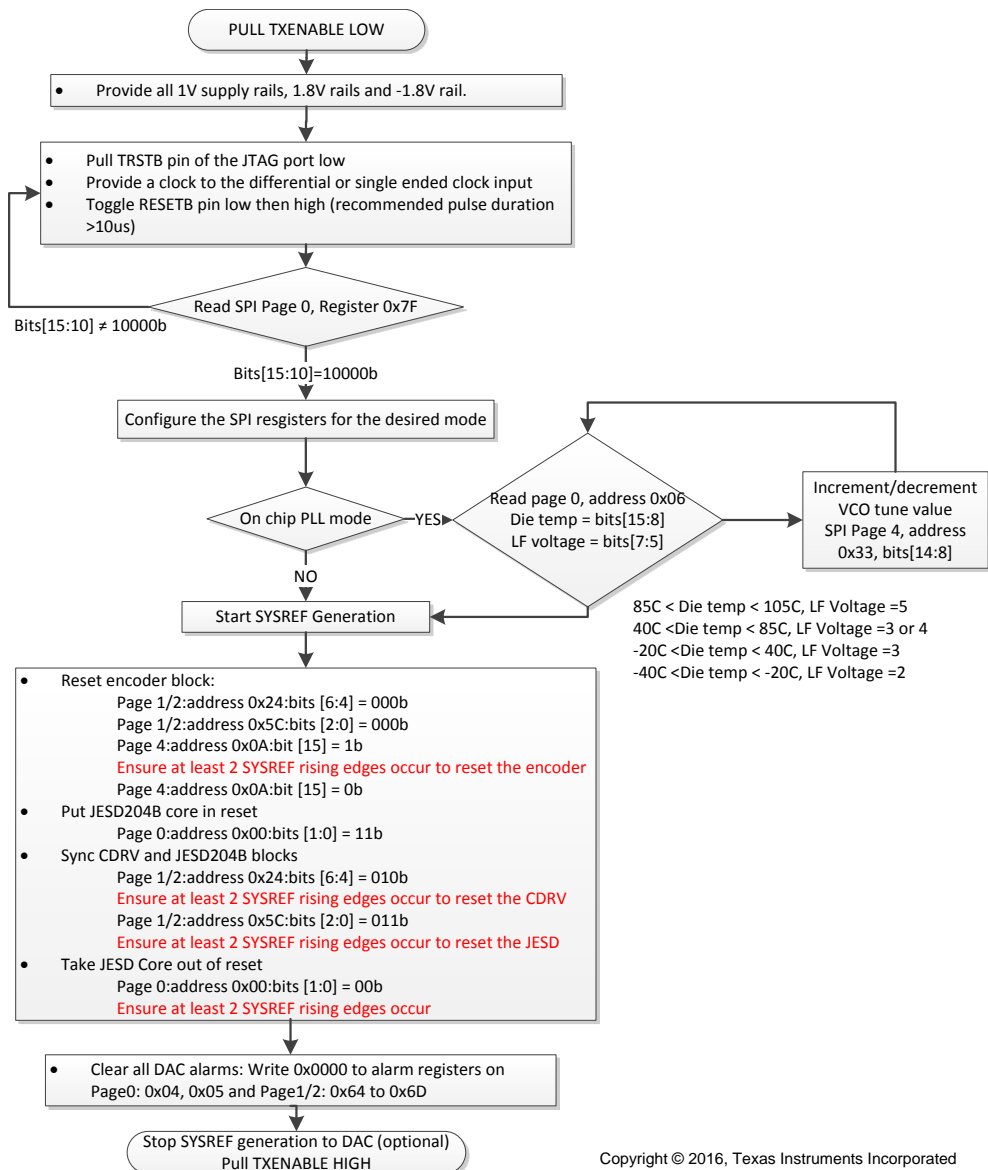
## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Start-up Sequence



Copyright © 2016, Texas Instruments Incorporated

Figure 141. DAC38RF8xx Recommended Startup Sequence

## 9.2 Typical Application: Multi-band Radio Frequency Transmitter

The DAC38RF8xx device family can be used in RF transmitters designed to support multiple operating bands. The two transmit antennae system shown in Figure 142 uses DAC38RF8xx to convert digital baseband signals from an FPGA directly to RF signals in LTE downlink band 1 (2110 MHz - 2170 MHz) and band 3 (1805 MHz - 1880 MHz).

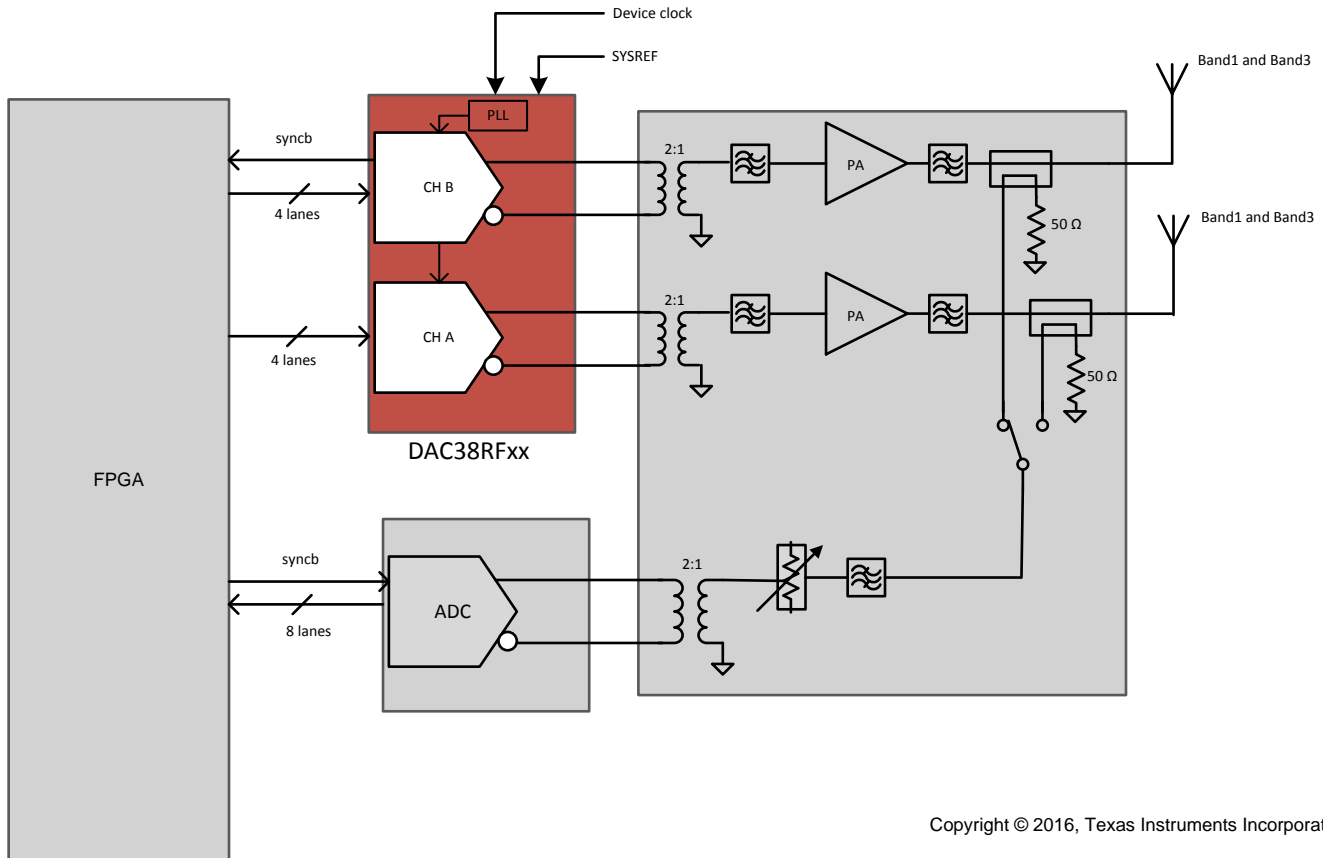


Figure 142. Two antennae multi-band Radio Frequency Transmitter

### 9.2.1 Design Requirements

Table 131. Dual band LTE downlink transmitter

Parameter	Value
Operating bands	Band 1 (2110 MHz - 2170 MHz) and Band 3 (1805 MHz to 1880 MHz)
Data rate (baseband)	368.64 MHz
Sampling frequency	8847.36 MHz
Interpolation	24
JESD204B Interface configuration	L-M-F-S-Hd = 8-8-2-1-0

## 9.2.2 Detailed Design Procedure

Two complex data streams of 20MHz LTE data generated in a baseband processor (FPGA/ASIC) is formatted based on [Table 18](#) and transmitted to DAC38RF8xx. Inside DAC38RF8xx, the complex input data at a rate of 368.64 MSPS is interpolated 24 times to the final output sampling rate of 8847.36 MSPS. This enables the final RF output to be positioned in the first Nyquist zone for minimal attenuation due to sinc(x) roll off. After interpolation, the output complex data stream is digitally mixed to the final RF frequencies. The digital mixing eliminates system imperfections such as local oscillator (LO) feed-through and sideband images that are inherent in analog mixers. Detailed block diagram is shown in [\(Figure 143\)](#)

To simplify the system clocking, a low frequency clock (or device clock) is provided as a reference to the on-chip PLL ([Internal PLL/VCO](#)) of DAC38RF8xx. The PLL generates a low phase noise, high frequency sampling clock from the low frequency reference.

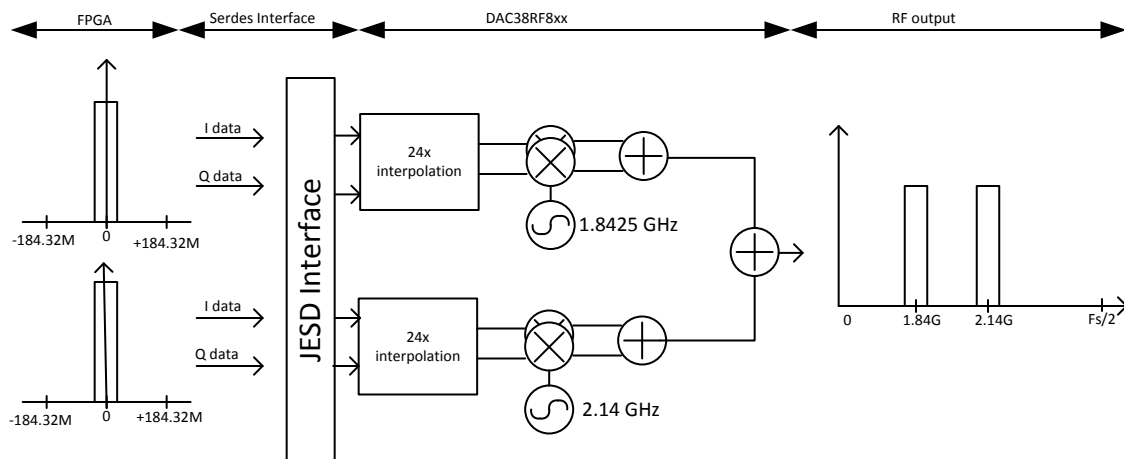


Figure 143. Dual band LTE Downlink Transmitter Block Diagram

### 9.2.2.1 Calculating the JESD204B Serdes Rate

Serdes rate =  $1.25 \times (M/L) \times \text{Baseband data rate} \times \text{Number of bits per sample}$  (16)

M is a JESD204B interface parameter that refers to the number of data streams from FPGA to DAC

L is a JESD204B interface parameter that refers to the number of serdes lanes used to transmit data

1.25 is a factor due to the 8B10B encoding of the baseband data

Example,

if the baseband data rate = 368.64 MSPS and L-M-F-S-Hd = 8-8-2-1-0

$$\text{Serdes rate} = 1.25 \times (8/8) \times 368.64 \times 16 = 7.3728 \text{ Gbps} \quad (15)$$

### 9.2.2.2 Calculating valid JESD204B SYSREF Frequency

Valid SYSREF frequencies depend on the following parameters:

1. Sample clock frequency
2. JESD204B internal clock divider value ([CLKJESD\\_DIV](#)). This depends on the DAC JESD204B L-M-F-S mode and interpolation
3. Number of octets in a frame (F)
4. Number of frames in a multi-frame (K)

Maximum SYSREF frequency =  $(\text{Sample clock frequency}/N)$ ,

where  $N = \text{LCM}(\text{CLKJESD\_DIV}, 4 \times K \times F)$ . N is the Least common multiple of  $4 \times K \times F$  and [CLKJESD\\_DIV](#).

All valid SYSREF frequencies are integer divisors of the maximum SYSREF frequency.

**Example:**

Given sampling clock frequency = 8.84736 GSPS, Interpolation = 24, DAC Mode=L-M-F-S=8-8-2-1 and K=20:

CLKJESD\_DIV = 24 (CLKJESD\_DIV)

Maximum SYSREF Frequency = 8847.36 MHz/240 = 36.864 MHz

Valid SYSREF Frequencies = 36.864 MHz/n, where n is any positive integer.

### 9.2.3 Application Curves



Figure 144. Dual band ACPR Performance in Downlink Band 3 with On-chip PLL





Figure 145. Dual band ACPR Performance in Downlink Band 1 with On-chip PLL

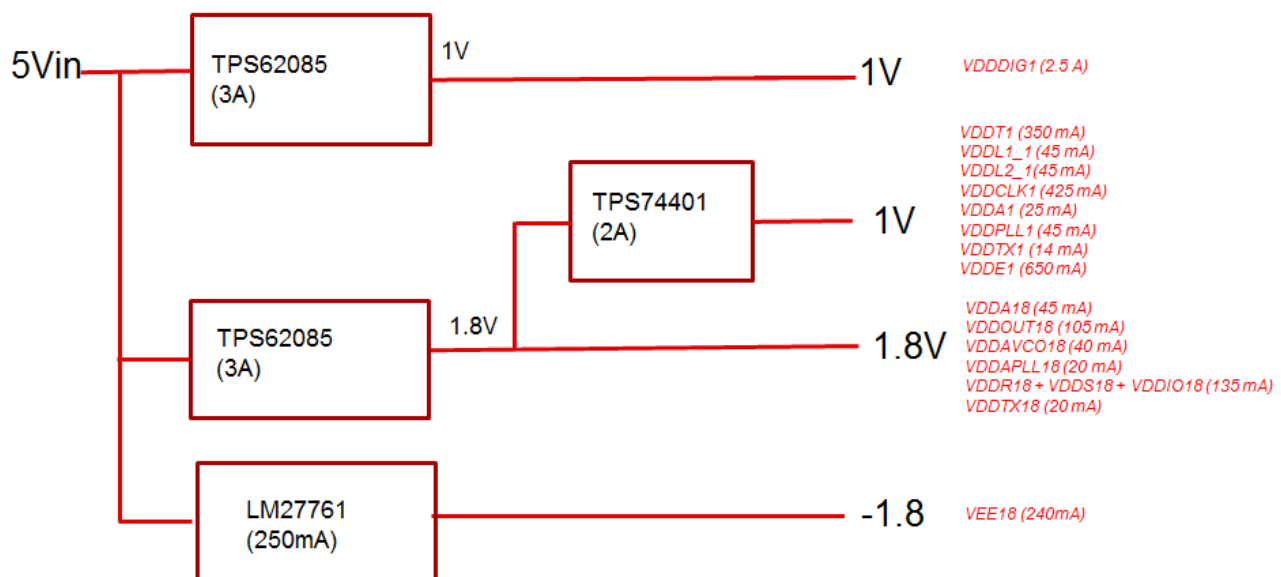
## 10 Power Supply Recommendations

Internally, DAC38RFxx comprises a digital subsystem, an analog subsystem, and a clock subsystem. Ideally, the power supply scheme should be partitioned according to these three relatively independent blocks to minimize interactions between them. Most importantly, sensitive analog and clock circuit power supply must be separated from digital switching noise to reduce direct coupling and mixing of switching spurs. Table 132 shows the power supply rails for DAC38RFxx grouped under their respective domains.

**Table 132. Power Supply Domains**

Supply rail	Nominal voltage (V)	Domain
VDDIG1	+1.0	Digital
VDDIO18	+1.8	
VDDR18	+1.8	
VDDS18	+1.8	
VDDT1	+1.0	
VDDE1	+1.0	
VDDL1_1	+1.0	
VEE18N	-1.8	Analog
VDDA1	+1.0	
VDDA18	+1.8	
VDDOUT18	+1.8	Clock
VDDPLL1	+1.0	
VDDAPLL18	+1.8	
VDDAVCO18	+1.8	
VDDCLK1	+1.0	
VDDL2_1	+1.0	
VDDTX1	+1.0	
VDDTX18	+1.8	

An example power supply scheme suitable for most applications of DAC38RFxx is shown in Figure 146. It is recommended to use ferrite beads (FB) to isolate the individual rails from each other.



**Figure 146. Power Supply Scheme for DAC38RFxx**

## 10.1 Power Supply Sequencing

There are no power supply sequencing requirements for all the 1-V and 1.8-V power supplies. For the -1.8 V VEE18 rail, it is recommended that this supply is the last to be enabled. Enabling VEE18 (while other supply voltages are disabled) can cause a small negative voltage to be present at the other rails (that is, VDDA1 and VDDD1G1). This small negative voltage can interfere with the startup of some DC-DC converters or LDO's connected to the 1 V and 1.8 V input power rails.

## 11 Layout

### 11.1 Layout Guidelines

- DAC RF output traces
  - Single-ended 50  $\Omega$  co-planar wave guide for output traces is recommended.
  - Use short RF traces. Place DAC close to edge of PCB to shorten the length of output and clock traces. This helps to minimize PCB loss and coupling
  - Avoid width/spacing differences when entering a landing pad (eg. a balun) by tapering or by redefining width/space rules for the traces
- Power supply planes
  - Ensure sufficient lateral spacing between two power planes (about 3x the thickness of the plane is recommended)
  - Insert ground plane between adjacent power planes where possible

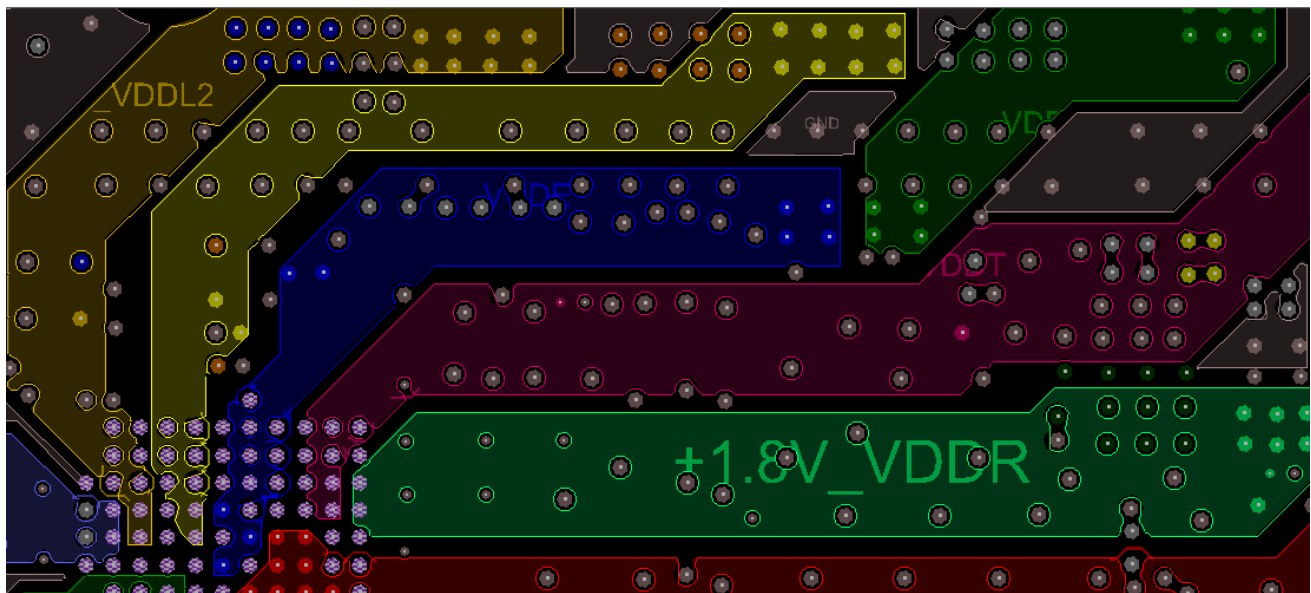
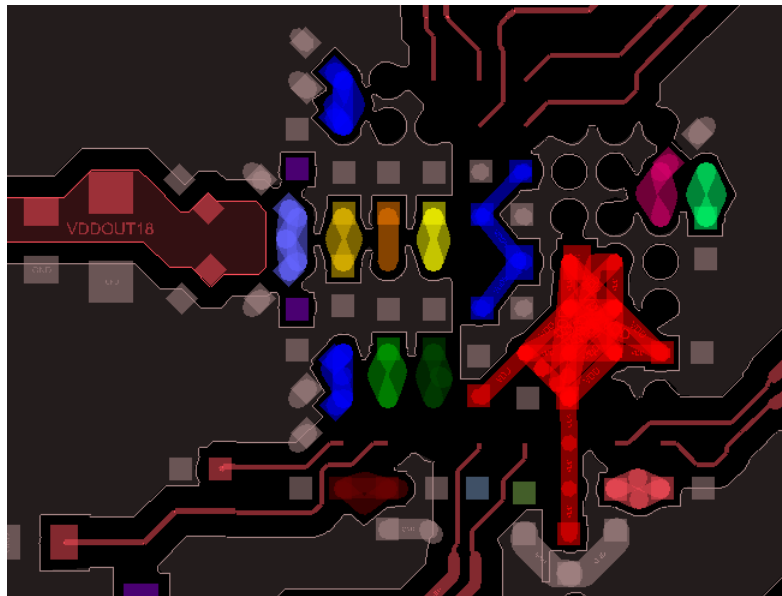


Figure 147. Example Power Plane Routing

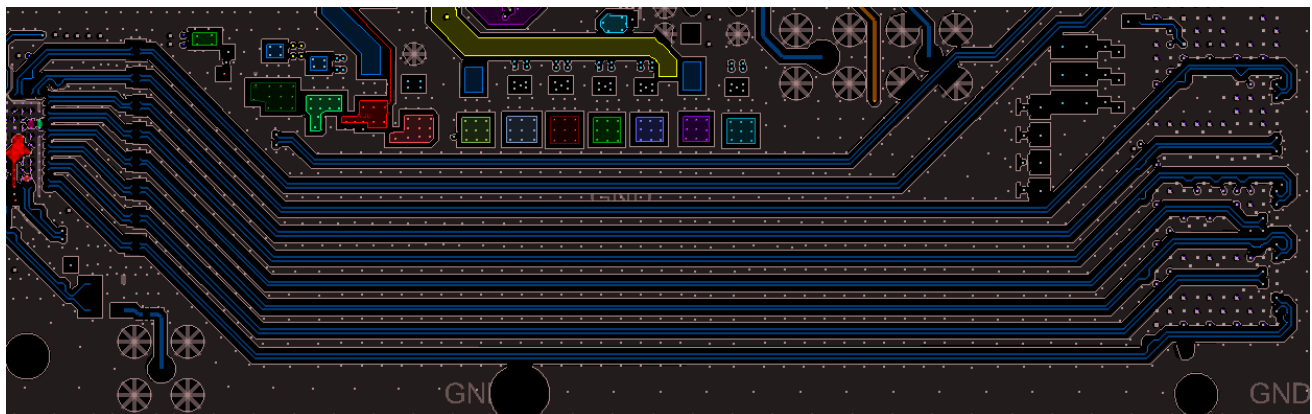
- Bypass Capacitors
  - Use bypass capacitors with in-pad vias and place between the pin and the power plane. Avoid sharing ground vias or pads of bypass caps used for different power rails
  - Minimize stubs on bypass capacitors to avoid parasitic inductance

## Layout Guidelines (continued)



**Figure 148. Bypass Capacitors Placed on the Power Supply Pin with In-pad Vias**

- High speed serdes traces
  - Route all serdes traces straight and minimized sharp curves or serpentines. Route for best signal integrity
  - Some skew between serdes traces can be tolerated. It is recommended to limit skew between traces to 320ps or less
  - Place ground planes between the serdes traces for improved isolation



**Figure 149. Layout Example of High Speed Serdes Traces**

## 11.2 Layout Example

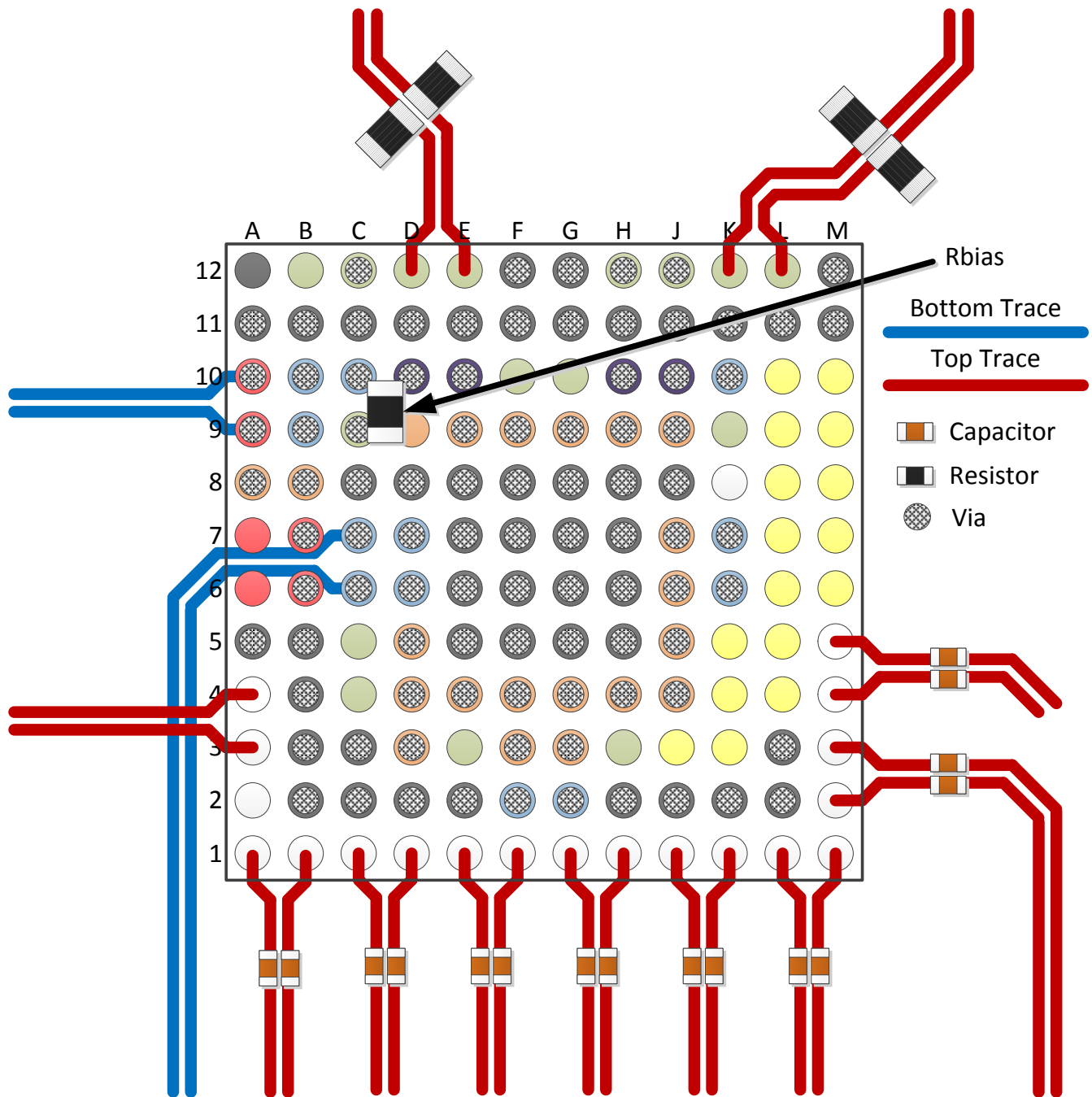


Figure 150. Layout Example of DAC38RFxx

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 133. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC38RF86	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
DAC38RF87	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
DAC38RF96	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
DAC38RF87	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC38RF86IAAV	PREVIEW	FCBGA	AAV	144	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF86I	
DAC38RF86IAAVR	PREVIEW	FCBGA	AAV	144	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF86I	
DAC38RF87IAAV	PREVIEW	FCBGA	AAV	144	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF87I	
DAC38RF87IAAVR	PREVIEW	FCBGA	AAV	144	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF87I	
DAC38RF96IAAV	PREVIEW	FCBGA	AAV	144	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF96I	
DAC38RF96IAAVR	PREVIEW	FCBGA	AAV	144	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF96I	
DAC38RF97IAAV	PREVIEW	FCBGA	AAV	144	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF97I	
DAC38RF97IAAVR	PREVIEW	FCBGA	AAV	144	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF97I	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



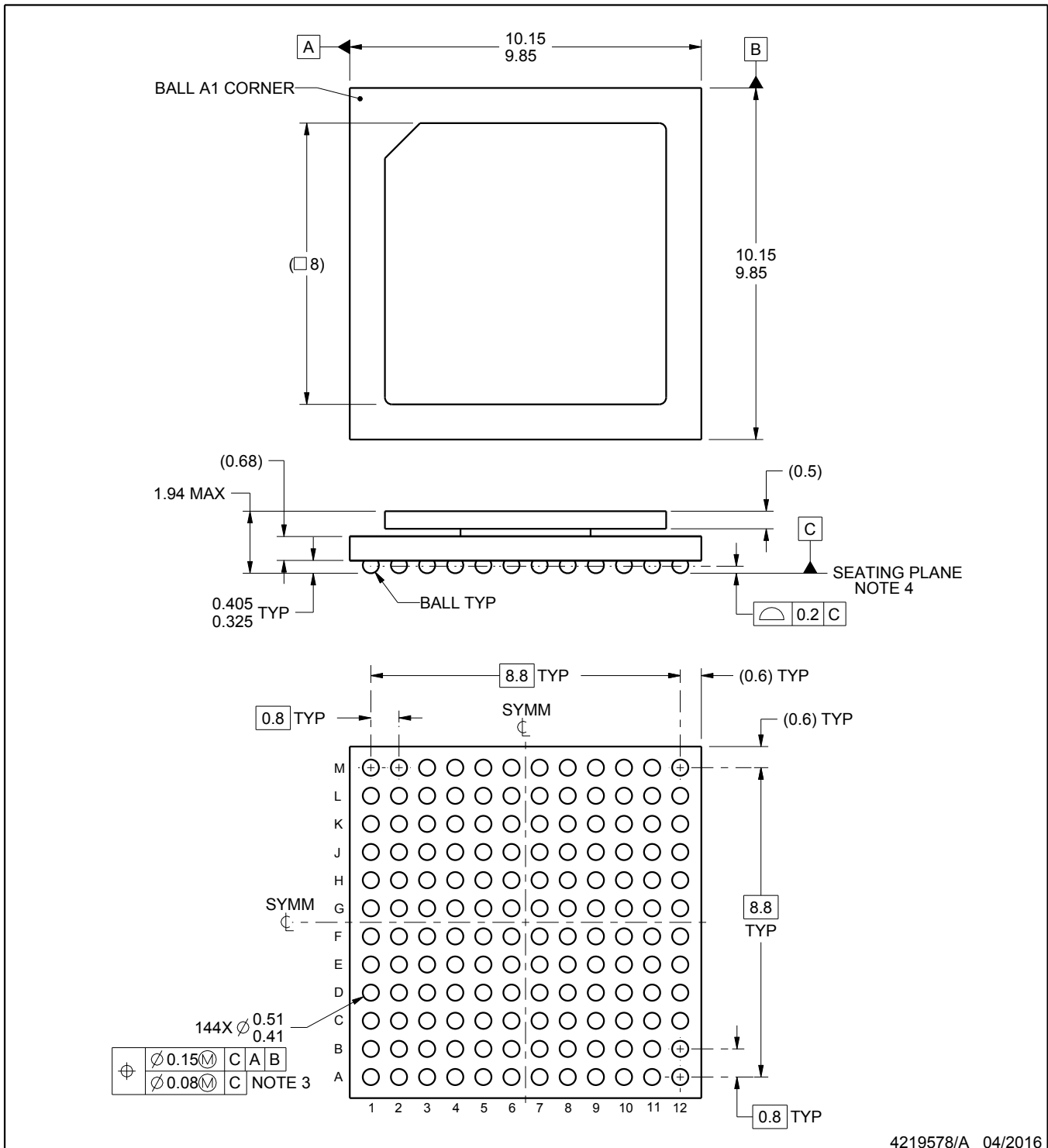
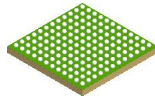
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



4219578/A 04/2016

NOTES:

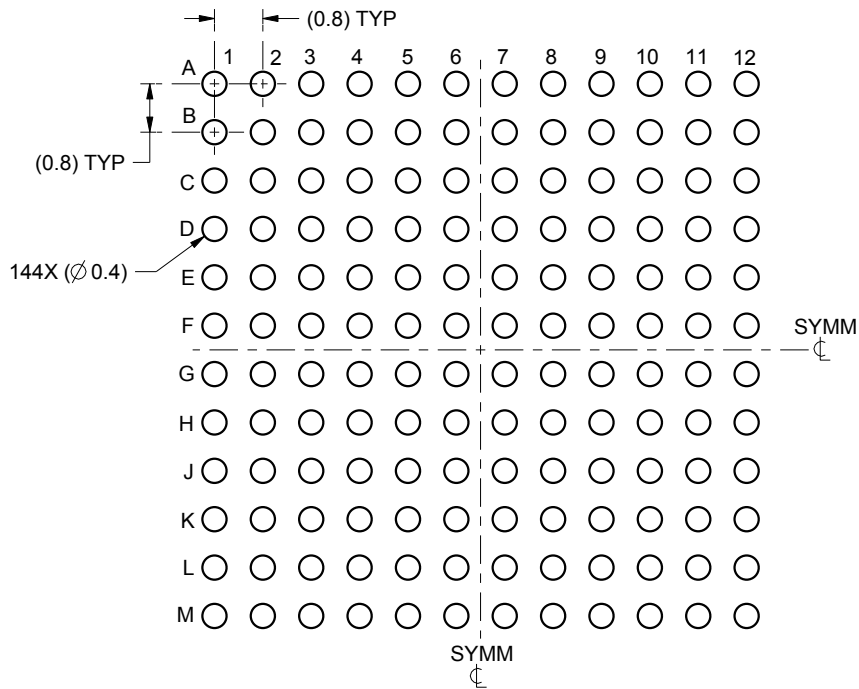
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

# EXAMPLE BOARD LAYOUT

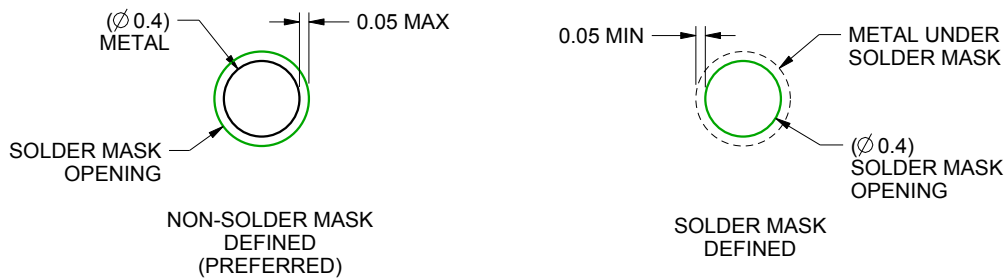
AAV0144A

FCBGA - 1.94 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS  
NOT TO SCALE

4219578/A 04/2016

NOTES: (continued)

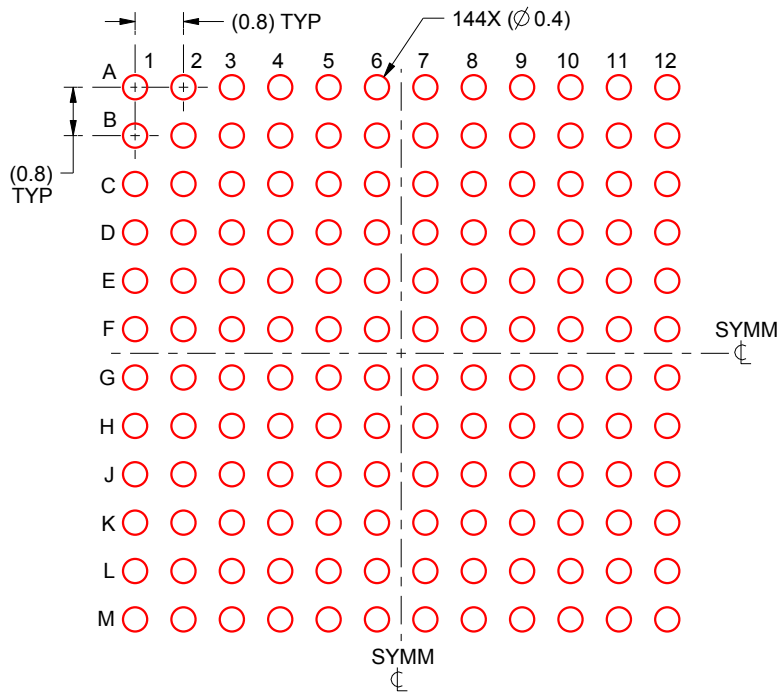
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

AAV0144A

FCBGA - 1.94 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:8X

4219578/A 04/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2017, Texas Instruments Incorporated