19-1189; Rev 0; 3/97

EVALUATION KIT AVAILABLE

MAXIM

10-Bit, 20Msps, TTL-Output ADC

General Description

The MAX1160 10-bit, monolithic analog-to-digital converter (ADC) is capable of 20Msps minimum word rates. An on-board track/hold ensures excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes drive requirement problems.

Inputs and outputs are TTL compatible. An overrange output is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is low at only 1W with +5V and -5.2V power-supply voltages. The MAX1160 also accepts wide ±2V input voltages.

The MAX1160 is available in 28-pin DIP and SO packages in the commercial temperature range.

Applications

Medical Imaging
Professional Video
Radar Receivers
Instrumentation
Digital Communications

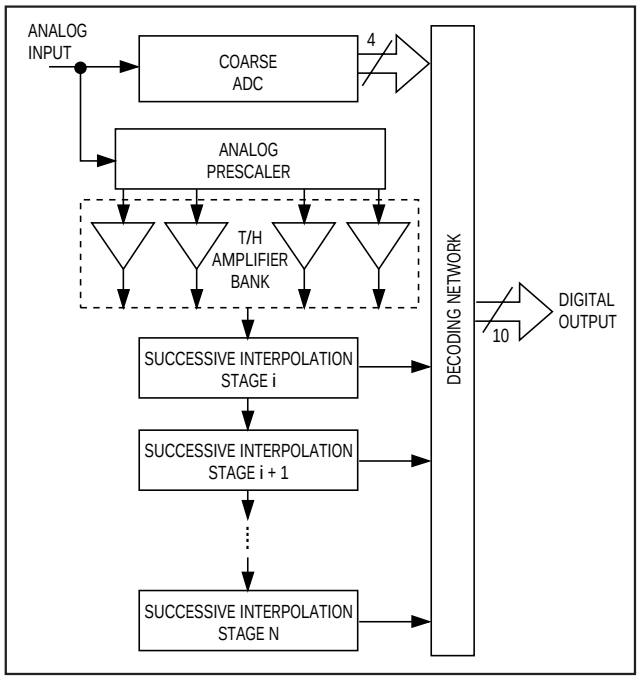
Features

- **Monolithic 20Msps Converter**
- **On-Chip Track/Hold**
- **Bipolar, ±2V Analog Input**
- **60dB SNR at 1MHz Input**
- **5pF Input Capacitance**
- **TTL Outputs**

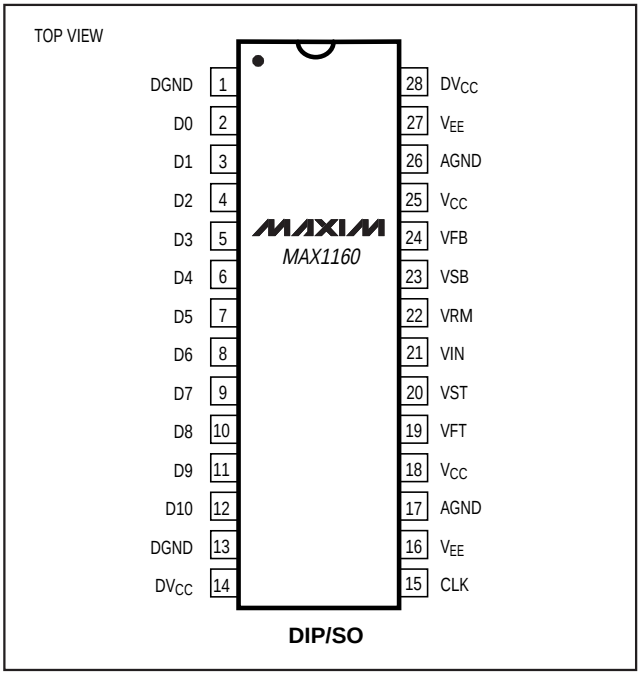
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1160ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160ACWI	0°C to +70°C	28 SO
MAX1160BCWI	0°C to +70°C	28 SO

Functional Diagram



Pin Configuration



DIP/SO

ABSOLUTE MAXIMUM RATINGS

V_{CC} 6V
V_{EE} .....-6V
Analog Input .....VFB ≤ VIN ≤ VFT
VFT, VFB .....3V, -3V
Reference-Ladder Current.....12mA
CLK Input.....V_{CC}
Digital Outputs.....30mA to -30mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP 1.14W
SO 1W
Operating Temperature Range.....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec). .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1160A			MAX1160B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			10			10			Bits
DC ACCURACY (± full scale, 250kHz sample rate, T_A = +25°C)									
Integral Nonlinearity		I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN} = 0V	VI		30	60		30	60	µA
Input Bias Current	T_A = -55°C to +125°C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	T_A = -55°C to +125°C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3dB small signal	V		120			120		MHz
Positive Full-Scale Error		V		±2.0			±2.0		LSB
Negative Full-Scale Error		V		±2.0			±2.0		LSB
REFERENCE INPUT									
Reference-Ladder Resistance		VI	500	800		500	800		Ω
Reference-Ladder Tempco		V		0.8			0.8		Ω/°C
TIMING CHARACTERISTICS									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1			1		ns
Aperture Jitter Time	T_A = +25°C	V		5			5		ps-RMS
Acquisition Time	T_A = +25°C	V		20			20		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MAX1160A MIN	MAX1160A TYP	MAX1160A MAX	MAX1160B MIN	MAX1160B TYP	MAX1160B MAX	UNITS
DYNAMIC PERFORMANCE										
Effective Number of Bits (ENOB)	f_{IN} = 1MHz				9.2			8.7		Bits
	f_{IN} = 3.58MHz				8.8			8.3		
	f_{IN} = 10MHz				7.5			7.0		
Signal-to-Noise Ratio (without harmonics) (SNR)	f_{IN} = 1MHz	T_A = +25°C	I	57	60		54	57		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	55	58		52	55		
	f_{IN} = 3.58MHz	T_A = +25°C	I	56	58		53	55		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	54	56		51	53		
	f_{IN} = 10MHz	T_A = +25°C	I	50	53		47	49		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	47	50		44	46		
Total Harmonic Distortion (THD)	f_{IN} = 1MHz	T_A = +25°C	I	57	60		54	57		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	54	57		51	54		
	f_{IN} = 3.58MHz	T_A = +25°C	I	56	58		53	55		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	53	55		50	52		
	f_{IN} = 10MHz	T_A = +25°C	I	46	48		43	45		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	45	47		42	44		
Signal-to-Noise and Distortion Ratio (SINAD)	f_{IN} = 1MHz	T_A = +25°C	I	55	57		52	54		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	52			49			
	f_{IN} = 3.58MHz	T_A = +25°C	I	54	55		51	52		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	51			48			
	f_{IN} = 10MHz	T_A = +25°C	I	44	47		41	44		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	43			40			
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1MHz	T_A = +25°C	V		67			67		dB
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz	T_A = +25°C	V		0.2			0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz	T_A = +25°C	V		0.5			0.7		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1160A MIN	MAX1160A TYP	MAX1160A MAX	MAX1160B MIN	MAX1160B TYP	MAX1160B MAX	UNITS
DIGITAL INPUTS									
Logic 1 Voltage		V	2.4		4.5	2.4		4.0	V
Logic 0 Voltage		V			0.8			0.8	V
Maximum Input Current Low	T_A = +25°C	IV	0	5	20	0	5	20	µA
Maximum Input Current High	T_A = +25°C	IV	0	5	20	0	5	20	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
DIGITAL OUTPUTS									
Logic 1 Voltage		IV	2.4			2.4			V
Logic 0 Voltage		IV			0.6			0.6	V
POWER-SUPPLY REQUIREMENTS									
Voltages	V_{CC}	IV	4.75		5.25	4.75		5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	
Currents	I_{CC}	VI		118	145		118	145	mA
	DI_{CC}	VI		40	55		40	55	
	$-I_{EE}$	VI		40	57		40	57	
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power-Supply Rejection	V_{CC} = 5V ±0.25V, V_{EE} = -5.2V ±0.25V	V		1.0			1.0		LSB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

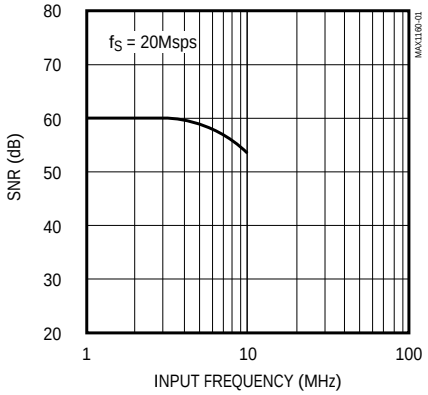
PIN	NAME	FUNCTION
1, 13	DGND	Digital Ground
2	D0	TTL Output (LSB)
3–10	D1–D8	TTL Outputs
11	D9	TTL Output (MSB)
12	D10	TTL Output Overrange
14, 28	DV_{CC}	+5V Supply (digital)
15	CLK	Clock
16, 27	V_{EE}	-5.2V Supply (analog)

PIN	NAME	FUNCTION
17, 26	AGND	Analog Ground
18, 25	V_{CC}	+5V Supply (analog)
19	VFT	Force for Top of Reference Ladder
20	VST	Sense for Top of Reference Ladder
21	VIN	Analog Input
22	VRM	Middle of Voltage Reference Ladder
23	VSB	Sense for Bottom of Reference Ladder
24	VFB	Force for Bottom of Reference Ladder

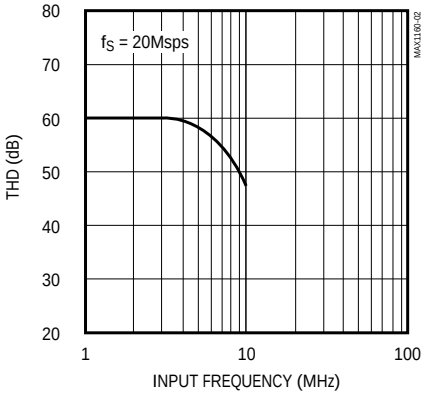
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

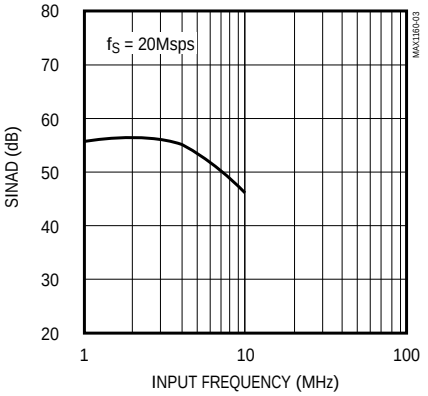
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



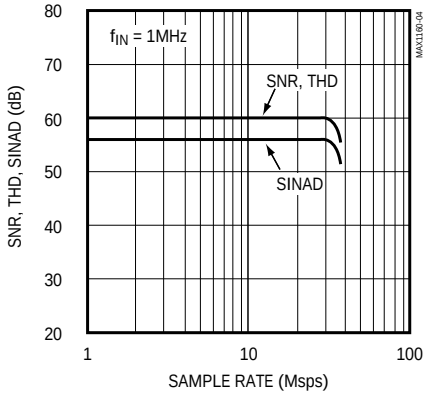
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



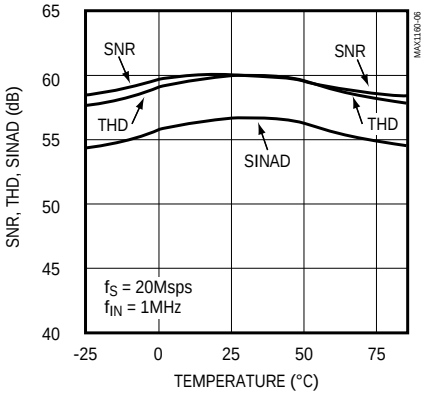
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



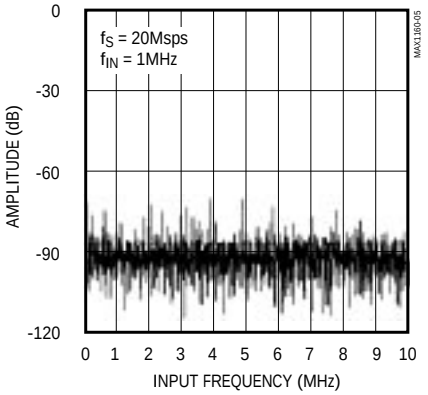
SNR, THD, SINAD vs. SAMPLE RATE



SNR, THD, SINAD vs. TEMPERATURE



SPECTRAL RESPONSE



Detailed Description

The MAX1160 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1160 in normal circuit operation. The following section provides a description of the pin functions, and outlines critical performance criteria to consider for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1160 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. Connect these beads as close to the device as possible. The connection between the beads and the MAX1160 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are recommended).

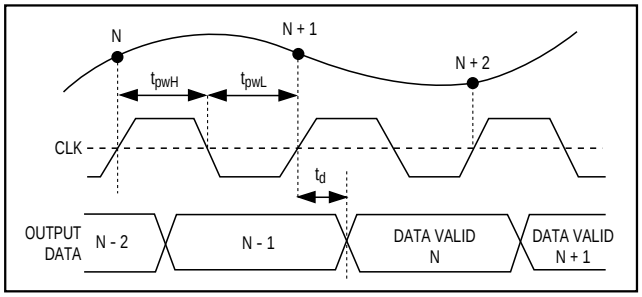


Figure 1a. Timing Diagram

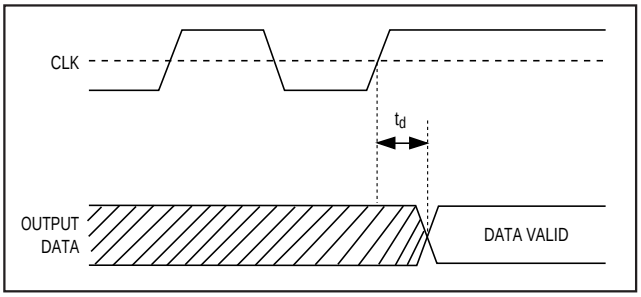


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Propagation Delay		14	18	ns
t_{pwH}	CLK High Pulse Width	20		300	ns
t_{pwL}	CLK Low Pulse Width	20			ns

The MAX1160 has two grounds: AGND and DGND. These internal grounds are isolated on the device. Use ground planes for optimum device performance. Use DGND for the DV_{CC} return path (typically 40mA) and for the return path for all digital output logic interfaces. Separate AGND and DGND from each other, connecting them together only through a ferrite bead at the device.

Connect a Schottky or hot carrier diode between AGND and V_{EE}. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply-sequencing latchup conditions. For optimum performance, use the recommended circuit shown in Figure 2.

Voltage Reference

The MAX1160 requires the use of two voltage references: VFT and VFB. VFT is the force for the top of the voltage-reference ladder (typically +2.5V); VFB (typically -2.5V) is the force for the bottom of the voltage-reference ladder. Both voltages are applied across an 800Ω internal reference-ladder resistance. The +2.5V voltage source for reference VFT must be current limited to 20mA (max) if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3. In addition, there are three reference-ladder taps (VST, VRM, and VSB). VST is the sense for the top of the reference ladder (+2V), VRM is the midpoint of the ladder (typically 0V), and VSB is the sense for the bottom of the reference ladder (-2V). The voltages at VST and VSB are the device's true full-scale input voltages when VFT and VFB are driven to the recommended voltages (typically +2.5V and -2.5V, respectively). These points should be used to monitor the device's actual full-scale input range. When not being used, a decoupling capacitor of 0.01µF (chip capacitor preferred) connected to AGND from each tap is recommended to minimize high-frequency noise injection.

Figure 2 shows an example of a recommended reference-driver circuit. IC1 is a MAX6225, a 2.5V reference with an accuracy of 0.2%. The 10kΩ potentiometer R1 supports a minimum adjustable range of 0.6%. Use an OP07 or equivalent device for IC2. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain 0.3LSB matching between VFT and VFB. If 0.1% matching is not met, then R4 can be used to adjust the VFB voltage to the desired level. Adjust VFT and VFB such that VST and VSB are exactly +2V and -2V, respectively.

The analog input range scales proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of VFT and VFB. However, because the device is laser trimmed to optimize performance with ±2.5V references, its accuracy degrades if operated beyond a ±2% range.

The following errors are defined:

+FS error = top of ladder offset voltage
= Δ(+FS - VST + 1LSB)

-FS error = bottom of ladder offset voltage
= Δ(-FS - VSB - 1LSB)

where the +FS (full-scale) input voltage is defined as the output transition between 11 1111 1110 and 11 1111 1111, and the -FS input voltage is defined as the output transition between 00 0000 0000 and 00 0000 0001 (Table 2).

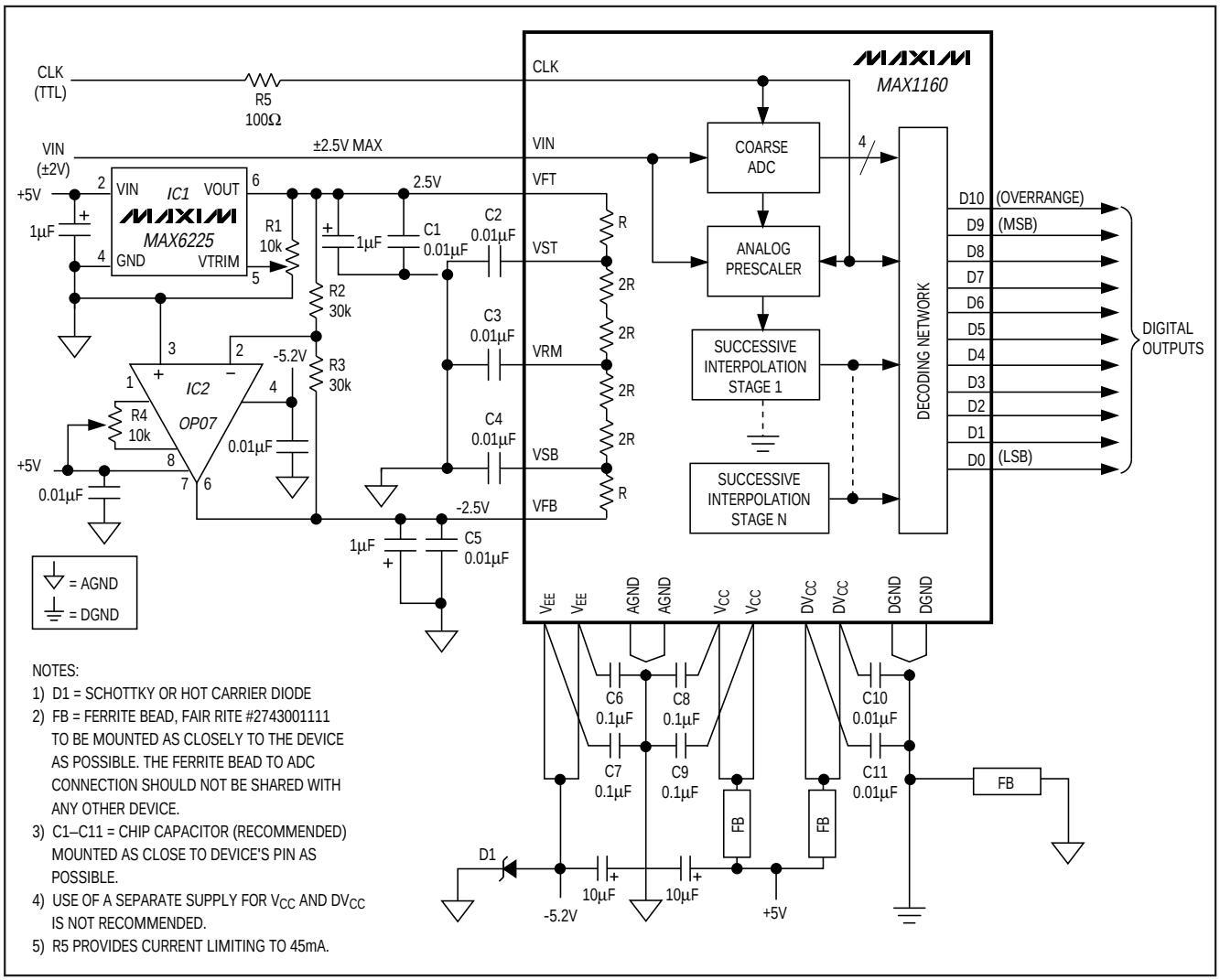
Analog Input

VIN is the analog input. The full-scale input range will be 80% of the reference voltage, or ±2V with VFB = -2.5V and VFT = +2.5V.

The analog input's drive requirements are minimal when compared to conventional flash converters. This is due to the MAX1160's extremely low (5pF) input capacitance and very high (300kΩ) input resistance. For example, for an input signal of ±2Vp-p with a 10MHz input frequency, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1160 is driven from a single-ended TTL input (CLK). The CLK pulse width (t_{pwH}) must be kept between 20ns and 300ns to ensure proper operation of the internal track/hold amplifier (Figure 1a). When operating the MAX1160 at sampling rates above 3Msps, it is recommended that the clock input duty cycle be kept at



NOTES:
1) D1 = SCHOTTKY OR HOT CARRIER DIODE
2) FB = FERRITE BEAD, FAIR RITE #2743001111 TO BE MOUNTED AS CLOSELY TO THE DEVICE AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.
3) C1–C11 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSE TO DEVICE'S PIN AS POSSIBLE.
4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED.
5) R5 PROVIDES CURRENT LIMITING TO 45mA.

Figure 2. Typical Operating Circuit

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2V + 1/2LSB	1	11 1111 1111
+2V - 1LSB	0	11 1111 111Ø
0V	0	ØØ ØØØØ ØØØØ
-2V + 1LSB	0	00 0000 000Ø
< 2V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1.)

50% to optimize performance, but performance will not be degraded if kept within the 40% to 60% range. The analog input signal is latched on the rising edge of CLK.

The clock input must be driven from fast TTL logic (VIH ≤ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω resistor (R5) in series to limit current to approximately 45mA.

Digital Outputs

The format of the output data (D0–D9) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one-clock-cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise and fall times are not symmetrical. Typical propagation delay is 14ns for the rise time and 6ns for the fall time (Figure 4). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Overrange Output

The overrange output (D10) is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0–D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the MAX1160 in higher-resolution systems.

Evaluation Board

The MAX1160 EV kit is available to help designers demonstrate the MAX1160's full performance. This board includes a reference circuit, a clock-driver circuit, output data latches, and an on-board reconstruction of the digital data. A separate data sheet describing the operation of this board is also available. Contact the factory for price and availability.

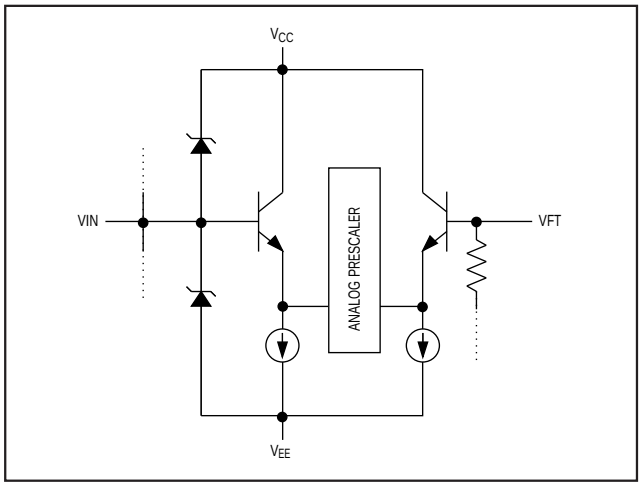


Figure 3. Analog Equivalent Input Circuit

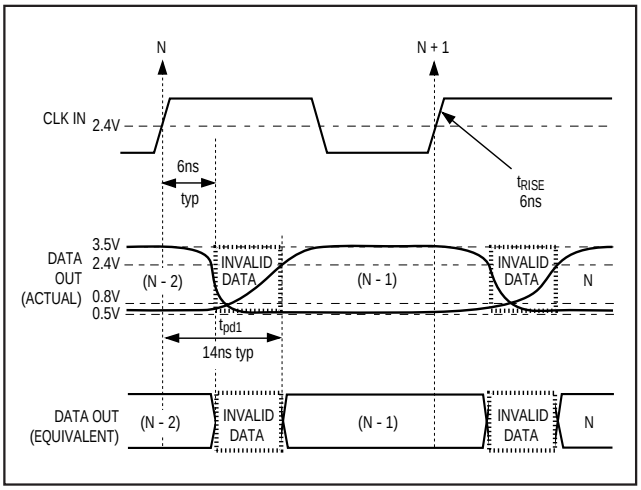


Figure 4. Digital Output Characteristics