NCV78713

High Efficiency Buck Single LED Driver with Integrated Current Sensing for Automotive Front Lighting

The NCV78713 is a single-chip and high efficient Buck Single LED Driver designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78713 is in particular designed for high current LEDs and provides a complete solution to drive 1 LED string of up-to 60 V. It includes 1 current regulator for the LED string and required diagnostic features for automotive front lighting with a minimum of external components – the chip doesn't need any external sense resistor for the buck current regulation. The available output current and voltage can be customized for the LED string. When more than 1 LED channel is required on 1 module, the NCV78713 can be combined with NCV78723 devices, incorporating Buck Dual LED Driver. Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

Features

- Single Chip
- Buck Topology
- 1 LED String up-to 60 V
- High Current Capability up to 1.6 A DC
- High Overall Efficiency
- Minimum of External Components
- Integrated High Accuracy Current Sensing
- Integrated Switched Mode Buck Current Regulator
- Average Current Regulation through the LEDs
- High Operating Frequencies to Reduce Inductor Sizes
- Low EMC Emission for LED Switching and Dimming
- SPI Interface for Dynamic Control of System Parameters
- Fail Safe Operating (FSO) Mode, Stand-Alone Mode

Typical Applications

- High Beam
- Low Beam
- DRL
- Position or Park Light
- Turn Indicator
- Fog
- Static Cornering

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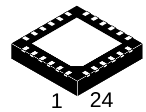
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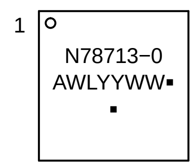
QFN24
CASE 485CS

MARKING DIAGRAM



N78713 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

TYPICAL APPLICATION SCHEMATIC

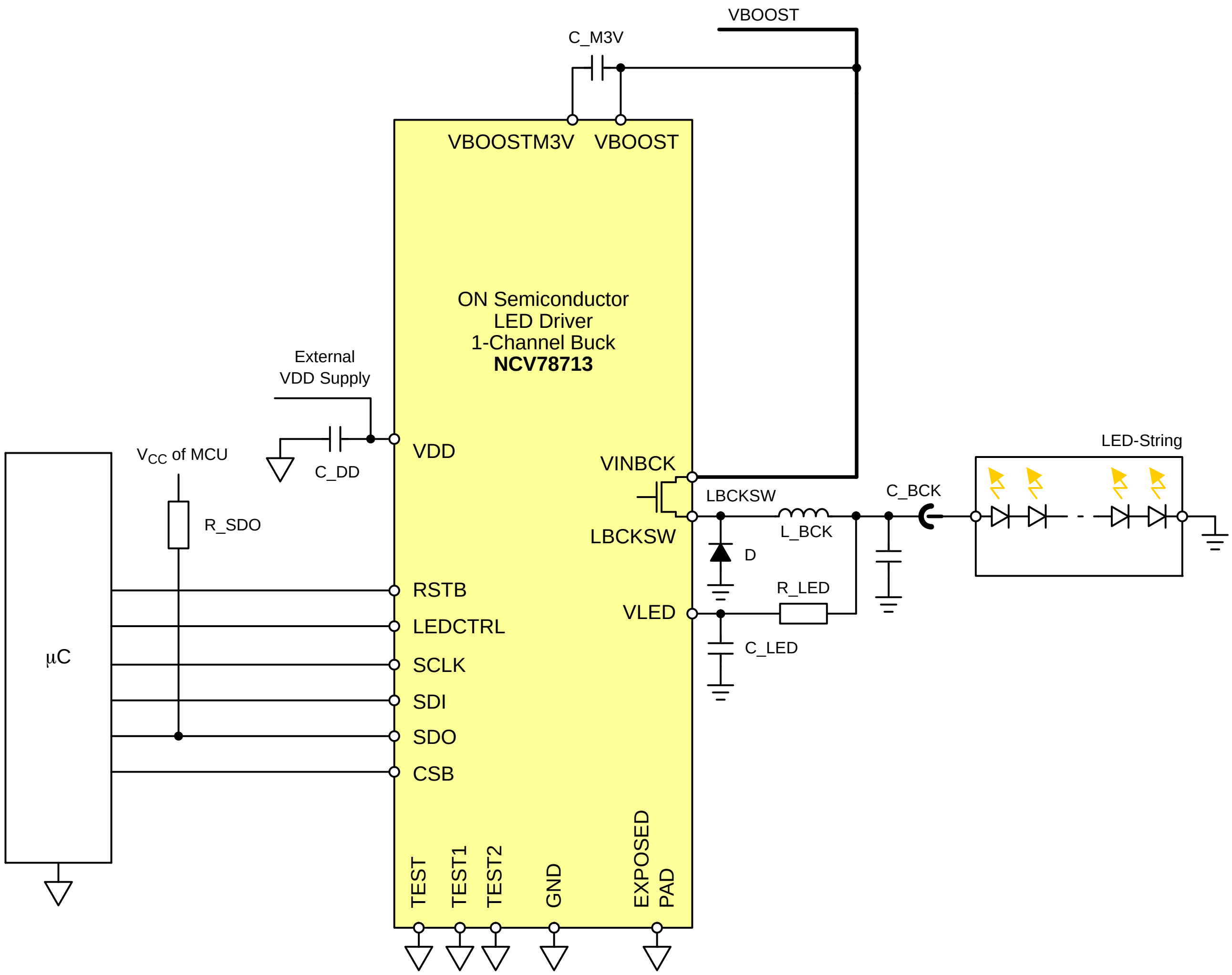


Figure 1. Typical Application Schematic

Table 1. PIN DESCRIPTION

Component	Function	Typical Value	Unit
L_BCK	Buck Regulator Coil (see Buck Regulator Chapter for Details)	47	µH
C_BCK	Buck Regulator Output Capacitor (see Buck Regulator Chapter for Details)	220	nF
C_M3V	Capacitor for M3V Regulator	(see Table 6 − VBOOSTM3V)	nF
C_DD	V_{DD} Decoupling Capacitor	470	nF
C_LED	Optional VLED Pin Filter Capacitor (Note 2)	1	nF
R_LED	VLED Pin Serial Resistor (Notes 2 and 3)	Min. 1	kΩ
R_SDO	SPI Pull-Up Resistor	1	kΩ
D	Buck Regulator Free-Wheeling Diode	e.g. MBRS2H100T3G	

1. Pin TEST has to be connected to ground. TEST1 and TEST2 pins can be connected to ground or left floating.
2. C_LED is optional. If used, time constant of the C_LED and R_LED filter has to be lower than minimal LEDCTRL ON time in PWM dimming for proper VLED measurement.
3. R_LED is necessary to ensure Absolute Maximum Ratings of IVLED current (see Table 3).

BLOCK DIAGRAM

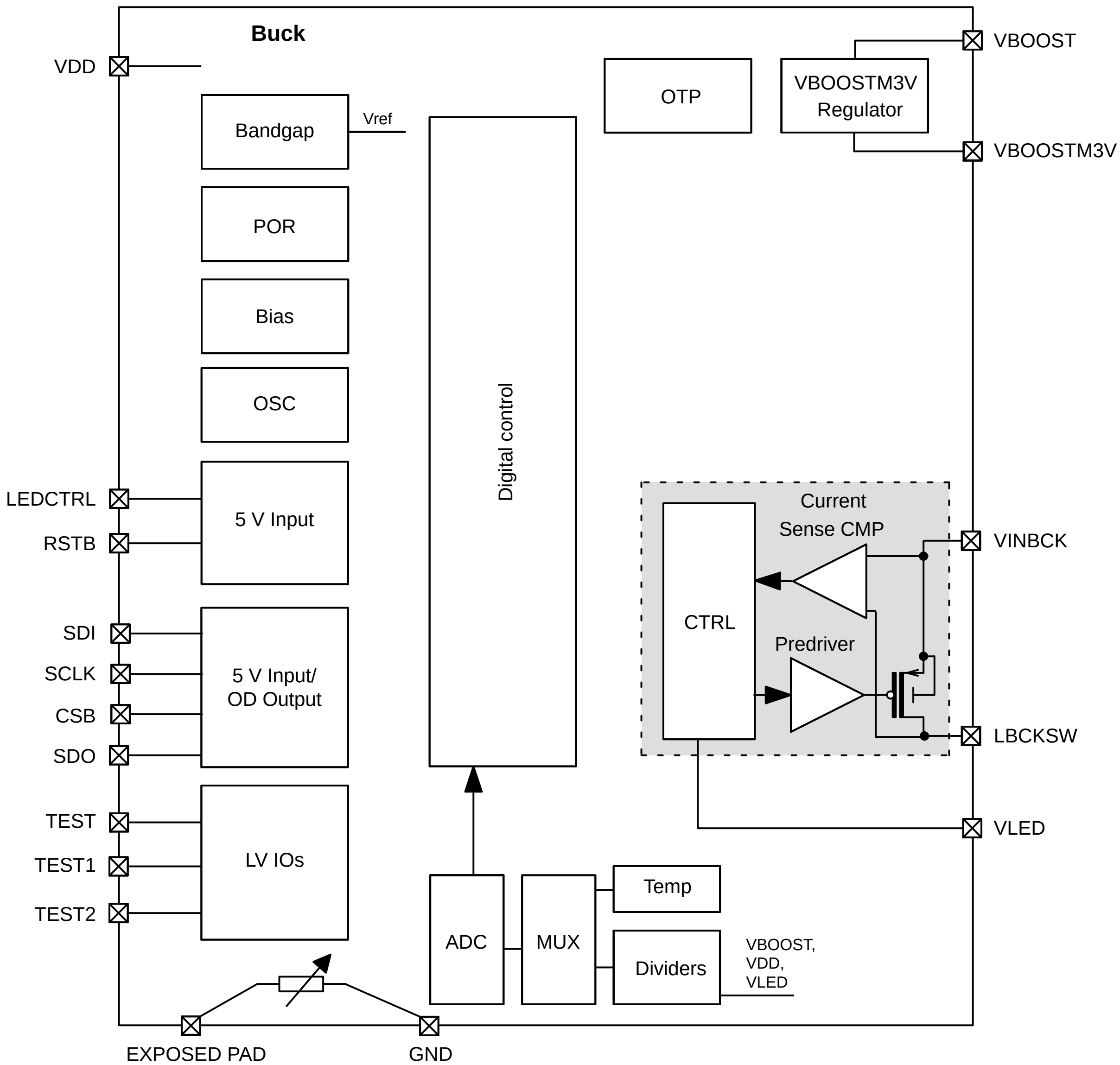


Figure 2. Block Diagram

ESD SCHEMATIC

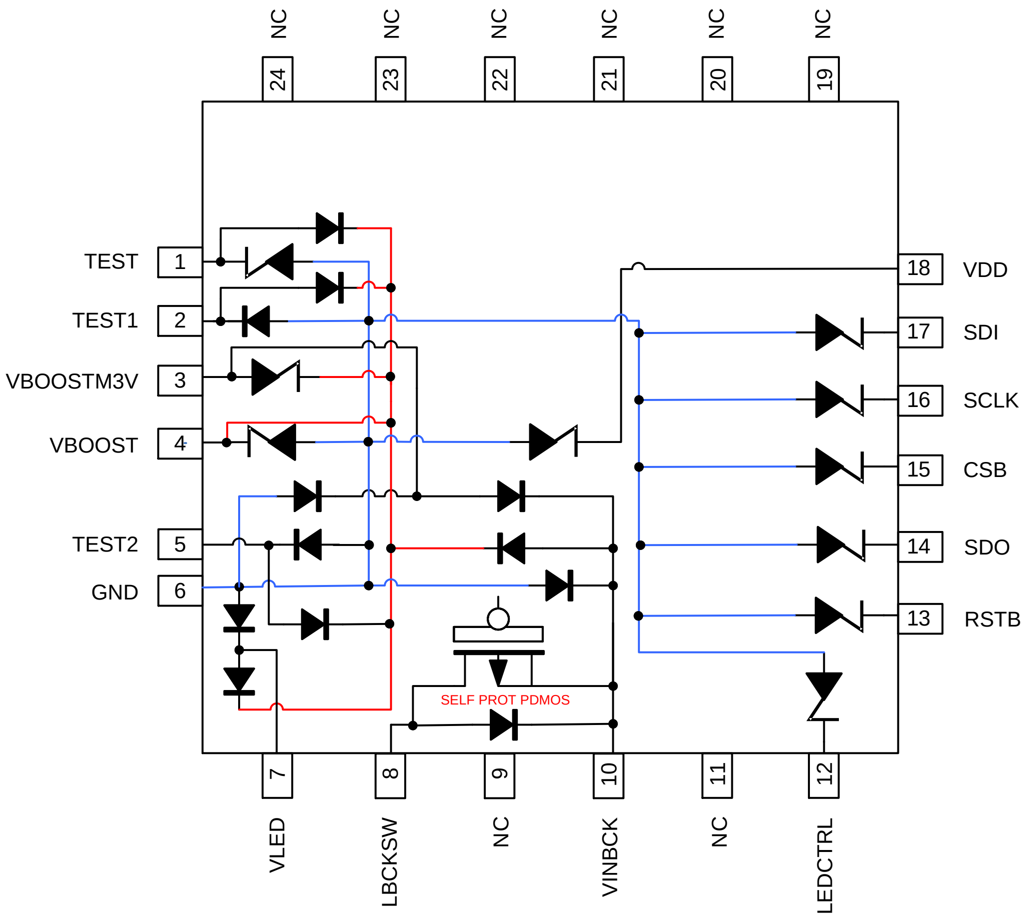


Figure 3. ESD Schematic

PACKAGE AND PIN DESCRIPTION

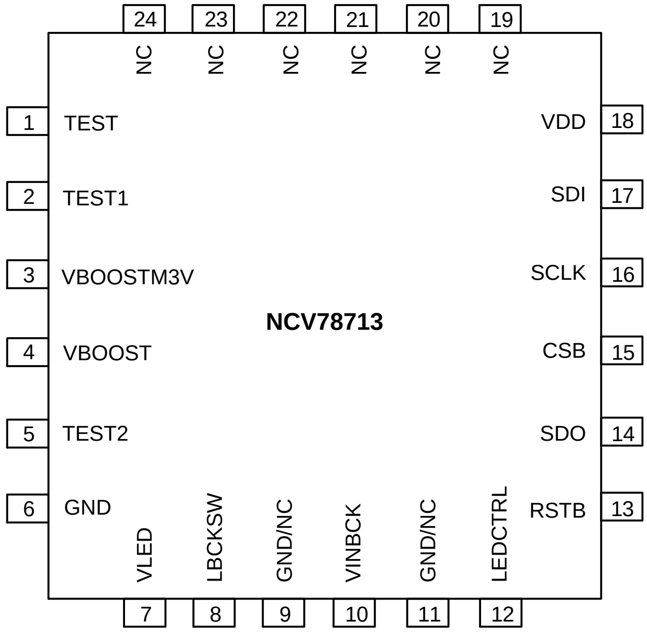


Figure 4. Pin Connections

Table 2. PIN DESCRIPTION

Pin No.	Pin Name	Description	I/O Type
1	TEST	Test Pin	LV In
2	TEST1	Test Pin	LV IN/OUT HV Tolerant
3	VBOOSTM3V	VBOOSTM3V Regulator Output Pin	HV OUT (Supply)
4	VBOOST	Booster Input Voltage Pin	HV Supply
5	TEST2	Test Pin	LV IN/OUT HV Tolerant
6	GND	Ground	Ground
7	VLED	LED String Forward Voltage Sense Input	HV IN
8	LBCKSW	Buck Switch Output	HV OUT
9, 11	GND/NC	GND/NC Connection in Application	NC
10	VINBCK	Buck High Voltage Supply	HV Supply
12	LEDCTRL	LED String Enable	MV IN
13	RSTB	External Reset Signal	MV IN
14	SDO	SPI Data Output	MV Open-Drain
15	CSB	SPI Chip Select (Chip Select Bar)	MV IN
16	SCLK	SPI Clock	MV IN
17	SDI	SPI Data Input	MV IN
18	VDD	3 V Logic Supply	LV Supply
19, 20, 21, 22, 23, 24	NC	GND/NC Connection in the Application	NC

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Minimum	Maximum	Unit
VBOOST Supply Voltage	V_{BOOST}	−0.3	+68	V
VINBCK Supply Voltage (Note 4)	VINBCK	Max of VBOOSTM3V − 0.3, −0.3	Min of V_{BOOST} + 0.3, 68	V
VBOOSTM3V Supply Voltage (Note 5)	VBOOSTM3V	Max of V_{BOOST} − 3.6, −0.3	Min of V_{BOOST} + 0.3, 68	V
VLED Sense Voltage	VLED	−0.3	Min of V_{BOOST} + 0.3, 68	V
Logic Supply Voltage (Note 6)	V_{DD}	−0.3	3.6	V
Medium Voltage IO Pins (Note 7)	IOMV	−0.3	7.0	V
Test Pins (Note 8)	TESTx	−0.3	Min of V_{BOOST} + 0.3, 68	V
Buck Switch Low Side (Note 4)	LBCKSW	−2.0	VINBCK + 0.3	V
VLED Sink/Source Current	IVLED	−30	30	mA
Storage Temperature (Note 9)	T_{STRG}	−50	150	°C
The Exposed Pad (Note 10)	EXPAD	GND − 0.3	GND + 0.3	V
Electrostatic Discharge on Component Level (Note 11) Human Body Model Charge Device Model	 V_{ESD_HBM} V_{ESD_CDM}	 −2 −500	 +2 +500	 kV V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. V(VINBCK − LBCKSW) < 70 V, the driver in off state.
5. The VBOOSTM3V regulator in off state.
6. Absolute maximum rating for pins: VDD, TEST. Also valid for relative difference V_{BOOST} − VBOOSTM3V.
7. Absolute maximum rating for pins: SCLK, CSB, SDI, SDO, LEDCTRL, RSTB. The μC interface pins (the IOMV pins) accept 5 V while the device is in the power-off mode (V_{DD} = 0 V).
8. Absolute maximum rating for pins: TEST1, TEST2.
9. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.
10. The exposed pad must be hard wired to GND pin in an application to ensure both electrical and thermal connection.
11. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
    ESD Charge Device Model tested per EIA/JESD22−C101
    Latch-up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 12) is a substantial part of the operation conditions; hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 4. RECOMMENDED OPERATING RANGES

Characteristic	Symbol	Min	Typ	Max	Unit
Boost Supply Voltage	V_{BOOST}	+8		+67	V
VINBCK Supply Voltage (Note 13)	VINBCK	V_{BOOST} − 0.1	V_{BOOST}	V_{BOOST} + 0.1	V
Low Voltage Supply	V_{DD}	3.05	3.3	3.6	V
Buck Switch Output Current	I_LBCKSW			1.9	A
Functional Operating Junction Temperature Range (Note 14)	T_{JF}	−40		155	°C
Parametric Operating Junction Temperature Range (Note 15)	T_{JP}	−40		150	°C
The Exposed Pad Connection (Note 16)	EXPOSED_PAD	GND − 0.1	GND	GND + 0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

12. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc. No more than 100 cumulated hours in life time above T_{TW}.
13. Hard connection of VINBCK to VBOOST on PCB.
14. The circuit functionality is not guaranteed outside the functional operating junction temperature range. Also please note that the device is verified on bench for operation up to 170°C but that the production test guarantees 155°C only.
15. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.
16. The exposed pad must be hard wired to GND pin in an application to ensure both electrical and thermal connection.

Table 5. THERMAL RESISTANCE

Characteristic	Package	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Exposed Pad (Note 17)	QFN24 5x5	R_{thjp}	−	5	−	°C/W

17. Includes also typical solder thickness under the Exposed Pad (EP).

Table 6. ELECTRICAL CHARACTERISTICS
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
VDD: 3 V LOW VOLTAGE ANALOG AND DIGITAL SUPPLY						
The VDD Current Consumption	I_VDD		−	−	6	mA
POR Toggle Level on VDD Rising	POR_{3V_H}		2.7	−	3.05	V
POR Toggle Level on VDD Falling	POR_{3V_L}		2.45	−	2.8	V
POR Hysteresis	POR_{3V_HYST}		0.01	0.2	0.75	V
OTP UV Toggle Level on VBOOST	OTP_UV		13	−	15	V
OTP UV Toggle Level Hysteresis	OTP_UV_HYST		0.01	0.2	0.75	V
VBOOSTM3V: HIGH SIDE AUXILIARY SUPPLY						
VBSTM3 Regulator Output Voltage	V_{BSTM3}	Referenced to VBOOST	−3.6	−3.3	−3.0	V
DC Output Current Consumption	M3V_IOUT		−	5	28 (Note 18)	mA
Output Current Limitation	M3V_ILIM		−	−	200	mA
VBSTM3 External Decoupling Cap.	$C_{VBSTM3V}$	Referenced to VBOOST	0.3	−	2.2	μF
VBSTM3 Ext. Decoupling Cap. ESR	$C_{VBSTM3V\_ESR}$	Referenced to VBOOST	−	−	200	mΩ
OSC10M: SYSTEM OSCILLATOR CLOCK						
System Oscillator Frequency	FOSC10M		8	10	12	MHz
ADC FOR MEASURING V_{BOOST}, V_{DD}, V_{LED}, TEMP						
ADC Resolution	ADC_RES		−	8	−	Bits
Nonlinearity Integral (INL) Differential (DNL)	 ADC_INL ADC_DNL	Best Fitting Straight Line Method	 −1.5 −2.0	 − −	 +1.5 +2.0	LSB
Full Path Gain Error for Measurements of V_{DD}, V_{LED}, V_{BOOST}	ADC_GAINER		−3.25	−	3.25	%
Offset at Output of ADC	ADC_OFFSET		−2	−	2	LSB
Time for 1 SAR Conversion	ADC_CONV	Full Conversion of 8 Bits	6.67	8	10	μs
ADC Full Scale for V_{DD} Measurement	ADCFS_VDD		3.87	4	4.13	V
ADC Full Scale for V_{LED} Measurement	ADCFS_VLED00 ADCFS_VLED01 ADCFS_VLED10 ADCFS_VLED11	The V_{LED} Range Code is “00” The V_{LED} Range Code is “01” The V_{LED} Range Code is “10” The V_{LED} Range Code is “11”	67.725 48.375 38.700 29.025	70 50 40 30	72.275 51.625 41.300 30.975	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
18. V_{BOOST} = 68 V, V_{LED} = 34 V, f_{BUCK} = 2 MHz, maximum total gate charge for activated BUCK channel Q_{GATE} = 14 nC.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
ADC FOR MEASURING V_{BOOST}, V_{DD}, V_{LED}, TEMP						
ADC Full Scale for V_{BOOST} Measurement	ADCFS_VBST		67.725	70	72.275	V
ADC Full Scale for Temp. Measurement	ADCFS_TEMP		193.5	200	206.5	°C
TSD Threshold Level	ADC_TSD	ADC Measurement of Junction Temperature	163	169	175	°C
V_{LED} Input Impedance	VLED_RES		210	−	650	kΩ
BUCK REGULATOR − SWITCH						
On Resistance, Range 1	Rdson1	At Room-Temperature, I(VINBCK) = 0.18 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	5.2	Ω
On Resistance at Hot, Range 1	Rdson1_hot	At Tj = 150 °C, I(VINBCK) = 0.18 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	7.2	Ω
On Resistance, Range 2	Rdson2	At Room-Temperature, I(VINBCK) = 0.375 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	2.6	Ω
On Resistance at Hot, Range 2	Rdson2_hot	At Tj = 150 °C, I(VINBCK) = 0.375 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	3.6	Ω
On Resistance, Range 3	Rdson3	At Room-Temperature, I(VINBCK) = 0.75 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	1.3	Ω
On Resistance at Hot, Range 3	Rdson3_hot	At Tj = 150 °C, I(VINBCK) = 0.75 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	1.8	Ω
On Resistance, Range 4	Rdson4	At Room-Temperature, I(VINBCK) = 1.5 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	0.65	Ω
On Resistance at Hot, Range 4	Rdson4_hot	At Tj = 150 °C, I(VINBCK) = 1.5 A, V(BOOST − VINBCK) ≤ 0.2 V	−	−	0.9	Ω
Switching Slope – ON Phase	T_{RISE}		−	3	−	V/ns
Switching Slope – OFF Phase (Note 19)	T_{FALL}		−	3	−	V/ns
BUCK REGULATOR − CURRENT REGULATION						
Current Sense Threshold Level, Range 1, Min Value	ITHR1_000	[BUCK_VTHR = 00000000] End of the BUCK ON-Phase	23.905	28.125	32.344	mA
Current Sense Threshold Level, Range 1, Spec. Value	ITHR1_110	[BUCK_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	112.5	−	mA
Current Sense Threshold Level, Range 1, Max Value	ITHR1_255	[BUCK_VTHR = 11111111] End of the BUCK ON-Phase	−	224.15	−	mA
Current Sense Threshold Level, Range 2, Min Value	ITHR2_000	[BUCK_VTHR = 00000000] End of the BUCK ON-Phase	47.813	56.25	64.688	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
19. Falling switching slope depends on used current (range, current sense threshold level) and free-wheeling diode capacitance.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
BUCK REGULATOR − CURRENT REGULATION						
Current Sense Threshold Level, Range 2, Spec. Value	ITHR2_110	[BUCK_VTHR = 01101110] End of the BUCK ON-phase. Min. Value for Specified Precision	−	225	−	mA
Current Sense Threshold Level, Range 2, Max Value	ITHR2_255	[BUCK_VTHR = 11111111] End of the BUCK ON-Phase	−	448.3	−	mA
Current Sense Threshold Level, Range 3, Min Value	ITHR3_000	[BUCK_VTHR = 00000000] End of the BUCK ON-Phase	95.625	112.5	129.375	mA
Current Sense Threshold Level, Range 3, Spec. Value	ITHR3_110	[BUCK_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	450	−	mA
Current Sense Threshold Level, Range 3, Max Value	ITHR3_255	[BUCK_VTHR = 11111111] End of the BUCK ON-phase	−	896.6	−	mA
Current Sense Threshold Level, Range 4, Min Value	ITHR4_000	[BUCK_VTHR = 00000000] End of the BUCK ON-Phase	191.25	225	258.75	mA
Current Sense Threshold Level, Range 4, Spec. Value	ITHR4_110	[BUCK_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	900	−	mA
Current Sense Threshold Level, Range 4, Max Value	ITHR4_255	[BUCK_VTHR = 11111111] End of the BUCK ON-Phase	−	1791.75	−	mA
Current Sense Threshold Increase per Code, Range 1	δITHR1	8 Bit, Linear Increase	−	0.77	−	mA
Current Sense Threshold Increase per Code, Range 2	δITHR2	8 Bit, Linear Increase	−	1.54	−	mA
Current Sense Threshold Increase per Code, Range 3	δITHR3	8 Bit, Linear Increase	−	3.08	−	mA
Current Sense Threshold Increase per Code, Range 4	δITHR4	8 Bit, Linear Increase	−	6.15	−	mA
Current Threshold Accuracy Only with Trimming Constant for the Highest Range (Note 20)	ITHR_ERR_DD	Specified for BUCK_VTHR ≥ 01101110, without the Delta of the Trimming Code and without Temp. Compensation	−8	−	+8	%
Current Threshold Accuracy without Temperature Compensation (Note 20)	ITHR_ERR_D	Specified for BUCK_VTHR ≥ 01101110, with the Delta of the Trimming Code and without Temp. Compensation	−6	−	+6	%
Current Threshold Accuracy (Note 20)	ITHR_ERR	Specified for BUCK_VTHR ≥ 01101110, the Delta of the Trimming Code and Temp. Compensation	−3	−	+3	%
Over-Current Detection Level, Range 1	OCDR1	Typ. 1.5 × ITHR1_255	286	−	388	mA
Over-Current Detection Level, Range 2	OCDR2	Typ. 1.5 × ITHR2_255	573	−	776	mA
Over-Current Detection Level, Range 3	OCDR3	Typ. 1.5 × ITHR3_255	1148	−	1553	mA
Over-Current Detection Level, Range 4	OCDR4	Typ. 1.5 × ITHR4_255	2295	−	3105	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
20. Measured as comparator DC threshold value, without comparator delay and switch falling slope.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
BUCK REGULATOR − CURRENT REGULATION						
Time Constant for Longest Off Time	TC_00	[BUCK_TOFF = 00000]	−	50	−	μs·V
Time Constant for Shortest Off Time	TC_31	[BUCK_TOFF = 11111]	−	5	−	μs·V
T_{OFF} Time Relative Error	TOFF_ERR	TC = $T_{OFF} \times V_{LED}$ @ VLED > 2 V, T_{OFF} > 350 ns	−10	−	+10	%
T_{OFF} Time Absolute Error	TOFF_ERR_ABS	TC = $T_{OFF} \times V_{LED}$ @ VLED > 2 V, $T_{OFF} \leq$ 350 ns	−35	−	+35	ns
Time Constant Decrease per Code	δTC	5 Bits, Exponential Decrease	−	7.16	−	%
Detection Level of V_{LED} to be Too Low	VLED_LMT		1.62	1.8	1.98	V
T_{OFF} Time for Low V_{LED} Voltages	TC_LOW	VLED < VLED_LMT	78	105	120	μs
OpenLED Detection Time	TON_OPEN		40	50	60	μs
Buck Minimum T_{ON} Time	TON_MIN	For VINBCK – LBCKSW < 2.4 V, No Failure at LBCKSW Pin	50	−	250	ns
Delay from BUCK ISENS Comparator Input Voltage Balance to BUCK Switch Going OFF	ISENSCMP_DEL	ISENS Cmp. Over-Drive ramp > 1 mV/10 ns	−	70	−	ns
5 V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, LEDCTRL, RSTB)						
High-Level Input Voltage	VINHI		2	−	−	V
Low-Level Input Voltage	VINLO		−	−	0.8	V
Pull Resistance (Note 21)	R_{PULL}		40	−	160	kΩ
LED PWM Propagation Delay (Note 22)	BUCK_SW_DEL	Activation Time of the BUCK Switch from the LEDCTRL Pin	4.4	5.5	6.95	μs
Sampling Resolution	LEDCTRL_SR		−	100	125	ns
RSTB Debouncer Time	RSTB_DEB		−	100	200	ns
5 V TOLERANT OPEN-DRAIN DIGITAL OUTPUT (SDO)						
Low-Voltage Output Voltage	VOUTLO	I_{OUT} = −10 mA (Current Flows into the Pin)	−	−	0.4	V
Equivalent Output Resistance	RDSON	Low-Side Switch	−	10	40	Ω
SDO Pin Leakage Current	SDO_ILEAK		−	−	2	μA
SDO Pin Capacitance	SDO_C		−	−	10	pF
CLK to SDO Propagation Delay	SDO_DL	Low-Side Switch Activation/Deactivation Time; @ 1 kΩ to 5 V, 100 pF to GND, for Falling Edge V(SDO) Goes below 0.5 V	−	−	60	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

21. Pull down resistor (R_{PD}) for RSTB, LEDCTRL, SDI and SCLK, pull up resistor (R_{PU}) for CSB to VDD.
22. Jitter is present due to the internal resynchronization.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
3 V DIGITAL INPUTS (TEST, TEST1, TEST2)						
High-Level Input Voltage	VIN3HI		2.3	−	−	V
Low-Level Input Voltage	VIN3LO		−	−	0.8	V
Pull Resistance	R_{PD3}	Pull-Down Resistance	−	−	60	kΩ
SPI INTERFACE						
CSB Setup Time	t_{CSS}		0.5	−	−	μs
CSB Hold Time	t_{CSH}		0.25	−	−	μs
SCLK Low Time	t_{WL}		0.5	−	−	μs
SCLK High Time	t_{WH}		0.5	−	−	μs
Data-In (DIN) Setup Time, Valid Data before Rising Edge of CLK	t_{SU}		0.25	−	−	μs
Data-In (DIN) Hold Time, Hold Data after Rising Edge of CLK	t_H		0.275	−	−	μs
Output (DOUT) Disable Time (Note 23)	t_{DIS}		0.08	−	0.32	μs
Output (DOUT) Valid (Note 23)	$t_{V1\rightarrow0}$		−	−	0.32	μs
Output (DOUT) Valid (Note 24)	$t_{V0\rightarrow1}$		−	−	0.32 + $t_{(RC)}$	μs
Output (DOUT) Hold Time	t_{HO}		0.01	−	−	μs
CSB High Time	t_{CS}		1	−	−	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
23. SDO low-side switch activation time.
24. Time depends on the SDO load and pull-up resistor.

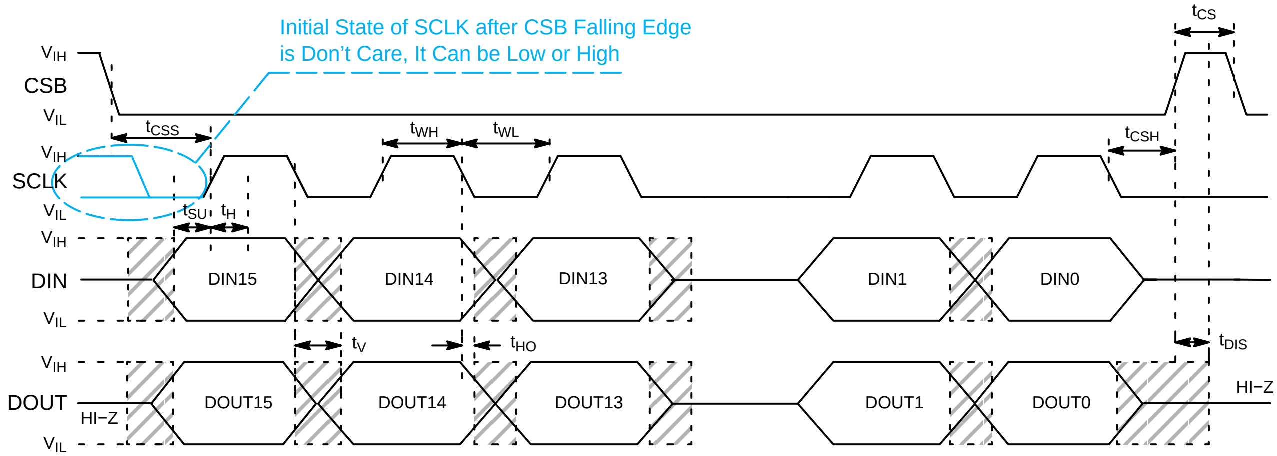


Figure 5. SPI Communication Timing

TYPICAL CHARACTERISTICS

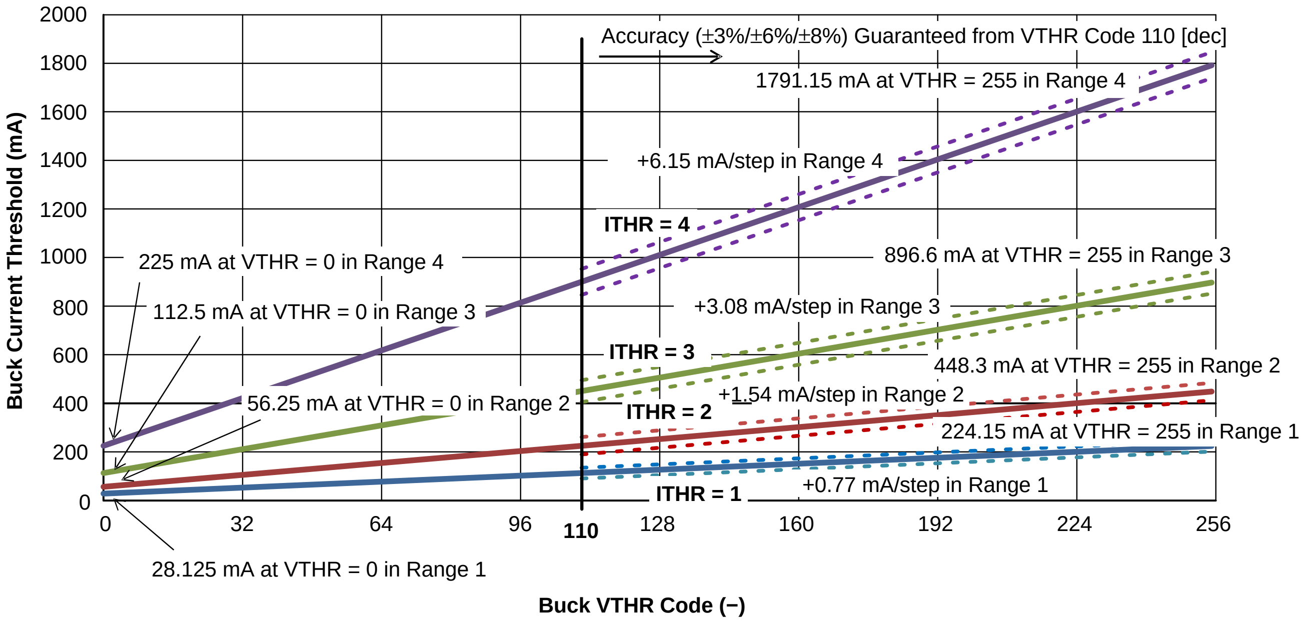


Figure 6. Buck Peak Current vs. Ranges and VTHR Code

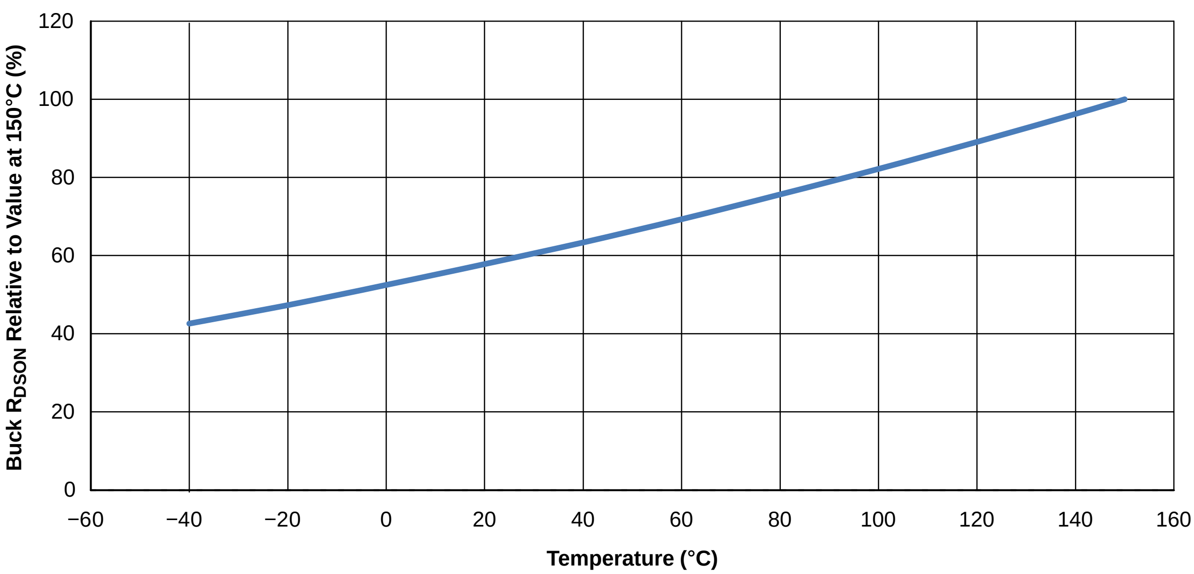


Figure 7. Typical Temperature Behavior of Buck Switch R_{DSON} Relative to the Value at 150°C

TYPICAL CHARACTERISTICS

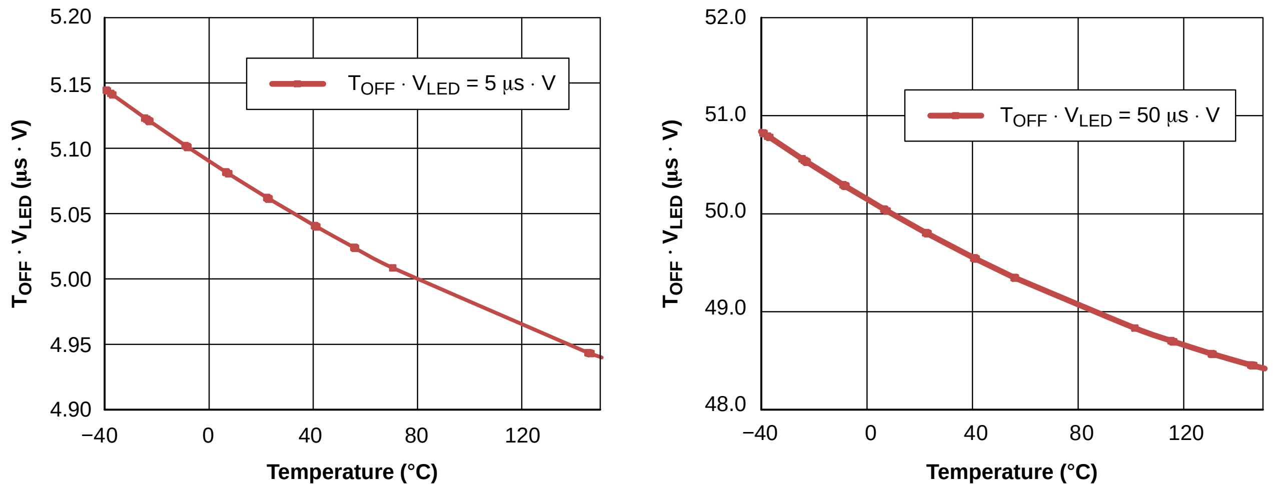
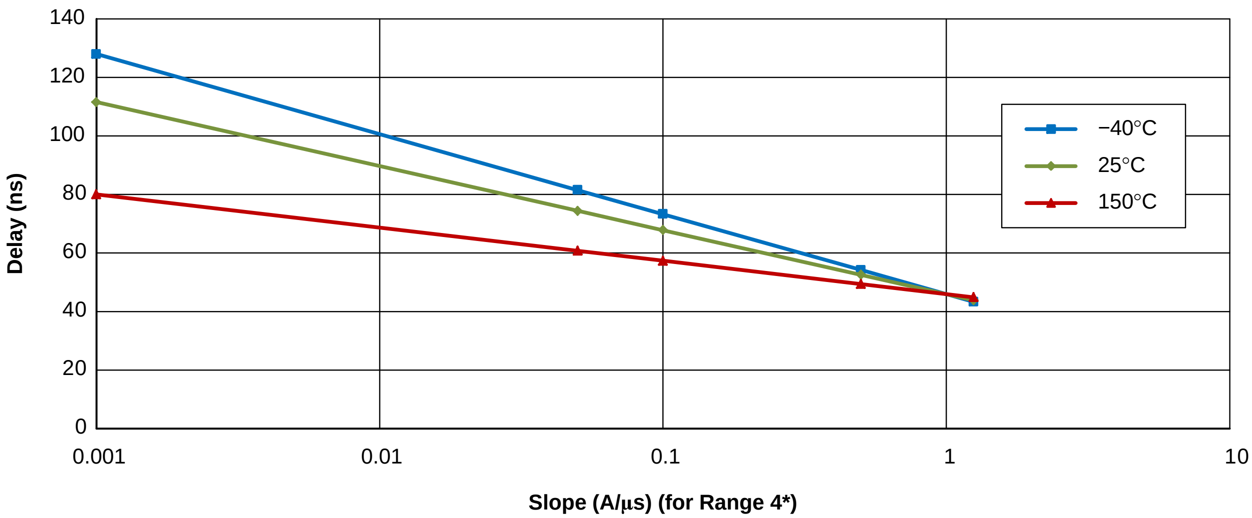


Figure 8. Typical Temperature Dependency of $T_{OFF} \cdot V_{LED}$ Constant (Shortest $T_{OFF} \cdot V_{LED}$ = 5 µs · V and Longest $T_{OFF} \cdot V_{LED}$ = 50 µs · V)



* In lower ranges, the same current slope (A/s) translates into a higher voltage slope (V/s) at the input of the comparator, because of the higher R_{DSON}. Resulting equations for all ranges:

Range 4: Comp. Delay [ns] = (0.0365 · Temp [°C] − 10.41) · ln(Slope [A/µs, Range 4]) + 46
Range 3: Comp. Delay [ns] = (0.0365 · Temp [°C] − 10.41) · ln(Slope · 2 [A/µs, Range 4]) + 46
Range 2: Comp. Delay [ns] = (0.0365 · Temp [°C] − 10.41) · ln(Slope · 4 [A/µs, Range 4]) + 46
Range 1: Comp. Delay [ns] = (0.0365 · Temp [°C] − 10.41) · ln(Slope · 8 [A/µs, Range 4]) + 46

Figure 9. Typical Comparator Delay vs. Slope

DETAILED OPERATING DESCRIPTION

Supply Concept in General

Two voltages have to be supplied to the NCV78713 chip – low voltage VDD logic supply and high voltage VBOOST for providing energy to the buck regulator. More detailed description follows.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip. NCV78713 does not contain internal VDD regulator and this voltage is supposed to be provided externally by a dedicated voltage regulator that fulfills specified voltage and current needs or can be supplied from the NCV78702/NCV78703 VDD pin.

The Power-On-Reset circuit (POR) monitors the VDD voltage and RSTB pin to control the out-of-reset and reset entering state. At power-up, the chip will exit from reset state when VDD > POR3V_H and RSTB pin is in "log. 1". No SPI communication is possible in reset state.

VBOOST Supply

The VBOOST supply voltage is the main high voltage supply for the chip. The voltage is supposed to be provided by booster chip such as NCV78702/NCV78703 or NCV878763 in an application. VINBCK pin has to be connected by low impedance track to this supply to ensure proper buck performance.

The VBOOST voltage is monitored by under-voltage comparator to check sufficient zapping voltage at VBOOST pin during OTP programming operation.

VBOOSTM3V Supply

The VBOOSTM3V is the high side auxiliary supply for the gate drive of the buck regulator's integrated high-side P-MOSFET switch. This supply receives energy directly from the VBOOST pin.

Internal Clock Generation – OSC10M

An internal RC clock named OSC10M is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection (refer to Table 6 − OSC10M: System Oscillator Clock for details). All timings depend on OSC10M accuracy.

Buck Regulator

General

The NCV78713 contains one high-current integrated buck current regulator, which is the source for the LED string. The buck is powered from the external booster regulator.

Buck Current Regulation Principle

Buck controls the inductor peak current ($I_{BUCKpeak}$) and incorporates a constant ripple ($\Delta I_{BUCKpkpk}$) control circuit to ensure also stable average current through the LED string, independently from the string voltage. The buck average current is in fact described by the formula:

$$I_{BUCK_{AVG}} = I_{BUCK_{peak}} - \frac{\Delta I_{BUCK_{pkpk}}}{2} \quad \text{(eq. 1)}$$

This is graphically exemplified by Figure 10.

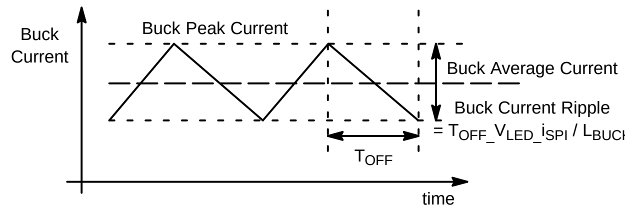


Figure 10. Buck Regulator Controlled Average Current

The parameter $I_{BUCKpeak}$ is programmable through the device by means of the internal registers for range selection BUCK_ISENS_THR[1:0] and code BUCK_VTHR[7:0].

The formula that defines the total ripple current over the buck inductor is also hereby reported:

$$\Delta I_{BUCK_{pkpk}} = \frac{T_{OFF} \cdot (V_{LED} + V_{DIODE})}{L_{BUCK}} \cong \frac{T_{OFF} \cdot V_{LED}}{L_{BUCK}} = \frac{T_{OFF\_}V_{LED\_}i_{SPI}}{L_{BUCK}} \quad \text{(eq. 2)}$$

In the formula above, T_{OFF} represents the buck switch off time, V_{LED} is the LED voltage feedback sensed at the NCV78713 VLED pin and L_{BUCK} is the buck inductance value. The parameter $T_{OFF\_}V_{LED\_}i_{SPI}$ is programmable by SPI (BUCK_TOFF[4:0] register), with values related to Table 6 − Buck Regulator – Current Regulation. In order to achieve a constant ripple current value, the device varies the T_{OFF} time inversely proportional to the V_{LED} sensed at the device pin, according to the selected factor $T_{OFF\_}V_{LED\_}i_{SPI}$. As a consequence to the constant ripple control and variable off time, the buck switching frequency depends on the boost voltage and LED voltage in the following way:

$$f_{BUCK} = \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \cdot \frac{1}{T_{OFF}} = \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \cdot \frac{V_{LED}}{T_{OFF\_}V_{LED\_}i_{SPI}} \quad \text{(eq. 3)}$$

The LED average current in time (DC) is equal to the buck time average current. Therefore, to achieve a given LED current target, it is sufficient to know the buck peak current and the buck current ripple. A rule of thumb is to count a minimum of 50% ripple reduction by means of the capacitor C_{BUCK} and this is normally obtained with a low cost ceramic component ranging from 100 nF to 470 nF (such values are typically used at connector sides anyway, so this is included in a standard BOM). The following figure reports a typical example waveform:

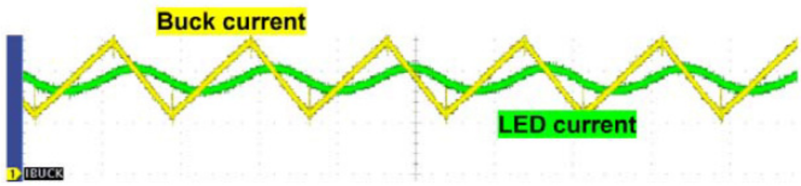


Figure 11. LED Current AC Components Filtered Out by Output Impedance (Oscilloscope Snapshot)

The use of C_{BUCK} is a cost effective way to improve EMC performances without the need to increase the value of L_{BUCK}, which would be certainly a far more expensive solution.

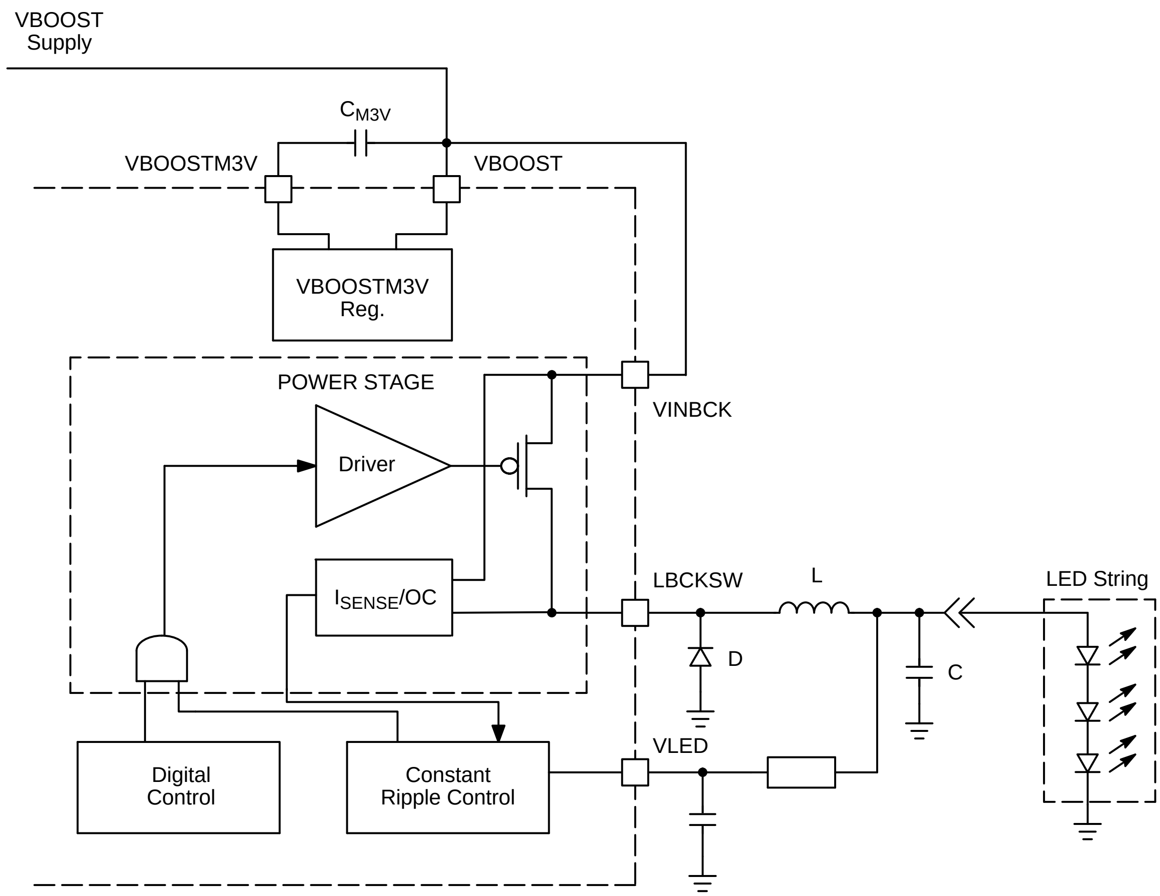


Figure 12. Buck Regulator Circuit Diagram

SW Compensation of the Buck Current Accuracy

In order to ensure buck current accuracy as specified in Table 6 − Buck Regulator – Current Regulation, set of constants trimmed during manufacturing process is available. Microcontroller should use them in the following way:

<u>To Reach ±8% Accuracy (±6% for Range 4) Over Whole Temperature Operating Range:</u>

All ranges: ***BUCK_ISENS_TRIM[6:0] = BUCK_ISENS_RNG[6:0]***

BUCK_ISENS_RNG[6:0] is trimming constant for the highest current range (Range 4) at hot temperature.

BUCK_ISENS_RNG[6:0] constant is loaded into BUCK_ISENS_TRIM[6:0] register automatically after the reset of the device.

<u>To Reach ±6% Accuracy Over Whole Temperature Operating Range:</u>

BUCK_ISENS_Dx[3:0] registers, meaning delta of the trimming constant with respect to the higher current range at hot temperature, have to be used. Trimming constant for the particular range at hot temperature can be then calculated as:

Range 4: ***BUCK_R4_trim_hot = BUCK_ISENS_RNG[6:0]***,
Range 3: ***BUCK_R3_trim_hot = BUCK_ISENS_RNG[6:0] + BUCK_ISENS_D3[3:0]***,
Range 2: ***BUCK_R2_trim_hot = BUCK_ISENS_RNG[6:0] + BUCK_ISENS_D3[3:0] + BUCK_ISENS_D2[3:0]***,
Range 1: ***BUCK_R1_trim_hot = BUCK_ISENS_RNG[6:0] + BUCK_ISENS_D3[3:0] + BUCK_ISENS_D2[3:0] + BUCK_ISENS_D1[3:0]***,

where:

delta of the trimming constant BUCK_ISENS_Dx[3:0] is signed, coded as two’s complement. Range of this constant is decadic <−8; 7>, binary <1000; 0111>.

Calculated trimming constant has to be then written into trimming SPI register:
BUCK_ISENS_TRIM[6:0] = BUCK_Ry_trim_hot

<u>To Reach ±3% Accuracy Over Whole Temperature Operating Range:</u>

In addition to BUCK_ISENS_Dx[3:0] registers, the BUCK_ISENS_TCx[3:0] registers, meaning temperature coefficients for the appropriate ranges, have to be used. Trimming value for a certain temperature can be then calculated as:

Range 4: ***BUCK_R4_trim = BUCK_R4_trim_hot*** + $k_{L3} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 3: ***BUCK_R3_trim = BUCK_R3_trim_hot*** + $k_{L2} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 2: ***BUCK_R2_trim = BUCK_R2_trim_hot*** + $k_{L1} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 1: ***BUCK_R1_trim = BUCK_R0_trim_hot*** + $k_{L0} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,

where:

buck temperature coefficient BUCK_ISENS_TCx[3:0] is signed, coded as two’s complement. Range of this constant is decadic <−8; 7>, binary <1000; 0111>,

k_{Lx} is linear coefficient for each current range calculated: k_{Lx} = (BUCK_ISENS_TCx[3:0] – $k_Q \cdot (170°C)^2$)/(−170°C) [code/°C]

k_Q is quadratic constant for all current ranges: $k_Q = 2.18 \cdot 10^{-4}$ [code/(°C)^2]

Tj is junction temperature in °C calculated from VTEMP[7:0] SPI register value according to the equation defined in chapter *ADC:* Device Temperature ADC: V_{TEMP}.

Thot temperature is constant equal to 125°C.

Calculated trimming constant has to be then written into trimming SPI register**:**
BUCK_ISENS_TRIM[6:0] = BUCK_Ry_trim

<u>Note</u>: The BUCK_ISENS_TRIM[6:0] SPI register allows compensation of the peak current app. in range ±40 % from actual value according to the following equation:

IBUCK = (ITHRx_000 + δITHRx · BUCK_VTHR[7:0]) · (1 + 0.4 · ((BUCK_ISENS_TRIM[6:0] − 63)/63)),

where:

ITHRx_000 is current for VTHR code 0 in ITHRx range (see Table 6 − Buck Regulator – Current Regulation),
δITHRx code step in range ITHRx (see Table 6 − Buck Regulator – Current Regulation).

Buck Overcurrent Protection

Being a current regulator, the NCV78713 buck is by nature preventing overcurrent in all normal situations. However, in order to protect the system from overcurrent even in case of failures, protection mechanism is available.

This protection is based on internal sensing over the buck switch: when the peak current rises above the maximum limit (OCDRx level, see Table 6 − Buck Regulator – Current Regulation), an internal counter starts to increment at each period, until the count written in BUCK_OC_OCCMP_THR[1:0] + 1 is attained. The count is reset if the current drops below OCDRx level or the buck channel is disabled and also at each dimming cycle. From the moment the count is reached onwards, the buck is kept continuously off, until the SPI error flag OCLED is read. After reading the flag, the buck is automatically re-enabled and will try to regulate the current again.

Dimming

The NCV78713 supports both analog and digital dimming (or so called PWM dimming). Analog dimming is performed by controlling the LED amplitude current during operation. This can be done by means of changing the peak current level and/or the T_{OFF}_V_{LED}_i_{SPI} constants by SPI commands (see Buck Regulator section).

In this section, we only describe PWM dimming as this is the preferred method to maintain the desired LED color temperature for a given current rating. In PWM dimming, the LED current waveform frequency is constant and the duty cycle is set according to the required light intensity. In order to avoid the beats effect, the dimming frequency should be set at “high enough” values, typically above 300 Hz.

PWM dimming is controlled externally by means of LEDCTRL input.

Digital Dimming

In digital dimming, the buck activation is transparently linked to the logic status of the LEDCTRL pin, which handles dimming signal. The only difference is the controlled phase shift of typical 5.5 μs (Table 6 − 5 V Tolerant Digital Inputs) that allows synchronized measurements of the VLED pin via the ADC (see dedicated section for more details). As the phase shift is applied both to rising edges and falling edges, with a very limited jitter, the PWM duty cycle is not affected. Apart from the phase shift and the system clock OSC10M, there is no limitation to the PWM duty cycle values or resolutions at the buck, which is a copy of the reference provided at the input.

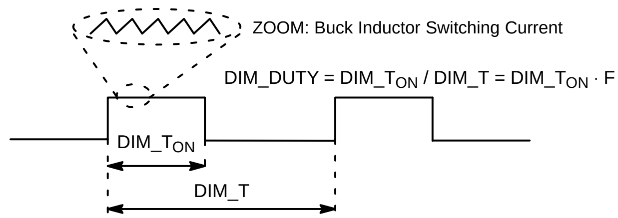


Figure 13. Buck Current Digital or PWM Dimming

ADC

General

The built-in analog to digital converter (ADC) is an 8-bit successive approximation register (SAR). This embedded peripheral can be used to provide the following measurements to the external Micro Controller Unit (MCU):

- VBOOST Voltage: Sampled at the VBOOST Pin
- VDD Voltage: Sampled at the VDD Pin
- VLEDON Voltage
- VLED Voltage
- VTEMP Measurement (Chip Temperature)

The internal NCV78713 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The external MCU can read out all ADC measured values via the SPI interface, in order to take application specific decisions. Please note that none of the MCU SPI commands interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

The state machine sampling and conversion scheme is represented in the figure below.

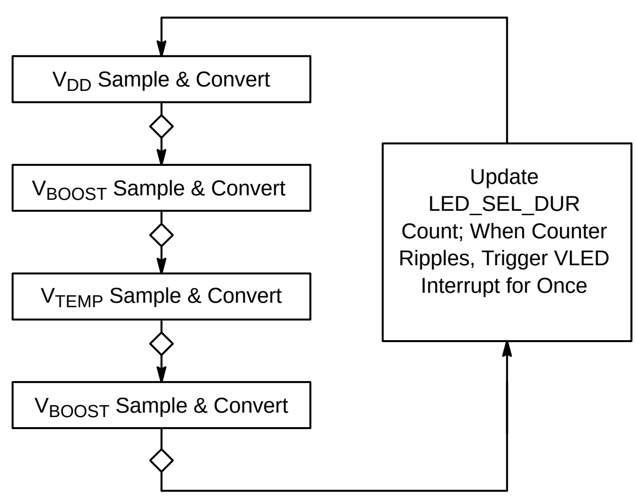


Figure 14. ADC Sample and Conversion Main Sequence

Referring to the figure above, the typical rate for a full SAR plus digital conversion per channel is 8 μs (Table 6 − ADC for Measuring VBOOST, VDD, VLED, TEMP). For instance, each new VBOOST ADC converted sample occurs at 16 μs typical rate, whereas for both the VDD and VTEMP channel the sampling rate is typically 32 μs, that is to say a complete cycle of the depicted sequence. This time is referred to as TADC_SEQ.

If the SPI setting LED_SEL_DUR[8:0] is not zero, then interrupts for the VLED measurements are allowed at the points marked with a rhombus, with a minimum cadence corresponding to the number of the elapsed ADC sequences (forced interrupt). In formulas:

$$T_{VLED\_INT\_Forced} = LED\_SEL\_DUR[8:0] \cdot T_{ADC\_SEQ} \qquad \text{(eq. 4)}$$

In general, prior to the forced interrupt status, the $VLED_{ON}$ ADC interrupts are generated when a falling edge on the control line for the buck is detected by the device. In case of *digital dimming*, this interrupt start signal corresponds to the LEDCTRL falling edge together with a controlled phase delay (Table 6 − 5 V Tolerant Digital Inputs). The purpose of the phase delay is to allow completion the ongoing ADC conversion before starting the one linked to the VLED interrupt: if at the moment of the conversion LEDCTRL pin is logic high, then the updated registers are VLEDON[7:0] and VLED[7:0]; otherwise, if LEDCTRL pin is logic low, the only register refreshed is VLED[7:0]. This mechanism is handled automatically by the NCV78713 logic without need of intervention from the user, thus drastically reducing the MCU cycles and embedded firmware and CPU cycles overhead that would be otherwise required.

A flow chart referring to the ADC interrupts is also displayed.

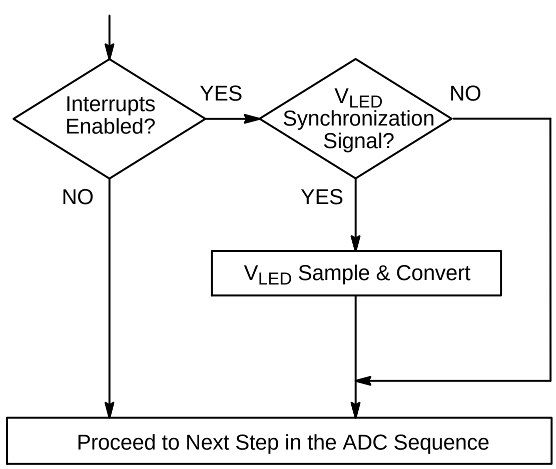


Figure 15. ADC VLED Interrupt Sequence

All NCV78713 ADC registers data integrity is protected by ODD parity on the bit 8 (that is to say the 9th bit if counting from the LSbit named "0"). Please refer to the SPI map section for further details.

Logic Supply Voltage ADC: V_{DD}

The logic supply voltage is sampled at VDD pin. The (8-bit) conversion ratio is 4/255 (V/dec) = 0.0157 (V/dec) typical. The converted value can be found in the SPI register VDD[7:0], protected with ODD parity bit.

Boost Voltage ADC: V_{BOOST}

This measurement refers to the boost voltage at the VBOOST pin, with an 8 bit conversion ratio of 70/255 (V/dec) = 0.274 (V/dec) typical, result can be found inside the SPI register VBOOST[7:0]. The value is protected by ODD parity bit. This measurement can be used by the MCU for diagnostics and booster control loop monitoring.

Device Temperature ADC: V_{TEMP}

By means of the VTEMP measurement, the MCU can monitor the device junction temperature (T_J) over time. The conversion formula is:

$$T_J = (VTEMP[7:0] - 50.5)/0.805 \qquad \text{(eq. 5)}$$

VTEMP[7:0] is the value read out directly from the related 8bit-SPI register (please refer to the SPI map). The value is also used internally by the device for the *thermal warning* and *thermal shutdown* functions. More details on these two can be found in the dedicated sections in this document. The value is protected by ODD parity bit.

LED String Voltage ADC: V_{LED}, V_{LEDON}

The voltage at the pin VLED is measured. There are 4 ranges available, that can be selected by means of ADC_VLED_RNG_SEL[1:0] register, to obtain higher resolution for LED voltage measurement.

Conversion ratios in dependency on selected range are:

0x0: 70/255 (V/dec) = 0.274 (V/dec);
0x1: 50/255 (V/dec) = 0.196 (V/dec);
0x2: 40/255 (V/dec) = 0.157 (V/dec);
0x3: 30/255 (V/dec) = 0.118 (V/dec).

This information, found in registers VLEDON[7:0] and VLED[7:0], can be used by the MCU to infer about the LED string status, for example, individual shorted LEDs. As for the other ADC registers, the values are protected by ODD parity.

Please note that in the case of constant LEDCTRL inputs and no dimming (in other words dimming duty cycle equals to 0% or 100%) the VLED interrupt is forced with a rate equal to $T_{VLED\_INT\_forced}$, given in the ADC general section. This feature can be exploited by MCU embedded algorithm diagnostics to read the LED channel voltage even when in OFF state, before module outputs activation (module startup pre-check).

Diagnostics

The NCV78713 features a wide range of embedded diagnostic features. Their description follows. Please also refer to the previous SPI section for more details.

Diagnostic Description

- *Thermal Warning:* this mechanism detects a user-programmable junction temperature which is in principle close, but lower, to the chip maximum allowed, thus providing the information that some action (power de-rating) is required to prevent overheating that would cause Thermal Shutdown. A typical power de-rating technique consists in reducing the output dimming duty cycle in function of the temperature: the higher the temperature above the thermal warning, the lower the duty cycle. The thermal warning flag (TW) is given in status register 0x14 and is latched. When VTEMP[7:0] raises to or above THERMAL_WARNING_THR[7:0] threshold, the TW flag is set. At power up the default thermal warning threshold is typically 159°C (SPI code 179).
- *Thermal Shutdown:* this safety mechanism intends to protect the device from damage caused by overheating, by disabling the both buck channels. The diagnostic is displayed per means of the TSD bit in status register 0x14 (latched). Once occurred, the thermal shutdown condition is exited when the temperature drops below the thermal warning level, thus providing hysteresis for thermal shutdown recovery process. Output is re-enabled automatically if BUCK_TSD_AUT_RCRV_EN = 1, or it is re-enabled by rising edge on BUCK_EN if BUCK_TSD_AUT_RCRV_EN = 0. The application thermal design should be made as such to avoid the thermal shutdown in the worst case conditions. The thermal shutdown level is not user programmable and is factory trimmed (see ADC_TSD in Table 6 − Buck Regulator – Switch).
- *SPI Error:* in case of SPI communication errors the SPIERR bit in status register 0x14 is set. The bit is latched. For more details, please refer to section “SPI protocol: Framing and Parity Error”.
- *Open LED String:* open LED diagnostic flag indicates whether the string is detected open. The detection is based on a counter overflow of typical 50 μs when the channel is activated. OPENLED flag (latched) is contained in status register 0x13. Please note that the open detection does not disable the buck channel(s).
- *Short LED String:* a short circuit detection is available per means of the flag SHORTLED (non-latched, status register 0x13). The detection is based on the voltage measured at the VLED pin via a dedicated internal comparator: when the voltage drops below the VLED_LMT minimum threshold (typical 1.8 V, see Table 6 − Buck Regulator – Current Regulation) the flag is set. Together with the detection, a fixed TOFF is used. Note that the detection is active also when the LED channel is off (in this case the fixed TOFF does not play any role).
- *Overcurrent:* this diagnostics protects the LED and the buck electronics from overcurrent. As the overcurrent is detected, the OCLED flag (latched, status register 0x13) is raised and the buck channel is disabled. More details about the detection mechanisms and parameters are given in section “Buck Overcurrent Protection”.
- *Buck Status:* register BUCK_STATUS shows the actual status of Buck output. When BUCK_STATUS is 1, the output regulates current to the LED.
- *LEDCTRL Pin Status:* SPI register LEDVAL indicates the actual logic level of the debounced LEDCTRL pin. This signal follows the output of 200 ns digital debouncer implemented on LEDCTRL pin.
- *Buck Running at Minimum TON Time:* register BUCK_MIN_TON (latched) indicates that minimal TON time is detected on the buck channel. It is clear by read flag. This information can be used for detection of transition period during which the BUCK output current decreases due to the change of BUCK_VTHR code or BUCK_ISENS_THR range.
- *Buck TON Time Duration:* SPI register BUCK_TON_DUR[7:0] reflects the last measured Buck TON time (1LSB = 200 ns) on the corresponding channel. When Buck runs with TON time < typ. 200 ns, the BUCK_TON_DUR[7:0] SPI register returns value 0x00. When Buck is stopped, the BUCK_TON_DUR[7:0] register keeps the last measured TON time.
- *HW Reset:* the out of reset condition is reported through the HWR bit (latched). This bit is set only at each Power On Reset (POR) and indicates the device is ready to operate.

A short summary table of the main diagnostic bits related to the LED outputs follows.

Table 7. LED OUTPUT DIAGNOSTIC SUMMARY

Diagnose		Detection Level	LED Output	Latched
Flag	Description			
TW	Thermal Warning	SPI Register Programmable	Not Disabled (If No TSD, otherwise Disabled)	Yes
TSD	Thermal Shutdown	Factory Trimmed	Disabled (Automatically Re-Enabled when Temp Falls below TW and BUCK_TSD_AUT_RCVR_EN = 1)	Yes
SPIERR	SPI Error	(See SPI Section)	Not Disabled	Yes
OPENLED	LED String Open Circuit	Buck on Time > TON_OPEN	Not Disabled	Yes
SHORTLED	LED String Short Circuit	VLED < VLED_LMT	Not Disabled (Fixed Buck TOFF Applied when Output is On)	No
OCLED	LED String Overcurrent	Ibuck > OCDR{1..4}	Disabled	Yes

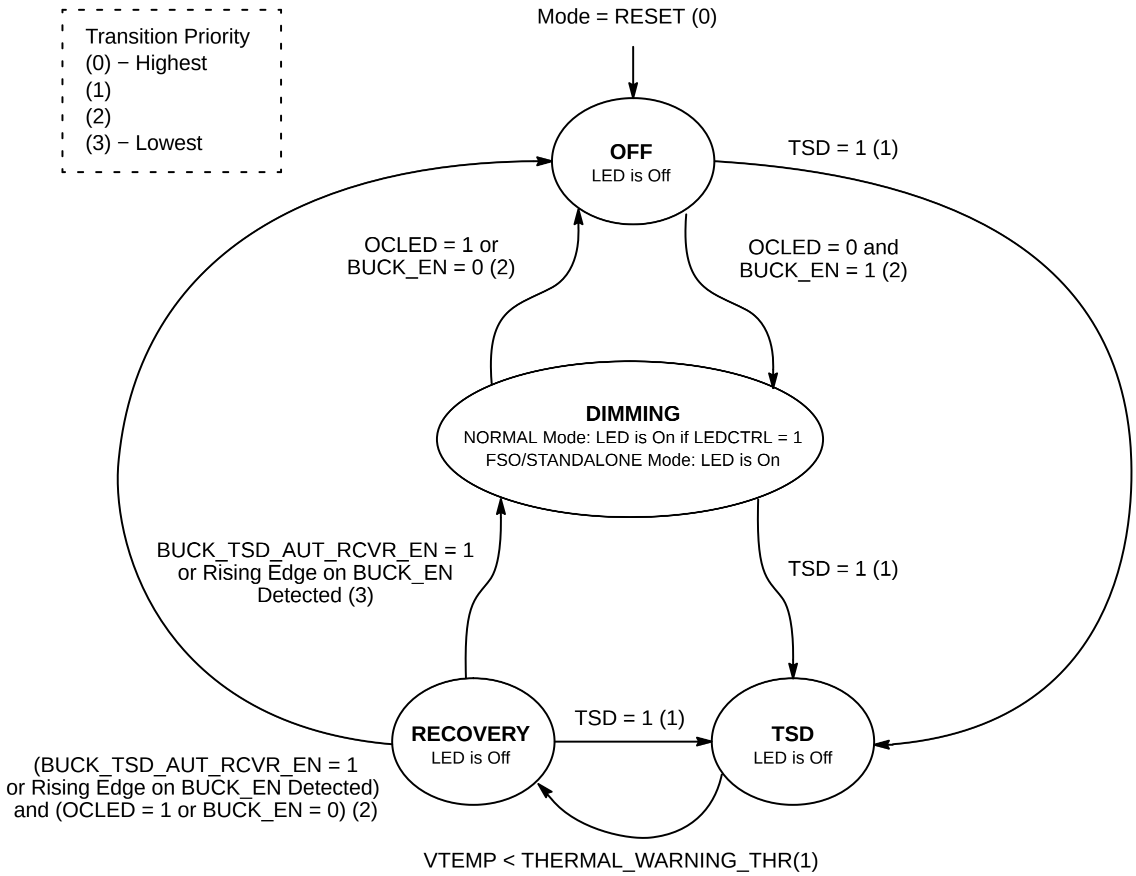


Figure 16. LED Dimming State Diagram

Functional Mode Description

Overview of all functional modes is in accordance to the state diagram on Figure 17. Individual states are described below.

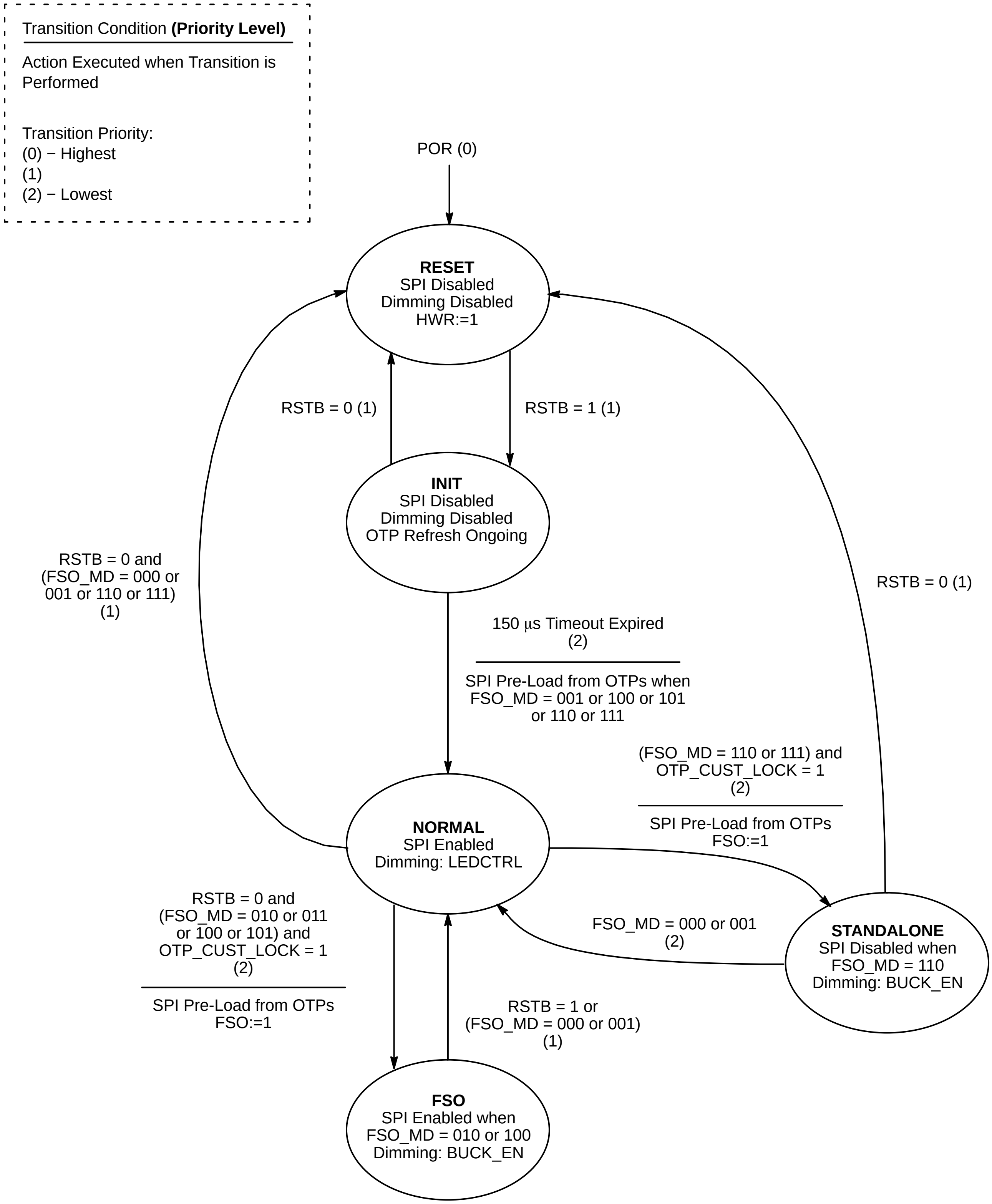


Figure 17. Functional Modes State Diagram

Reset

Asynchronous reset is caused either by POR (POR always causes asynchronous reset − transition to reset state) or by falling edge on RSTB pin (in normal/stand-alone mode, when FSO_MD[2:0] = 000 or 001 or 110 or 111).

Init and Normal Mode

Normal mode is entered through Init state after internal delay of 150 μs. In Init state, OTP refresh is performed. If OTP bits for FSO_MD[2:0] register and *OTP Lock Bit* are programmed, transition to FSO/SA mode is possible.

FSO/Stand-Alone Mode

FSO (Fail-Safe Operation)/Stand-Alone modes can be used for two main purposes:

- Default power-up operation of the chip (**Stand-Alone** functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings)
- **Fail-Safe** functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed)

FSO/stand-alone function is controlled according to Table 8. Entrance into FSO/Stand-alone mode is possible only after customer OTP zapping when *OTP Lock Bit* is set. After FSO mode activation, the FSO bit in status register is set. FSO register is cleared by read register.

When FSO/Stand-Alone mode is activated, content of the following SPI registers is preloaded from OTP memory:

BUCK_VTHR[7:0],
BUCK_ISENS_THR[1:0],
BUCK_TOFF[4:0],
BUCK_EN,
FSO_MD[2:0],
BUCK_TSD_AUT_RCVR_EN,
BUCK_OC_OCCMP_THR[1:0].

BUCK_ISENS_TRIM[6:0] register is preloaded from BUCK_ISENS_RNG[6:0] register.

In FSO (entered via falling edge on RSTB pin) and Stand-Alone modes, **BUCK_EN** is controlled from SPI register map (SPI registers are updated from OTP's after entrance into these modes).

BUCK_EN is supposed to be set '1' for the BUCK operation in the FSO/stand-alone mode.

When control registers are pre-loaded from OTP's after POR and FSO mode is not entered (valid for FSO_MD[2:0] = 100 or 101), BUCK_EN is kept inactive ('0') until the first valid SPI operation is finished to avoid potential activation of buck regulator immediately after POR (to prevent undefined state of LEDCTRL pin in case MCU leaves POR later than NCV78713).

In FSO and Stand-Alone modes, the logic level at **LEDCTRL** pin is ignored and digital PWM dimming with LEDCTRL pin is not available. The output can be dimmed only by means of BUCK_EN register.

A falling edge on RSTB pin may trigger either entrance into FSO mode or reset in dependency on FSO_MD[2:0] register value. Please refer to Table 8 and Figure 17 for more details.

Once FSO mode is entered via falling edge on RSTB pin, reset function of RSTB pin is blocked until FSO mode is exited. FSO mode can be exited by the rising edge on RSTB pin or by writing FSO_MD[2:0] = 000 or 001 (possible only in FSO modes, where SPI control register update is allowed: FSO_MD[2:0] = 011 or 101).

In stand-alone mode (FSO_MD[2:0] = 110 or 111), RSTB has always reset functionality.

During entrance into FSO mode, value of FSO_MD[2:0] SPI register (preloaded from OTP) is latched into internal register and all FSO related functions are then controlled according to it. Purpose is to avoid the reset of the device when FSO mode is active and FSO_MD[2:0] is changed to value corresponding to stand-alone mode, where RSTB pin has reset functionality. The internal register is cleared after POR or when FSO mode is exited.

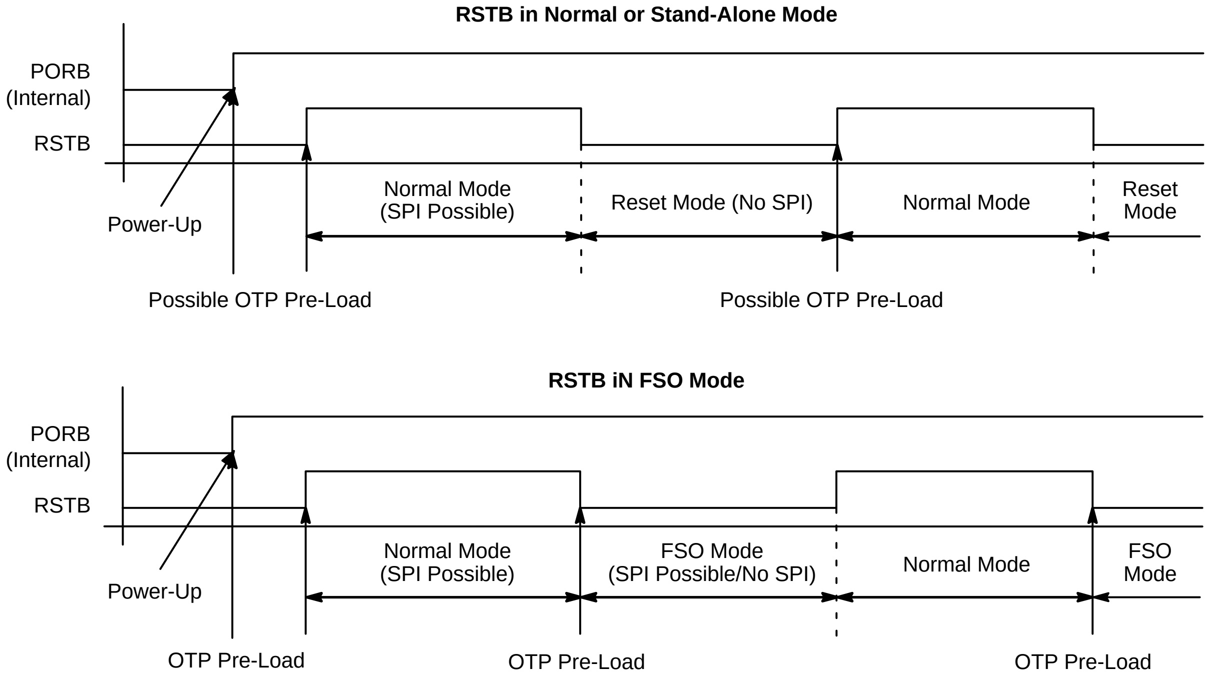


Figure 18. RSTB Pin Functionality in Normal, Stand-Alone and FSO Modes

Table 8. FSO MODES

FSO_MD[2:0]	Description
000_b = 0	**FSO Mode Disabled, Registers are Loaded with Safe Value = 0x00h after POR, Default** • After the reset, control registers are loaded with 0x00h value. • Entrance into FSO mode is not possible • RSTB pin has **reset** functionality • LEDCTRL pin is functional (buck enable/disable, digital PWM dimming available)
001_b = 1	**FSO Mode Disabled, Registers are Loaded with Data from OTP Memory after POR** • After the reset, control registers are loaded with data stored in OTP memory (device's OTP memory has to be programmed, *OTP Lock Bit* has to be set). It reduces number of SPI transfers needed to configure the device after the reset. • Entrance into FSO mode is not possible • RSTB pin has **reset** functionality • LEDCTRL pin is functional (buck enable/disable, digital PWM dimming available)
010_b = 2	**FSO Entered after Falling Edge on RSTB Pin, Registers are Loaded with Safe Value = 0x00h after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is **disabled** (SPI write operation is blocked; clearing of SPI registers is blocked; in case of invalid SPI frame, SPIERR flag is set). • RSTB pin serves to enter/exit FSO mode. • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).
011_b = 3	**FSO Entered after Falling Edge on RSTB Pin, Registers are Loaded with Safe Value = 0x00h after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is **enabled** • FSO mode can be exited by writing FSO_MD[2:0] = 000 • RSTB pins serves to enter/exit FSO mode. • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).
100_b = 4	**FSO Entered after Falling Edge on RSTB Pin, Registers are Loaded with Data from OTP Memory after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is **disabled** (SPI write operation is blocked; clearing of SPI registers is blocked; in case of invalid SPI frame, SPIERR flag is set). • RSTB pin serves to enter/exit FSO mode. • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).

Table 8. FSO MODES (continued)

FSO_MD[2:0]	Description
101_b = 5	**FSO Entered after Falling Edge on RSTB Pin, Registers are Loaded with Data from OTP Memory after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is **enabled** • FSO mode can be exited by writing FSO_MD[2:0] = 000 • RSTB pin serves to enter/exit FSO mode. • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).
110_b = 6	**SA (Stand-Alone)/FSO Entered after POR (RSTB Pin Rising Edge), Registers are Loaded with Data from OTP Memory** • After FSO/SA mode activation, control registers are loaded with data from OTP memory • SPI register update (SPI write/read operation) in SA/FSO mode is **disabled** (SPI write operation is blocked; clearing of SPI registers is blocked; in case of invalid SPI frame, SPIERR flag is set). • RSTB pin has **reset** functionality • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).
111_b = 7	**SA (Stand-Alone)/FSO Entered after POR (RSTB Pin Rising Edge), Registers are Loaded with Data from OTP Memory** • After SA/FSO mode activation, control registers are loaded with data from OTP memory • SPI register update (SPI write/read operation) in SA/FSO mode is **enabled** • FSO mode can be exited by writing FSO_MD[2:0] = 000 • RSTB pin has **reset** functionality • LEDCTRL pin is not functional (buck enable/disable only by means of BUCK_EN SPI/OTP bit, digital PWM dimming not available).

SPI Interface

General

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV78713 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The NCV78713 SPI transfer size is 16 bits.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCLK) synchronizes shifting and sampling of the information on the two serial data lines: SDO and SDI. The SDO signal is the output from the Slave (NCV78713), and the SDI signal is the output from the Master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple-slave system.

The CSB line is active low. If an NCV78713 is not selected, SDO is in high impedance state and it does not interfere with SPI bus activities. Since the NCV78713 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

The implemented SPI allows connection to multiple slaves by means of star connection (CSB per slave) or by means of daisy chain.

An SPI star connection requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 16 bits per communication.

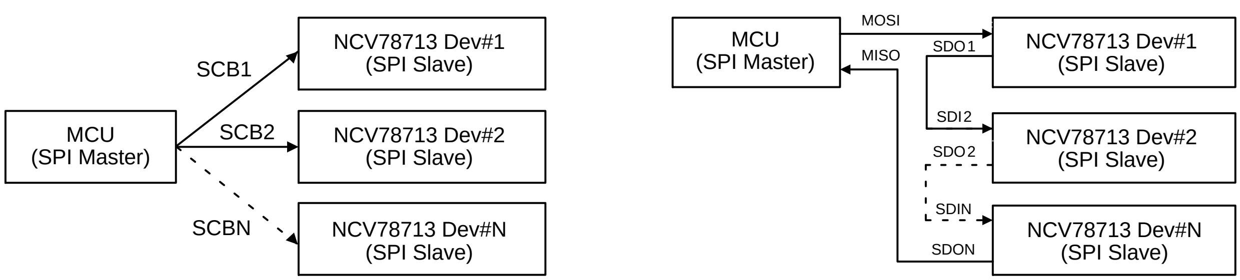


Figure 19. SPI Star vs. Daisy Chain Connection

SPI Daisy Chain Mode

SPI daisy chain connection bus width is always four lines independently on the number of slaves. However, the SPI transfer frame length will be a multiple of the base frame length so N × 16 bits per communication: the data will be interpreted and read in by the devices at the moment the CSB rises.

A diagram showing the data transfer between devices in daisy chain connection is given further: CMDx represents the 16-bit command frame on the data input line transmitted by the Master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

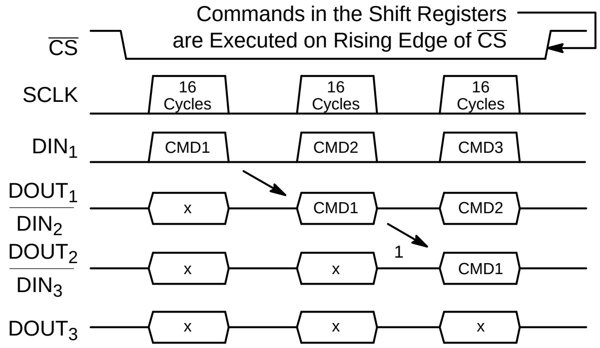


Figure 20. SPI Daisy Chain Data Shift between Slaves. The Symbol 'x' Represents the Previous Content of the SPI Shift Register Buffer

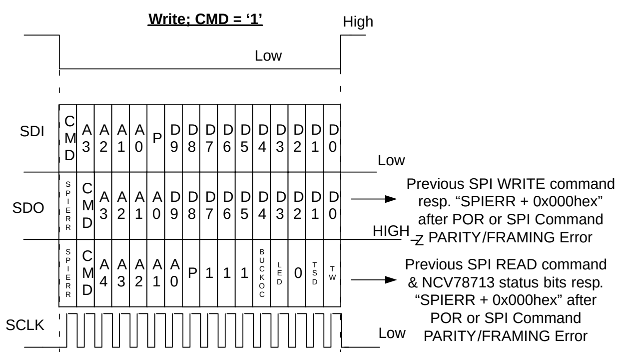
The NCV78713 default power up communication mode is "star". In order to enable daisy chain mode, a multiple of 16 bits clock cycles must be sent to the devices, while the SDI line is left to zero.

NOTE: To come back to star mode the NOP register (address 0x0000) must be written with all ones, with the proper data parity bit and parity framing bit: see SPI protocol for details about parity and write operation.

SPI Transfer Format

Two types of SPI commands (to SDI pin of NCV78713) from the micro controller can be distinguished: "Write to a control register" and "Read from register (control or status)".

The frame protocol for the *write operation*:



P = not (CMD xor A3 xor A2 xor A1 xor A0 xor D9 xor D8 xor D7 xor D6 xor D5 xor D4 xor D3 xor D2 xor D1 xor D0)

Figure 21. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the SDI) is composed from the following fields:

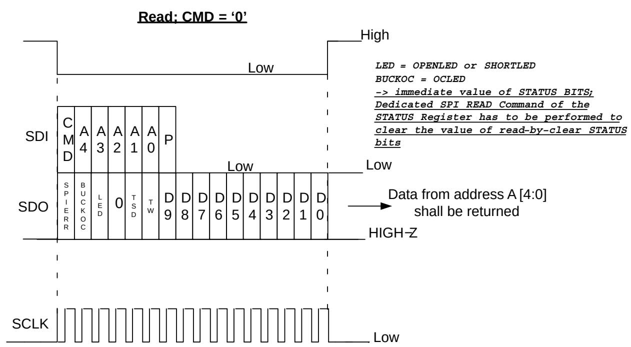
- Bit[15] (MSB): CMD bit = 1 for write operation,
- Bits[14:11]: 4 bits WRITE ADDRESS field,
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame,
- Bits[9:0]: 10 bit DATA to write

Device in the same time replies to the master (on the SDO):

- If the previous command was a write and no SPI error had occurred, a copy of the command, address and data written fields,
- If the previous command was a read, the response frame summarizes the address used and an overall diagnostic check (copy of the main detected errors, see Figures 21 and 22 for details),
- In case of previous SPI error or after power-on-reset, only the MSB bit will be 1, followed by zeros.

If parity bit in the frame is wrong, device will not perform command and <SPI> flag will be set.

The frame protocol for the *read operation*:



P = not (CMD xor A4 xor A3 xor A2 xor A1 xor A0)

Figure 22. SPI Read Frame

Referring to the previous picture, the read frame coming from the master (into the SDI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 0 for read operation,
- Bits[14:10]: 5 bits READ ADDRESS field,
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame,
- Bits [8:0]: 9 bits zeroes field.

Device in the same frame provides to the master (on the SDO) data from the required address (in frame response), thus achieving the lowest communication latency.

SPI Framing and Parity Error

SPI communication framing error is detected by the NCV78713 in the following situations:

- Not an integer multiple of 16 CLK pulses are received during the active-low CSB signal;
- LSB bits (8..0) of a read command are not all zero;
- SPI parity errors, either on write or read operation.

Once an SPI error occurs, the <SPI> flag can be reset only by reading the status register in which it is contained (using in the read frame the right communication parity bit).

SPI ADDRESS MAP

Table 9. NCV78713 SPI ADDRESS MAP

ADDR	R/W	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	NA	NOP Register (Read/Write Operation Ignored)									
0x01	R/W	0x0		0x0							
0x02	R/W	BUCK_ISENS_THR[1:0]		BUCK_VTHR[7:0]							
0x03	R/W	0x0					BUCK_TOFF[4:0]				
0x04	R/W	0x0			BUCK_OC_OCCMP_ THR[1:0]		FSO_MD[2:0]			0x0	BUCK_EN
0x05	R/W	0x0	BUCK_ TSD_AUT_ RCVR_EN	THERMAL_WARNING_THR[7:0]							
0x06	R/W	VTEMP_OFF_ COMP ODD PAR.*	LED_SEL_DUR[8:0]								
0x07	R/W	VTEMP_OFF_COMP[2:0]*			0x0						
0x08	R/W	VTEMP_OFF_COMP[5:3]*			BUCK_ISENS_TRIM[6:0]						
0x09	R/W	0x0		ADC_VLED_RNG_ SEL[1:0]		OTP_BIAS_H	OTP_BIAS_L	OTP_ADDR[1:0]		OTP_OPERATION[1:0]	
0x0A	R	0x0	ODD PARITY	0x0							
0x0B	R	0x0	ODD PARITY	VLEDON[7:0]							
0x0C	R	0x0	ODD PARITY	0x0							
0x0D	R	0x0	ODD PARITY	VLED[7:0]							
0x0E	R	0x0	ODD PARITY	VTEMP[7:0]							
0x0F	R	0x0	ODD PARITY	VBOOST[7:0]							
0x10	R	0x0	ODD PARITY	VDD[7:0]							
0x11	R	0x0	ODD PARITY	0x0							
0x12	R	0x0	ODD PARITY	BUCK_TON_DUR[7:0]							
0x13	R	0x0	ODD PARITY	0x0		0x0	0x0	0x0	OPENLED	SHORTLED	OCLED
0x14	R	0x0	ODD PARITY	OTP_FAIL	FSO	HWR	0x0	LEDVAL	SPIERR	TSD	TW
0x15	R	0x0	ODD PARITY	0x0			OTP_ ACTIVE	0x0	BUCK_ MIN_TON	0x0	BUCK_ STATUS
0x16	R	0x0	ODD PARITY	0x0	0x0						
0x17	R	0x0	ODD PARITY	0x0	BUCK_ISENS_RNG[6:0]						
0x18	R	0x0	ODD PARITY	BUCK_ISENS_D1[3:0]				0x0			
0x19	R	0x0	ODD PARITY	BUCK_ISENS_D2[3:0]				0x0			
0x1A	R	0x0	ODD PARITY	BUCK_ISENS_D3[3:0]				0x0			
0x1B	R	0x0	ODD PARITY	BUCK_ISENS_TC1[3:0]				BUCK_ISENS_TC0[3:0]			
0x1C	R	0x0	ODD PARITY	BUCK_ISENS_TC3[3:0]				BUCK_ISENS_TC2[3:0]			
0x1D	R	0x0	ODD PARITY	0x0							
0x1E	R	OTP_DATA[9:0]									
0x1F	R	0x0		REVID[7:0]							
OTHER	R	0x0									

*Read Only

Table 10. BIT DEFINITION

Symbol	MAP Position	Description
REGISTER 0X00 (CR): NOP REGISTER, RESET VALUE (POR) = 0000000000_2		
NOP	Bits [9:0] – ADDR_0x00	NOP Register (Read/Write Operation Ignored)
REGISTER 0X01 (CR): NOP REGISTER, RESET VALUE (POR) = 0000000000_2		
NOP	Bits [9:0] – ADDR_0x01	NOP Register (Read/Write Operation Ignored)
REGISTER 0X02 (CR): BUCK PEAK CURRENT SETTINGS, RESET VALUE (POR) = 0000000000_2		
BUCK_ISENS_THR[1:0]	Bits [9:8] – ADDR_0x02	Peak Current: Selection of the Range 1, 2, 3 or 4
BUCK_VTHR[7:0]	Bits [7:0] – ADDR_0x02	Peak Current Comparator Threshold Value
REGISTER 0X03 (CR): BUCK TOFF SETTINGS, RESET VALUE (POR) = 0000000000_2		
BUCK_TOFF[4:0]	Bits [4:0] – ADDR_0x03	Buck TOFF·VLED Constant Settings
REGISTER 0X04 (CR): BUCK SETTINGS, RESET VALUE (POR) = 0000000000_2		
BUCK_OC_OCCMP_THR[1:0]	Bits [6:5] – ADDR_0x04	Overcurrent Detection Settings
FSO_MD[2:0]	Bits [4:2] – ADDR_0x04	FSO Mode Selection
BUCK_EN	Bit 0 – ADDR_0x04	Buck Regulator Enable Bit
REGISTER 0X05 (CR): BUCK SETTINGS, RESET VALUE (POR) = 0010110011_2		
BUCK_TSD_AUT_RCVR_EN	Bit 8 – ADDR_0x05	Buck Automatic Recovery after TSD
THERMAL_WARNING_THR[7:0]	Bits [7:0] – ADDR_0x05	Thermal Warning Threshold Settings
REGISTER 0X06 (CR): BUCK SETTINGS, RESET VALUE (POR) = $X000000000_2$		
VTEMP_OFF_COMP ODD PAR.	Bit 9 – ADDR_0x06	ADC VTEMP Trimming Parity Bit
LED_SEL_DUR[8:0]	Bits [8:0] – ADDR_0x06	VLED Measurement Settings
REGISTER 0X07 (CR): BUCK SETTINGS, RESET VALUE (POR) = $XXX0000000_2$		
VTEMP_OFF_COMP[2:0]	Bits [9:7] – ADDR_0x07	ADC VTEMP Trimming
REGISTER 0X08 (CR): BUCK SETTINGS, RESET VALUE (POR) = $XXX0000000_2$		
VTEMP_OFF_COMP[5:3]	Bits [9:7] – ADDR_0x08	ADC VTEMP Trimming
BUCK_ISENS_TRIM[6:0]	Bits [6:0] – ADDR_0x08	Compensation of the Buck Peak Current
REGISTER 0X09 (CR): BUCK SETTINGS, RESET VALUE (POR) = 0000000000_2		
ADC_VLED_RNG_SEL[1:0]	Bits [7:6] – ADDR_0x09	Range Select for VLED ADC
OTP_BIAS_H	Bit 5 – ADDR_0x09	OTP Bias High
OTP_BIAS_L	Bit 4 – ADDR_0x09	OTP Bias Low
OTP_ADDR[1:0]	Bits [3:2] – ADDR_0x09	OTP Address
OTP_OPERATION[1:0]	Bits [1:0] – ADDR_0x09	OTP Operation
REGISTER 0X0B (SR): VLEDON, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x0B	Odd Parity over Data
VLEDON[7:0]	Bits [7:0] – ADDR_0x0B	Output of VLED ADC
REGISTER 0X0D (SR): VLED, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x0D	Odd Parity over Data
VLED[7:0]	Bits [7:0] – ADDR_0x0D	Output of VLED ADC
REGISTER 0X0E (SR): VTEMP, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x0E	Odd Parity over Data
VTEMP[7:0]	Bits [7:0] – ADDR_0x0E	Output of VTEMP ADC
REGISTER 0X0F (SR): VBOOST, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x0F	Odd Parity over Data
VBOOST[7:0]	Bits [7:0] – ADDR_0x0F	Output of VBOOST ADC
REGISTER 0X10 (SR): VDD, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x10	Odd Parity over Data
VDD[7:0]	Bits [7:0] – ADDR_0x10	Output of VDD ADC

Table 10. BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0X12 (SR): BUCK_TON_DUR, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x12	Odd Parity over Data
BUCK_TON_DUR[7:0]	Bits [7:0] – ADDR_0x12	Buck Ton Duration
REGISTER 0X13 (SR): BUCK DIAGNOSTICS, RESET VALUE (POR) = $0X000000X0_2$		
ODD PARITY	Bit 8 – ADDR_0x13	Odd Parity over Data
OPENLED	Bit 2 – ADDR_0x13	Buck Open LED Flag, Latched
SHORTLED	Bit 1 – ADDR_0x13	Buck Short LED Flag, Non-Latched
OCLED	Bit 0 – ADDR_0x13	Buck Overcurrent Flag, Latched
REGISTER 0X14 (SR): BUCK DIAGNOSTICS, RESET VALUE (POR) = $0X0010XXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x14	Odd Parity over Data
OTP_FAIL	Bit 7 – ADDR_0x14	OTP Failure Flag, Latched
FSO	Bit 6 – ADDR_0x14	Chip being in FSO Mode Flag, Non-Latched
HWR	Bit 5 – ADDR_0x14	Hardware Reset Flag, Latched
LEDVAL	Bit 3 – ADDR_0x14	Actual Status of LEDCTRL Pin, Non-Latched
SPIERR	Bit 2 – ADDR_0x14	SPI Error Flag, Latched
TSD	Bit 1 – ADDR_0x14	Thermal Shutdown Flag, Latched
TW	Bit 0 – ADDR_0x14	Thermal Warning Flag, Latched
REGISTER 0X15 (SR): BUCK DIAGNOSTICS, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x15	Odd Parity over Data
OTP_ACTIVE	Bit 4 – ADDR_0x15	OTP Active Flag, Non-Latched
BUCK_MIN_TON	Bit 2 – ADDR_0x15	Minimal Ton Detected on Buck, Latched
BUCK_STATUS	Bit 0 – ADDR_0x15	Actual Status of Buck Regulator, Non-Latched
REGISTER 0X17: BUCK TRIMMING, RESET VALUE (POR) = $0X0XXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x17	Odd Parity over Data
BUCK_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x17	Trimming Constant for Highest Range on Hot for Buck Peak Current
REGISTER 0X18: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x18	Odd Parity over Data
BUCK_ISENS_D1[3:0]	Bits [7:4] – ADDR_0x18	Delta Trimming Constant for Buck Peak Current
REGISTER 0X19: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x19	Odd Parity over Data
BUCK_ISENS_D2[3:0]	Bits [7:4] – ADDR_0x19	Delta Trimming Constant for Buck Peak Current
REGISTER 0X1A: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1A	Odd Parity over Data
BUCK_ISENS_D3[3:0]	Bits [7:4] – ADDR_0x1A	Delta Trimming Constant for Buck Peak Current
REGISTER 0X1B: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1B	Odd Parity over Data
BUCK_ISENS_TC1[3:0]	Bits [7:4] – ADDR_0x1B	Temperature Coefficient Trimming Constant for Buck Peak Current
BUCK_ISENS_TC0[3:0]	Bits [3:0] – ADDR_0x1B	Temperature Coefficient Trimming Constant for Buck Peak Current
REGISTER 0X1C: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1C	Odd Parity over Data
BUCK_ISENS_TC3[3:0]	Bits [7:4] – ADDR_0x1C	Temperature Coefficient Trimming Constant for Buck Peak Current
BUCK_ISENS_TC2[3:0]	Bits [3:0] – ADDR_0x1C	Temperature Coefficient Trimming Constant for Buck Peak Current

Table 10. BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0X1E: OTP DATA, RESET VALUE (POR) = 0000000000_2		
OTP_DATA[9:0]	Bits [9:0] – ADDR_0x1E	OTP Data
REGISTER 0X1F: REVID, RESET VALUE (POR) = $00000XXXXXXX_2$		
REVID[7:0]	Bits [7:0] – ADDR_0x1F	Revision ID

POR values of status registers are shown in situation that FSO mode is not entered after POR. All latched flags are “cleared by read”. ‘x’ means that value after reset is defined during reset phase (diagnostics) or is trimmed during manufacturing process.

SPI register SPI_REVID[7:0] is used to track the silicon version, following encoding mechanism is used:

- SPI_REVID[2:0]: Metal Tune <0 to 7>
- SPI_REVID[4:3]: Full Mask Version <0 to 3>
- SPI_REVID[5]: L713/L723 Distinguishing Bit (REVID[5] = 1 means L713)
- SPI_REVID[7:6]: Constant 00 [binary]

First full mask version has SPI_REVID[7:0] = 0x28hex (Full mask = 0x1 & Metal-Tune = 0x0, REVID[5] = 1).

OTP MEMORY

Description

The OTP (Once Time Programmable) memory contains 40 bits which bear the most important application dependant parameters and is user programmable via SPI interface. The programming of these bits is typically done at the end of the module manufacturing line.

OTP memory serves to store configuration data for Fail-Safe or Stand-Alone functionality or default configuration of the chip after power-up.

The OTP bits can be programmed only once, this is ensured by dedicated *OTP Lock Bit* which is set during programming.

Table 11. OTP MAP

OTP Bits	Connection to SPI Register
OTP[7:0]	Not Applicable
OTP[9:8]	Not Applicable
OTP[17:10]	BUCK_VTHR[7:0]
OTP[19:18]	BUCK_ISENS_THR[1:0]
OTP[24:20]	Not Applicable
OTP[29:25]	BUCK_TOFF[4:0]
OTP[30]	Not Applicable
OTP[31]	BUCK_EN
OTP[34:32]	FSO_MD[2:0]
OTP[35]	Not Applicable
OTP[36]	BUCK_TSD_AUT_RCR_EN
OTP[38:37]	BUCK_OC_OCCMP_THR[1:0]
OTP[39]	OTP Lock Bit

The OTP bits addressed by SPI register OTP_ADDR[1:0] are accessible (read only) in the SPI register OTP_DATA[9:0] after OTP Refresh operation (OTP_OPERATION[1:0] = 0x1) in the following way:

OTP_ADDR[1:0] = 0x0: OTP_DATA[9:0] = OTP[9:0]
OTP_ADDR[1:0] = 0x1: OTP_DATA[9:0] = OTP[19:10]
OTP_ADDR[1:0] = 0x2: OTP_DATA[9:0] = OTP[29:20]
OTP_ADDR[1:0] = 0x3: OTP_DATA[9:0] = OTP[39:30]

OTP Operations

The NCV78713 supports following operations with OTP memory:

- OTP_OPERATION[1:0] = 0x0 or 0x3:
  NOP (no operation)
- OTP_OPERATION[1:0] = 0x1:
  OTP Refresh – refresh of the whole OTP memory (40 bits). Data addressed by SPI register OTP_ADDR[1:0] are available in SPI register OTP_DATA[9:0] after the end of OTP Refresh operation
- OTP_OPERATION[1:0] = 0x2:
  OTP Zap – data from SPI register (those listed in Table 11) and *OTP Lock Bit* are programmed into OTP memory. OTP Zap operation is allowed to be performed only once − when *OTP Lock Bit* is unprogrammed

SPI status bit OTP_ACTIVE is set to “log. 1” when an OTP operation is in progress.

OTP Programming Procedure

Following procedure should be applied to program OTP memory:

- VBOOST voltage has to be in range between 15 V and 20 V with current capability at least 50 mA
- VDD voltage has to be kept in range for normal mode operation
- The junction temperature has to stay in range from 0°C to 125°C during OTP programming
- SPI registers listed in Table 11 have to be written with required content
- Content of the SPI registers (those listed in Table 11) is programmed into the OTP memory by OTP_OPERATION[1:0] = 0x2 SPI write command. *OTP Lock Bit* is programmed automatically at the same time to prevent any further OTP programming

OTP Programming Verification

OTP_FAIL bit in the SPI status register is set when VBOOST under-voltage (see OTP_UV parameter) is detected during OTP Zap operation. It is clear by read flag.

The OTP_BIAS_H and OTP_BIAS_L registers are used to check proper OTP programming. After OTP programming, the OTP content has to be the same as programmed when OTP is read with OTP_BIAS_H = 1 and OTP_BIAS_L = 1.

Following procedure should be applied to verify OTP content:

- VDD voltage has to be kept in range for normal mode operation
- Write SPI registers OTP_BIAS_L = 1 and OTP_BIAS_H = 0
- Write SPI register OTP_OPERATION[1:0] = 0x1 (OTP Refresh) for all OTP_ADDR[1:0] values and check corresponding OTP_DATA[9:0] content which has to match with previously programmed data
- Write SPI registers OTP_BIAS_L = 0 and OTP_BIAS_H = 1
- Write SPI register OTP_OPERATION[1:0] = 0x1 (OTP Refresh) for all OTP_ADDR[1:0] values and check corresponding OTP_DATA[9:0] content which has to match with previously programmed data
- Programming is considered as successful when no mismatch is observed

Table 12. ORDERING INFORMATION

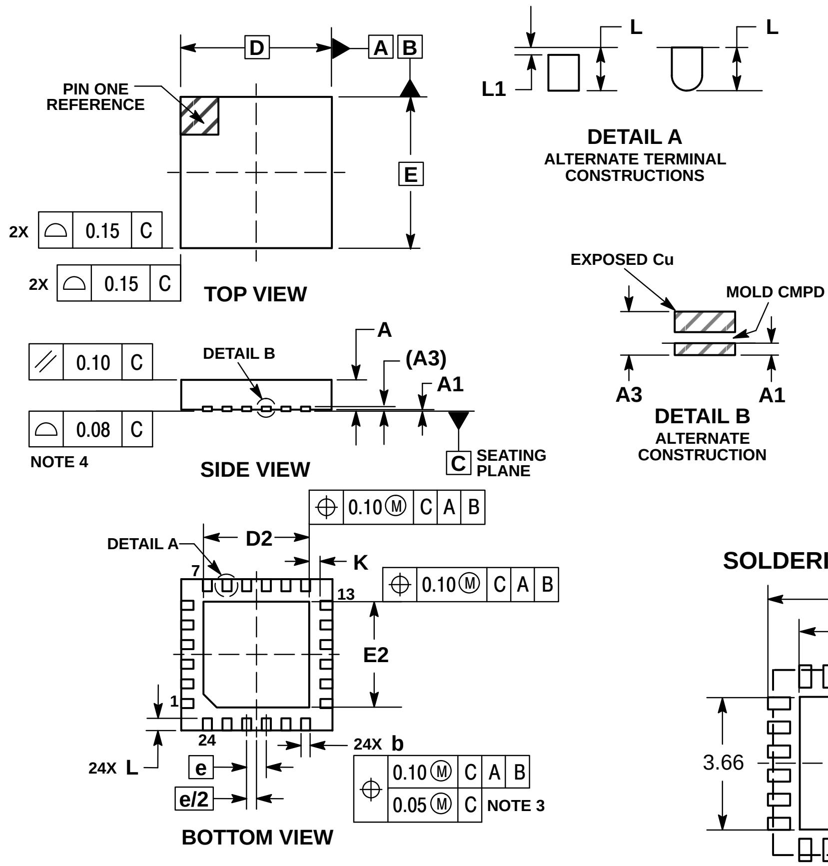
Device	Marking	Package*	Shipping†
NCV78713MW0R2G	N78713−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78713MW0G	N78713−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	60 Units / Tube

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

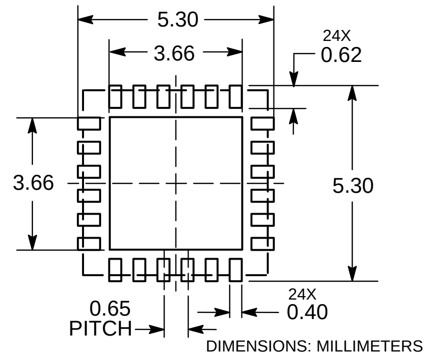
QFN24 5x5, 0.65P
CASE 485CS
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	−−−	0.05
A3	0.20 REF	
b	0.25	0.35
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.65 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	−−−	0.15

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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