SILEGO

SLG7NT4503

GreenPAK 3™

SEQUENCER

General Description

Silego SLG7NT4503 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

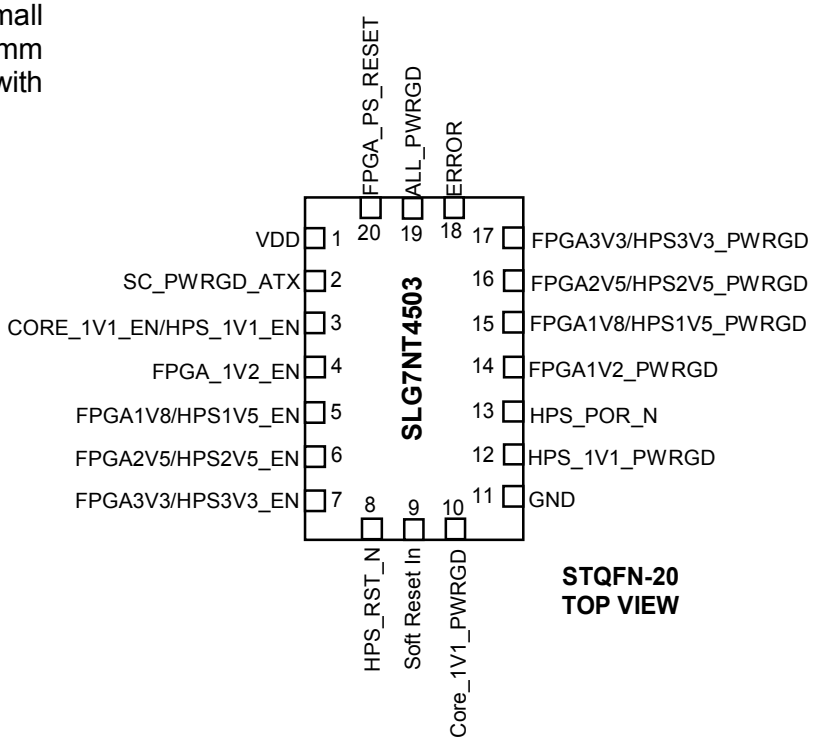
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

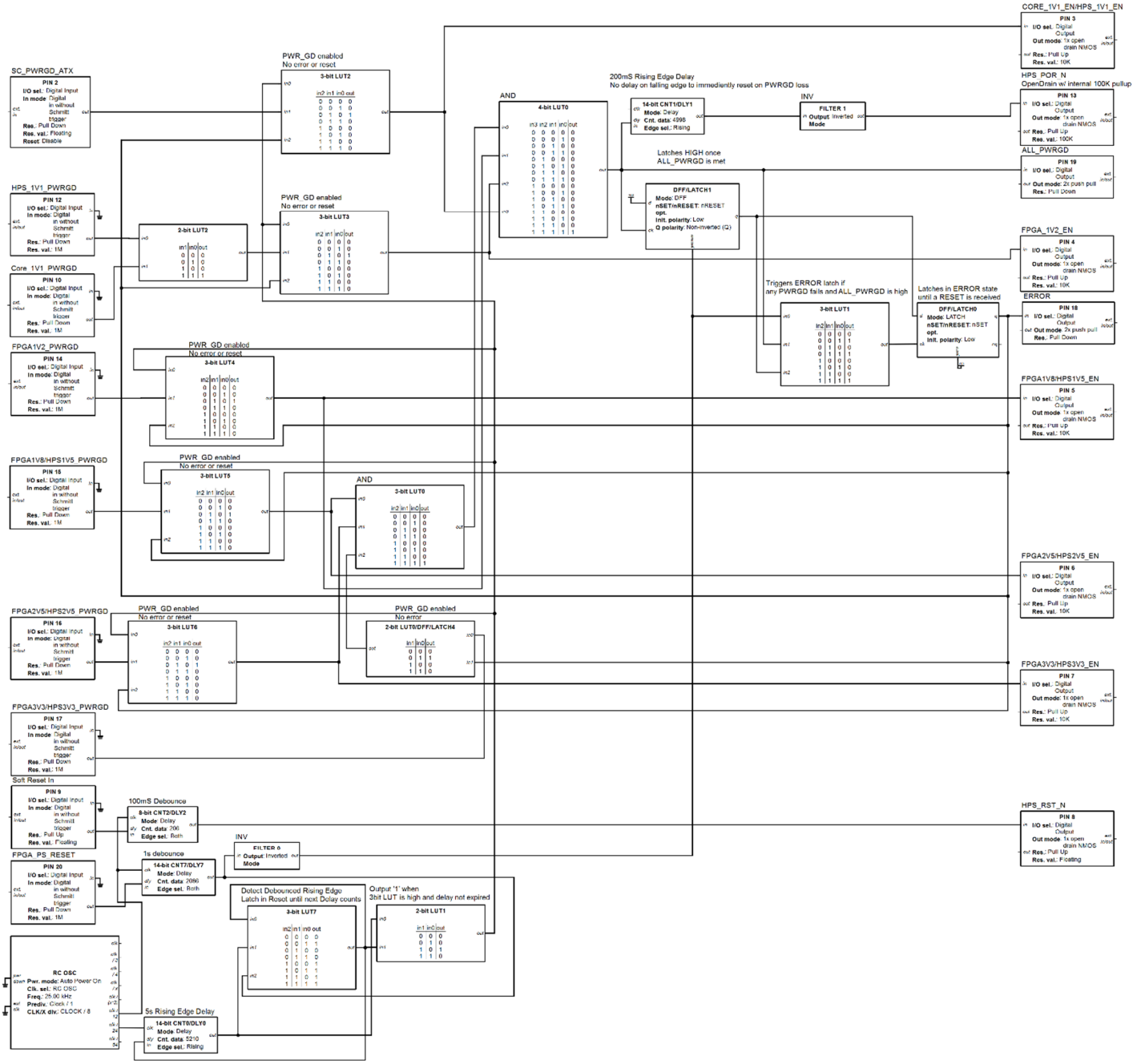
- 2 Outputs — Push Pull 2X
- 7 Outputs — Open Drain NMOS 1X

Pin Configuration



STQFN-20
TOP VIEW

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	SC_PWRGD_ATX	Digital Input	Digital Input without Schmitt trigger
3	CORE_1V1_EN/HPS_1V1_EN	Digital Output	Open Drain NMOS 1X
4	FPGA_1V2_EN	Digital Output	Open Drain NMOS 1X
5	FPGA1V8/HPS1V5_EN	Digital Output	Open Drain NMOS 1X
6	FPGA2V5/HPS2V5_EN	Digital Output	Open Drain NMOS 1X
7	FPGA3V3/HPS3V3_EN	Digital Output	Open Drain NMOS 1X
8	HPS_RST_N	Digital Output	Open Drain NMOS 1X
9	Soft Reset In	Digital Input	Digital Input without Schmitt trigger
10	Core_1V1_PWRGD	Digital Input	Digital Input without Schmitt trigger
11	GND	GND	Ground
12	HPS_1V1_PWRGD	Digital Input	Digital Input without Schmitt trigger
13	HPS_POR_N	Digital Output	Open Drain NMOS 1X
14	FPGA1V2_PWRGD	Digital Input	Digital Input without Schmitt trigger
15	FPGA1V8/HPS1V5_PWRGD	Digital Input	Digital Input without Schmitt trigger
16	FPGA2V5/HPS2V5_PWRGD	Digital Input	Digital Input without Schmitt trigger
17	FPGA3V3/HPS3V3_PWRGD	Digital Input	Digital Input without Schmitt trigger
18	ERROR	Digital Output	Push Pull 2X
19	ALL_PWRGD	Digital Output	Push Pull 2X
20	FPGA_PS_RESET	Digital Input	Digital Input without Schmitt trigger

Ordering Information

Part Number	Package Type
SLG7NT4503V	V=STQFN-20
SLG7NT4503VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	1400	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=3.3V	1.78	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	--	--	1.21	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull, I_{OH} = 3mA, 2X Driver, at VDD=3.3 V	2.87	3.21	--	V
V_{OL}	LOW-Level Output Voltage	Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	V
		Push Pull, I_{OL} = 3mA, 2X Driver, at VDD=3.3 V	--	0.060	0.108	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	11.522	24.16	--	mA
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V	9.750	16.488	--	mA
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.37	--	
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 3, 4, 5, 6, 7	7	10	13	kΩ
		Pull up on PIN 13	70	100	130	
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 10, 12, 14, 15, 16, 17, 20	700	1000	1300	kΩ

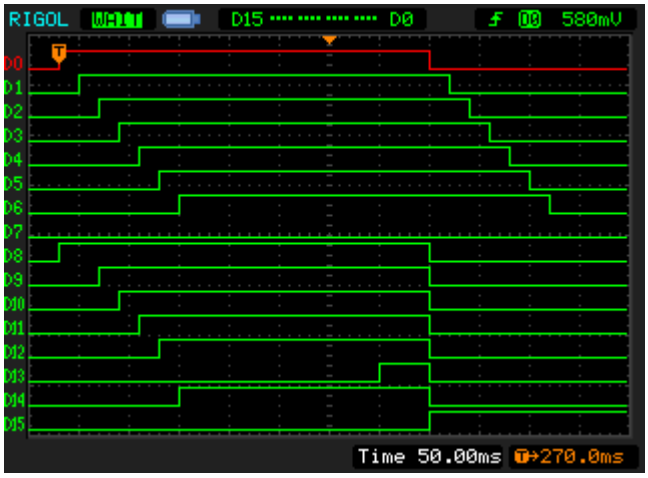
T_{DLY0}	Delay0 Time	At temperature 25°C	4.86	5	5.16	s
		At temperature -20°C +45°C (note 1)	4.59	5	5.85	
T_{DLY1}	Delay1 Time	At temperature 25°C	194.68	200.02	205.73	ms
		At temperature -20°C +45°C (note 1)	183.68	200.02	233.33	
T_{DLY2}	Delay2 Time	At temperature 25°C	97.18	100.08	103.18	ms
		At temperature -20°C +45°C (note 1)	91.69	100.08	117.02	
T_{DLY7}	Delay7 Time	At temperature 25°C	975.6	1002.48	1031.19	ms
		At temperature -20°C +45°C (note 1)	920.5	1002.48	1169.55	
T_{SU}	Start up Time	From VDD rising past 1.6V	--	1	--	ms

1. Guaranteed by Design.

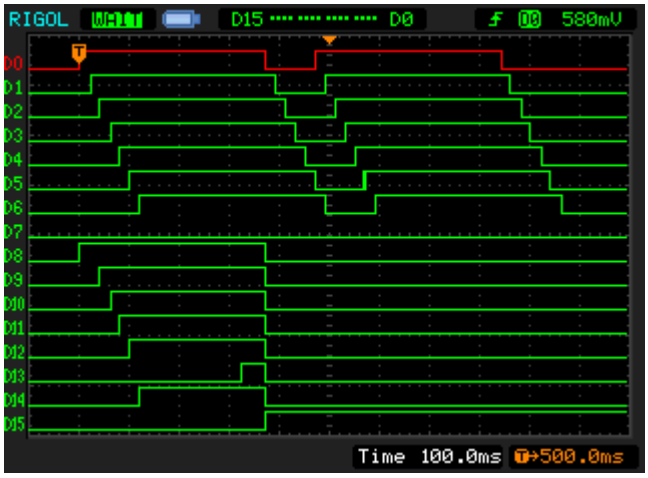
Functionality Waveforms

D0 – PIN#2 (SC_PWRGD_ATX)
D1 – PIN#10 (Core_1V1_PWRGD)
D2 – PIN#12 (HPS_1V1_PWRGD)
D3 – PIN#14 (FPGA1V2_PWRGD)
D4 – PIN#15 (FPGA1V8/HPS1V5_PWRGD)
D5 – PIN#16 (FPGA2V5/HPS2V5_PWRGD)
D6 – PIN#17 (FPGA3V3/HPS3V3_PWRGD)
D7 – PIN#20 (FPGA_PS_RESET)
D8 – PIN#3 (CORE_1V1_EN/HPS_1V1_EN)
D9 – PIN#4 (FPGA_1V2_EN)
D10 – PIN#5 (FPGA1V8/HPS1V5_EN)
D11 – PIN#6 (FPGA2V5/HPS2V5_EN)
D12 – PIN#7 (FPGA3V3/HPS3V3_EN)
D13 – PIN#13 (HPS_POR_N)
D14 – PIN#19 (ALL_PWRGD)
D15 – PIN#18 (ERROR)

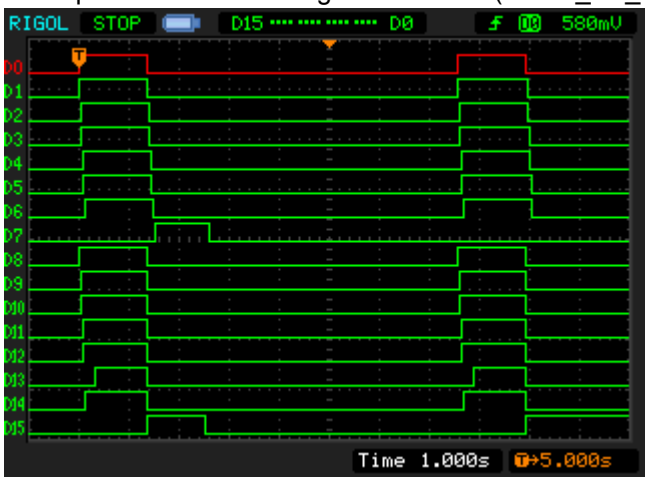
1. Sequencer operation



2. Sequencer after latched reset state operation

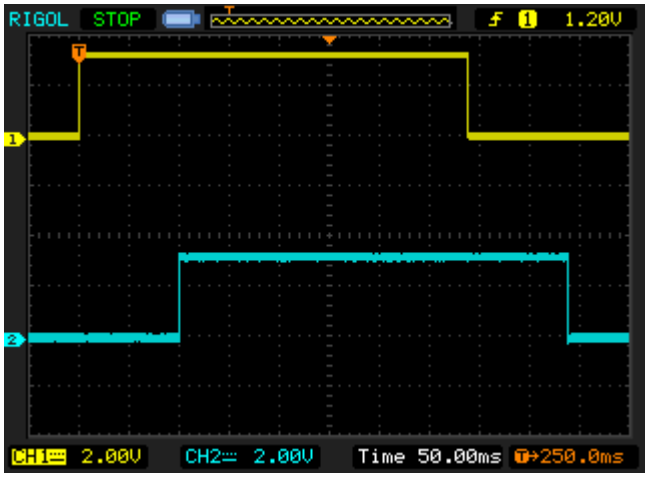


3. Sequencer after reset signal on PIN20 (FPGA_PS_RESET) operation

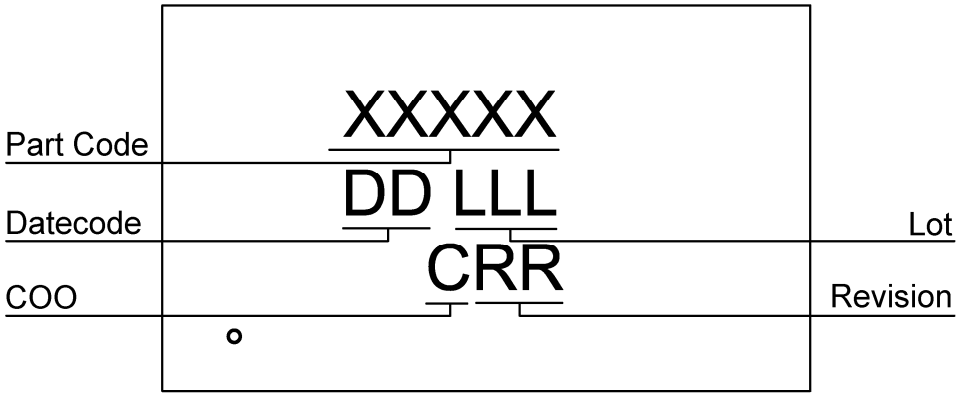


Channel 1 (yellow/top line) – PIN#9 (Soft Reset In)
Channel 2 (light blue/2nd line) – PIN#8 (HPS_RST_N) with external 5kΩ pull up resistor

4. PIN8 (HPS_RST_N) operation



Package Top Marking



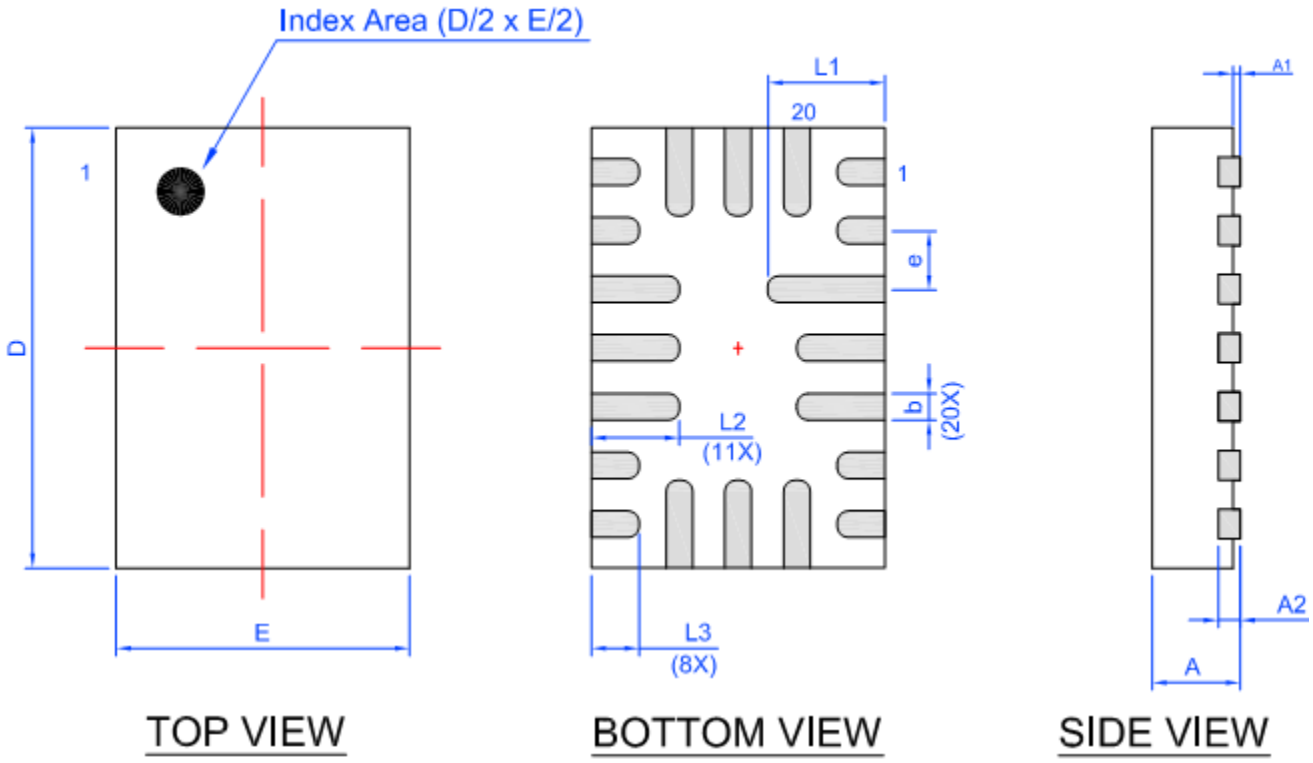
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.11	002	U			08/26/2014

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

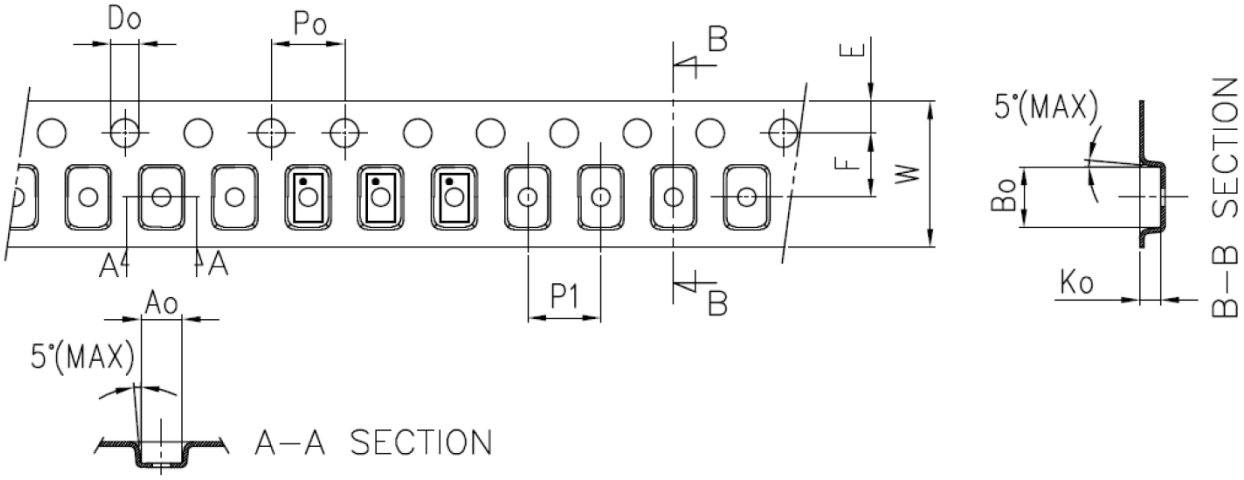
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).
More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
08/18/2014	0.10	New design for SLG46722
08/26/2014	0.11	Removed inverter from HPS_POR_N output

Silego Website & Support

Silego Technology Website
Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:
http://greenpak.silego.com/
http://greenpak2.silego.com/
http://greenpak3.silego.com/
http://greenfet.silego.com/
http://greenfet2.silego.com/
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Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/

Silego Technical Support
Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

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Silego Technology has live training assistance and sales support available at http://www.silego.com/. Please contact us to schedule a 1 on 1 training session with one of our application engineers.

Contact Your Local Sales Representative
Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly
Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL:
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Other Information
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