ES8323S

Low Power Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- 256/384Fs and USB 12/24 MHz system clocks
- Sophisticated analog input and output routing, mixing and gain
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 92 dB signal to noise ratio, -85 dB THD+N
- Auto level control (ALC) and noise gate

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 93 dB signal to noise ratio, -85 dB THD+N
- Headphone driver capless mode
- Bass or treble
- Stereo enhancement
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

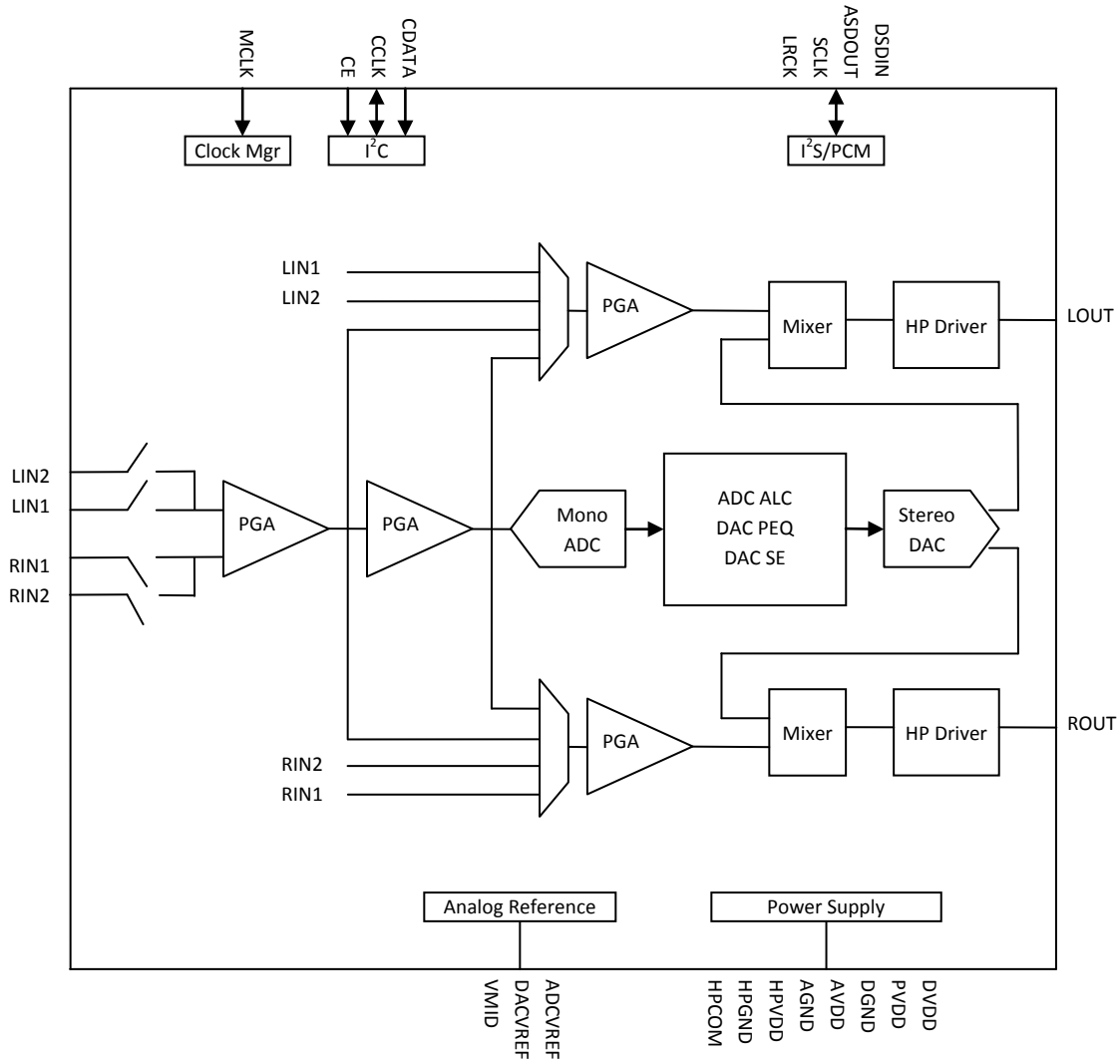
APPLICATIONS

- MID/Tablet
- Portable audio

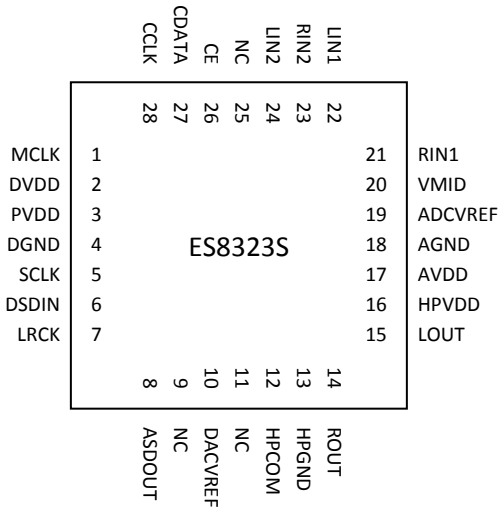
ORDERING INFORMATION

ES8323S -40°C ~ +85°C
QFN-28

1. BLOCK DIAGRAM

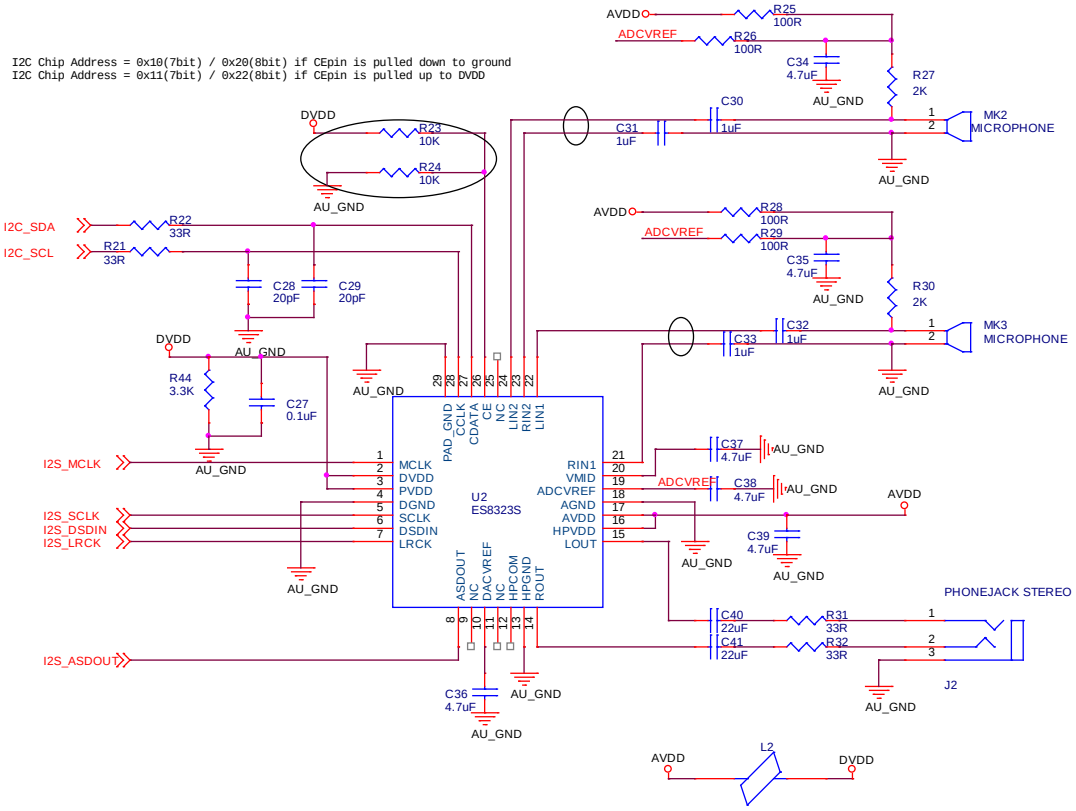


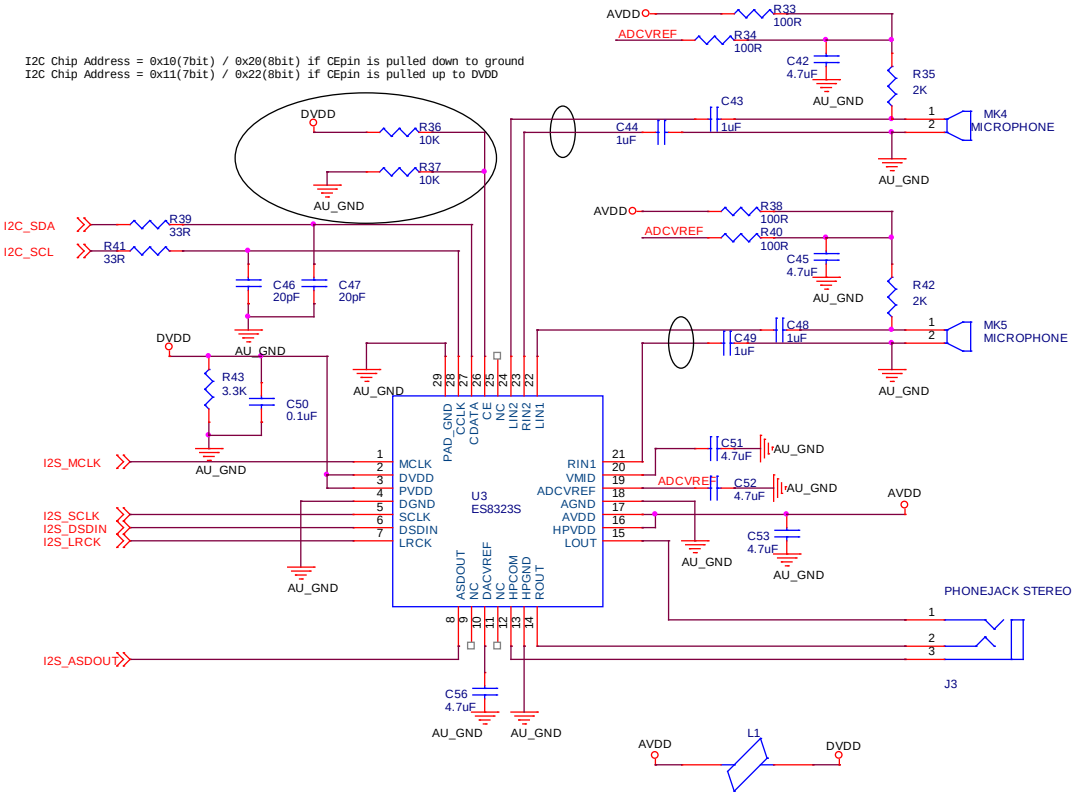
2. PIN OUT AND DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	MCLK	I	Master clock
2	DVDD	Supply	Digital core supply
3	PVDD	Supply	Digital IO supply
4	DGND	Supply	Digital ground
5	SCLK	I/O	Audio data bit clock
6	DSDIN	I	DAC audio data
7	LRCK	I/O	Audio data left and right clock
8	ASDOUT	O	ADC audio data
9	NC		No connect
10	DACVREF	O	Decoupling capacitor
11	NC		No connect
12	HPCOM	O	No connect or bias for capless mode
13	HPGND	Supply	Ground for headphone output drivers
14	ROUT	O	Right analog output
15	LOUT	O	Left analog output
16	HPVDD	Supply	Supply for headphone output drivers
17	AVDD	Supply	Analog supply
18	AGND	Supply	Analog ground
19	ADCVREF	O	Decoupling capacitor
20	VMID	O	Decoupling capacitor
21	RIN1	I	Right analog input
22	LIN1	I	Left analog input
23	RIN2	I	Right analog input
24	LIN2	I	Left analog input
25	NC		No connect
26	CE	I	I^2C device address selection
27	CDATA	I/O	I^2C data input or output
28	CCLK	I	I^2C clock input

3. TYPICAL APPLICATION CIRCUIT





4. POWER ON RESET

The device resets itself when DVDD (pin 2) ramp from ground voltage to supply voltage. The ground voltage needs to be less than 0.2V for proper reset. When DVDD voltage is removed, it is important to let it drop below 0.2V before next power up. An optional discharge resistor (3.3K, for example) can be placed between DVDD and DGND (pin 4).

5. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports two types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), and USB clocks (12/24 MHz).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with specific rates. The device can auto detect MCLK/LRCK ratio according to Table 1. The device supports the MCLK/LRCK ratios listed in Table 1. The LRCK/SCLK ratio is normally 64.

Table 1 Slave Mode Sampling Frequencies and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	50kHz – 100kHz	128, 192, 256, 384, 512

In master mode, LRCK and SCLK are derived internally from MCLK. The available MCLK/LRCK ratios and SCLK/LRCK ratios are listed in Table 2.

Table 2 Master Mode Sampling Frequencies and MCLK/LRCK Ratio

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC Sample Rate (ALRCK)	ADCFsRatio [4:0]	DAC Sample Rate (DLRCK)	DACFsRatio [4:0]	SCLK Ratio
Normal Mode						
12.288 MHz	24.576MHz	8 kHz (MCLK/1536)	01010	8 kHz (MCLK/1536)	01010	MCLK/6
		8 kHz (MCLK/1536)	01010	48 kHz (MCLK/256)	00010	MCLK/4
		12 kHz (MCLK/1024)	00111	12 kHz (MCLK/1024)	00111	MCLK/4
		16 kHz (MCLK/768)	00110	16 kHz (MCLK/768)	00110	MCLK/6
		24 kHz (MCLK/512)	00100	24 kHz (MCLK/512)	00100	MCLK/4
		32 kHz (MCLK/384)	00011	32 kHz (MCLK/384)	00011	MCLK/6
		48 kHz (MCLK/256)	00010	8 kHz (MCLK/1536)	01010	MCLK/4
		48 kHz (MCLK/256)	00010	48 kHz (MCLK/256)	00010	MCLK/4
		96 kHz (MCLK/128)	00000	96 kHz (MCLK/128)	00000	MCLK/2
11.2896 MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	01001	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		8.0182 kHz (MCLK/1408)	01001	44.1 kHz (MCLK/256)	00010	MCLK/4
		11.025 kHz (MCLK/1024)	00111	11.025 kHz (MCLK/1024)	00111	MCLK/4

		22.05 kHz (MCLK/512)	00100	22.05 kHz (MCLK/512)	00100	MCLK/4
		44.1 kHz (MCLK/256)	00010	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		44.1 kHz (MCLK/256)	00010	44.1 kHz (MCLK/256)	00010	MCLK/4
		88.2 kHz (MCLK/128)	00000	88.2 kHz (MCLK/128)	00000	MCLK/2
18.432 MHz	36.864MHz	8 kHz (MCLK/2304)	01100	8 kHz (MCLK/2304)	01100	MCLK/6
		8 kHz (MCLK/2304)	01100	48 kHz (MCLK/384)	00011	MCLK/6
		12 kHz (MCLK/1536)	01010	12 kHz (MCLK/1536)	01010	MCLK/6
		16 kHz (MCLK/1152)	01000	16 kHz (MCLK/1152)	01000	MCLK/6
		24 kHz (MCLK/768)	00110	24 kHz (MCLK/768)	00110	MCLK/6
		32 kHz (MCLK/576)	00101	32 kHz (MCLK/576)	00101	MCLK/6
		48 kHz (MCLK/384)	00011	8 kHz (MCLK/2304)	01100	MCLK/6
		48 kHz (MCLK/384)	00011	48 kHz (MCLK/384)	00011	MCLK/6
		96 kHz (MCLK/192)	00001	96 kHz (MCLK/192)	00001	MCLK/3
16.9344 MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	01011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		8.0182 kHz (MCLK/2112)	01011	44.1 kHz (MCLK/384)	00011	MCLK/6
		11.025 kHz (MCLK/1536)	01010	11.025 kHz (MCLK/1536)	01010	MCLK/6
		22.05 kHz (MCLK/768)	00110	22.05 kHz (MCLK/768)	00110	MCLK/6
		44.1 kHz (MCLK/384)	00011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		44.1 kHz (MCLK/384)	00011	44.1 kHz (MCLK/384)	00011	MCLK/6
		88.2 kHz (MCLK/192)	00001	88.2 kHz (MCLK/192)	00001	MCLK/3
USB Mode						
12 MHz	24MHz	8 kHz (MCLK/1500)	11011	8 kHz (MCLK/1500)	11011	MCLK
		8 kHz (MCLK/1500)	11011	48 kHz (MCLK/250)	10010	MCLK
		8.0214 kHz (MCLK/1496)	11010	8.0214 kHz (MCLK/1496)	11010	MCLK
		8.0214 kHz (MCLK/1496)	11010	44.118 kHz (MCLK/272)	10011	MCLK
		11.0259 kHz (MCLK/1088)	11001	11.0259 kHz (MCLK/1088)	11001	MCLK
		12 kHz (MCLK/1000)	11000	12 kHz (MCLK/1000)	11000	MCLK
		16 kHz (MCLK/750)	10111	16 kHz (MCLK/750)	10111	MCLK
		22.0588 kHz (MCLK/544)	10110	22.0588 kHz (MCLK/544)	10110	MCLK
		24 kHz (MCLK/500)	10101	24 kHz (MCLK/500)	10101	MCLK
		32 kHz (MCLK/375)	10100*	32 kHz (MCLK/375)	10100*	MCLK
		44.118 kHz (MCLK/272)	10011	8.0214 kHz (MCLK/1496)	11010	MCLK
		44.118 kHz (MCLK/272)	10011	44.118 kHz (MCLK/272)	10011	MCLK
		48 kHz (MCLK/250)	10010	8 kHz (MCLK/1500)	11011	MCLK
		48 kHz (MCLK/250)	10010	48 kHz (MCLK/250)	10010	MCLK
		88.235 kHz (MCLK/136)	10001	88.235 kHz (MCLK/136)	10001	MCLK
		96 kHz (MCLK/125)	10000	96 kHz (MCLK/125)	10000	MCLK

6. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-

byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a "start" signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I^2C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 3 Write Data to Register in I^2C Interface Mode

	Chip Address		R/W		Register Address		Data to be written		
start	001000	AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

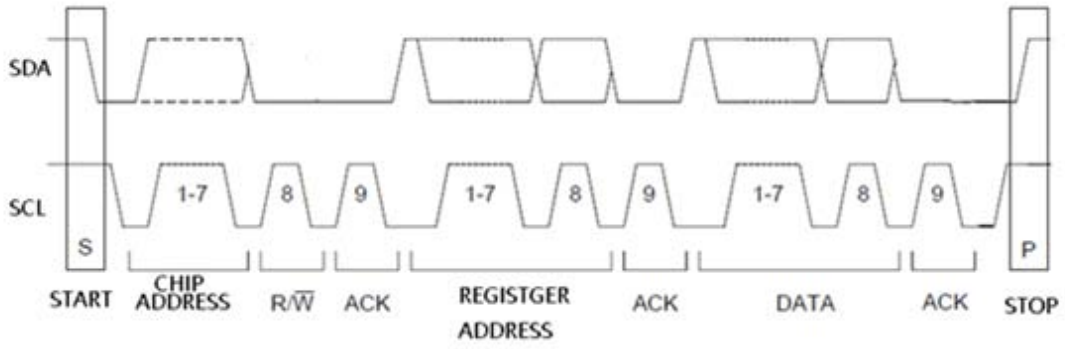


Figure 1a I^2C Write Timing

Table 4 Read Data from Register in I^2C Interface Mode

	Chip Address		R/W		Register Address		
Start	001000	AD0	0	ACK	RAM	ACK	
	Chip Address		R/W		Data to be read		
Start	001000	AD0	1	ACK	Data	NACK	Stop

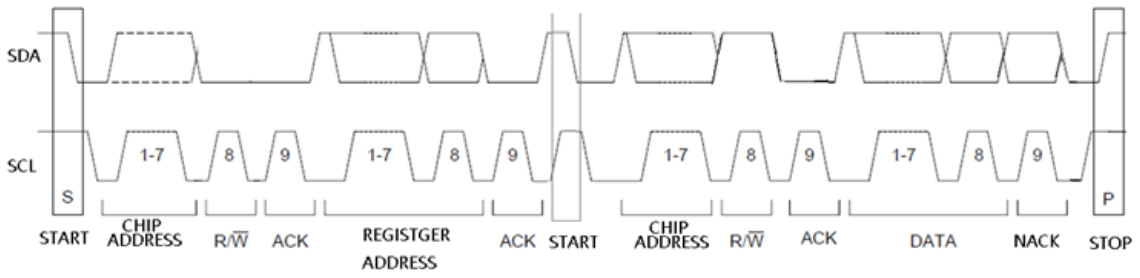


Figure 1b I²C Read Timing

7. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I²S, left justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 5.

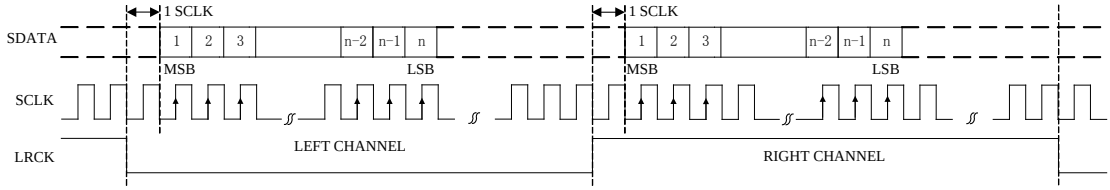


Figure 2 I²S Serial Audio Data Format Up To 24-bit

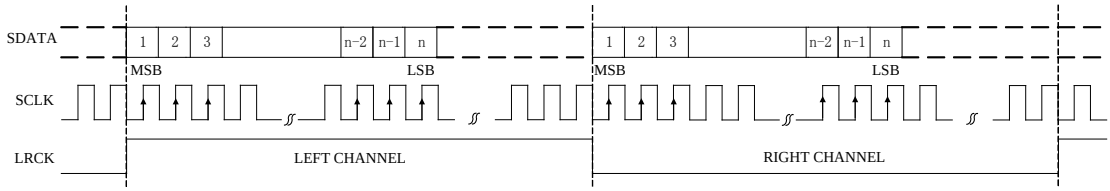


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

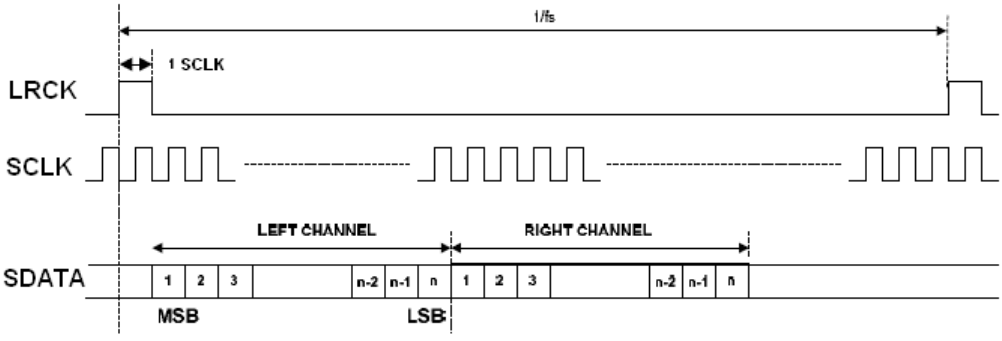


Figure 4 DSP/PCM Mode A

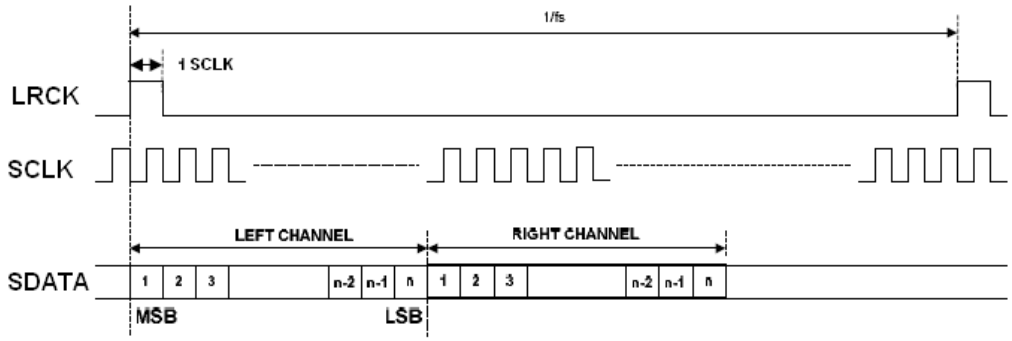


Figure 5 DSP/PCM Mode B

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.0V
Digital Supply Voltage Level	-0.3V	+5.0V
Input Voltage Range	DGND-0.3V	DVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage Level	2.0	3.3	3.6	V
Digital Supply Voltage Level	1.6	1.8	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	85	92	95	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%

Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		20		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	83	93	95	dB
THD+N	-85	-83	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	40			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz Fs = 44.1KHz Fs = 48KHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V:				mW

Play back Play back and record DVDD=3.3V, PVDD=3.3V, AVDD=3.3V: Play back Play back and record		7 16 31 59		
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		TBD TBD		mW

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

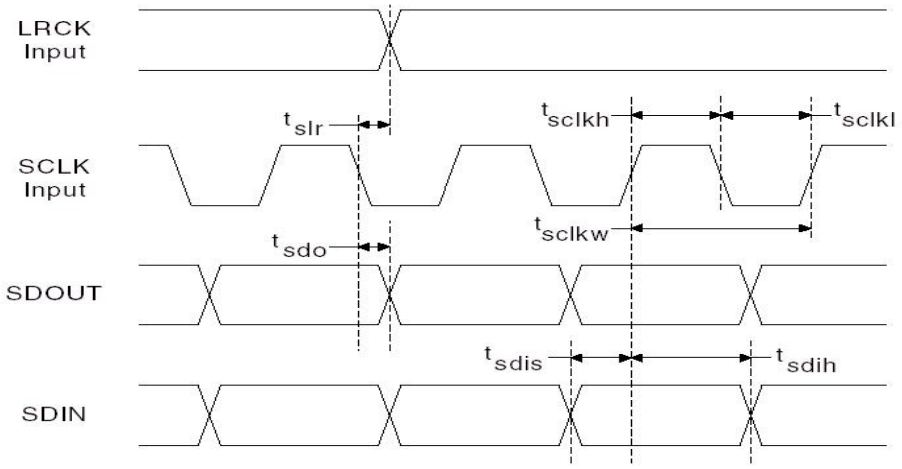


Figure 8 Serial Audio Port Timing

I^2C SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
SCL Clock Frequency	FSCL		400	KHz
Bus Free Time Between Transmissions	TTWID	1.3		us
Start Condition Hold Time	TTWSTH	0.6		us
Clock Low time	TTWCL	1.3		us

Clock High Time	TTWCH	0.4		us
Setup Time for Repeated Start Condition	TTWSTS	0.6		us
SDA Hold Time from SCL Falling	TTWDH		900	ns
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		300	ns
Fall Time SCL	TTWF		300	ns

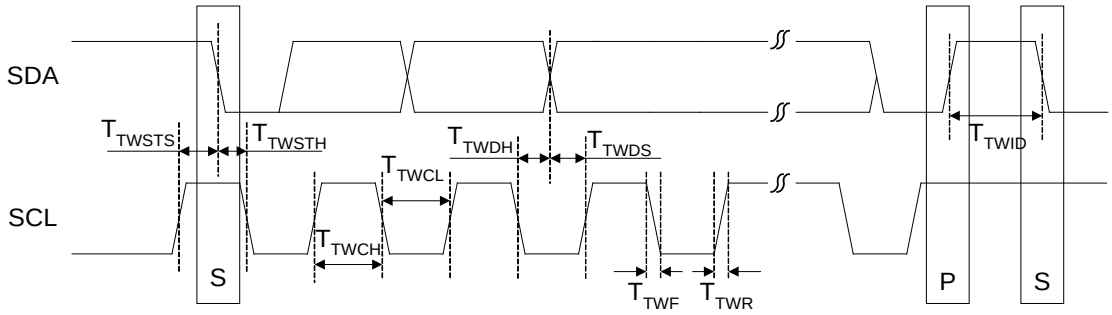


Figure 10 I^2C Timing

9. CONFIGURATION REGISTER DEFINITION

REGISTER 0 – CHIP CONTROL 1, DEFAULT 0000 0100

Bit Name	Bit	Description
SCPReset	7	0 – normal (default) 1 – reset control port register to default
LRCM	6	0 – ALRCK disabled when both ADC disabled; DLRCK disabled when both DAC disabled (default) 1 – ALRCK and DLRCK disabled when all ADC and DAC disabled
DACMCLK	5	0 – when SameFs=1, ADCMCLK is the chip master clock source (default) 1 – when SameFs=1, DACMCLK is the chip master clock source
SameFs	4	0 – ADC Fs differs from DAC Fs (default) 1 – ADC Fs is the same as DAC Fs
SeqEn	3	0 – internal power up sequence disable (default) 1 – internal power up sequence enable
EnRef	2	0 – disable reference 1 – enable reference (default)
VMIDSEL	1:0	00 – Vmid disabled (default) 01 – 50 kΩ divider enabled 10 – 500 kΩ divider enabled 11 – 5 kΩ divider enabled

REGISTER 1 – CHIP CONTROL 2, DEFAULT 0001 1111

Bit Name	Bit	Description
LPVcmMod	5	0 – normal (default) 1 – low power
LPVrefBuf	4	0 – normal 1 – low power (default)
PdnAna	3	0 – normal 1 – entire analog power down (default)
PdnIbiasgen	2	0 – normal 1 – ibiasgen power down (default)
VrefLo	1	0 – normal 1 – low power (default)
PdnVrefbuf	0	0 – normal 1 – power down (default)

REGISTER 2 – CHIP POWER MANAGEMENT, DEFAULT 1100 0011

Bit Name	Bit	Description
adc_DigPDN	7	0 – normal 1 – resets ADC DEM, filter and serial data port (default)
dac_DigPDN	6	0 – normal 1 – resets DAC DSM, DEM, filter and serial data port (default)
adc_stm_rst	5	0 – normal (default) 1 – reset ADC state machine to power down state
dac_stm_rst	4	0 – normal (default) 1 – reset DAC state machine to power down state
adcVref_PDN	1	0 – ADC analog reference power up 1 – ADC analog reference power down (default)
dacVref_PDN	0	0 – DAC analog reference power up 1 – DAC analog reference power down (default)

REGISTER 3 – ADC POWER MANAGEMENT, DEFAULT 1010 1100

Bit Name	Bit	Description
PdnAINL	7	0 – normal 1 – left analog input power down (default)
PdnADCL	5	0 – left ADC power up 1 – left ADC power down (default)
PdnADCBiasgen	2	0 – normal 1 – power down (default)
flashLP	1	0 – normal (default) 1 – ADC low power
intLP	0	0 – normal (default) 1 – low power

REGISTER 4 – DAC POWER MANAGEMENT, DEFAULT 1100 0000

Bit Name	Bit	Description
PdnDACL	7	0 – left DAC power up 1 – left DAC power down (default)
PdnDACR	6	0 – right DAC power up 1 – right DAC power down (default)
HPCOM	5	0 – HPCOM disable (default) 1 – HPCOM enable
LOUT	3	0 – LOUT disabled (default) 1 – LOUT enabled
ROUT	2	0 – ROUT disabled (default) 1 – ROUT enabled

REGISTER 5 – CHIP LOW POWER 1, DEFAULT 0000 0000

Bit Name	Bit	Description
LPDACL	7	0 – normal (default) 1 – low power
LPDACR	6	0 – normal (default) 1 – low power
LPHPCOM	5	0 – normal (default) 1 – low power
LPLOUT1	3	0 – normal (default) 1 – low power

REGISTER 6 – CHIP LOW POWER 2, DEFAULT 0000 0000

Bit Name	Bit	Description
LPPGA	7	0 – normal (default) 1 – low power
LPLMIX	6	0 – normal (default) 1 – low power
LPADCvrp	1	0 – normal (default) 1 – low power
LPDACvrp	0	0 – normal (default) 1 – low power

REGISTER 7 – ANALOG VOLTAGE MANAGEMENT, DEFAULT 1111 1100

Bit Name	Bit	Description

VSEL	7:0	11111100 – normal (default)

REGISTER 8 – MASTER MODE CONTROL, DEFAULT 1000 0000

Bit Name	Bit	Description	
MSC	7	0 – slave serial port mode 1 – master serial port mode (default)	
MCLKDIV2	6	0 – MCLK not divide (default) 1 – MCLK divide by 2	
BCLK_INV	5	0 – normal (default) 1 – BCLK inverted	
BCLKDIV	4:0	00000 – master mode BCLK generated automatically based on the clock table (default) 00001 – MCLK/1 00010 – MCLK/2 00011 – MCLK/3 00100 – MCLK/4 00101 – MCLK/6 00110 – MCLK/8 00111 – MCLK/9 01000 – MCLK/11 01001 – MCLK/12 01010 – MCLK/16 01011 – MCLK/18 01100 – MCLK/22 01101 – MCLK/24 01110 – MCLK/33	01111 – MCLK/36 10000 – MCLK/44 10001 – MCLK/48 10010 – MCLK/66 10011 – MCLK/72 10100 – MCLK/5 10101 – MCLK/10 10110 – MCLK/15 10111 – MCLK/17 11000 – MCLK/20 11001 – MCLK/25 11010 – MCLK/30 11011 – MCLK/32 11100 – MCLK/34 Others – MCLK/4

REGISTER 9 – ADC CONTROL 1, DEFAULT 0000 0000

Bit Name	Bit	Description	
MicAmpL	7:4	Left channel PGA gain	
		0000 – 0 dB (default) 0001 – +3 dB 0010 – +6 dB 0011 – +9 dB 0100 – +12 dB	0101 – +15 dB 0110 – +18 dB 0111 – +21 dB 1000 – +24 dB

REGISTER 10 – ADC CONTROL 2, DEFAULT 0000 0000

Bit Name	Bit	Description
LINSEL	7:6	Channel input select 00 – LIN2/RIN2 (default) 01 – LIN1/RIN1 10 – reserved 11 – L-R differential input, L/R selection refer to DS (reg0xB[7])
capmode	0	0 – cap mode disabled (default) 1 – cap mode enabled

REGISTER 11 – ADC CONTROL 3, DEFAULT 0000 0000

Bit Name	Bit	Description
DS	7	Differential input select 0 – from input LIN2-RIN2 (default)

		1 – from input LIN1-RIN1
LDCM	6	ADC DC measure 0 – disable (default) 1 – enable
TRI	2	0 – ASDOUT is ADC normal output (default) 1 – ASDOUT tri-stated, ALRCK, DLRCK and SCLK are inputs

REGISTER 12 – ADC CONTROL 4, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCLRP	5	I2S or left justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
ADCFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserved 11 – DSP/PCM mode serial audio data format

REGISTER 13 – ADC CONTROL 5, DEFAULT 0000 0110

Bit Name	Bit	Description
adc_ratio_sel	6	ADC ratio selection for slave mode 0 – ADC ratio auto detect (default) 1 – ADC ratio use ADCFsRatio
ADCFsMode	5	0 – single speed mode (default) 1 – double speed mode
ADCFsRatio	4:0	Master mode ADC MCLK to sampling frequency ratio 00000 – 128 00001 – 192 00010 – 256 00011 – 384 00100 – 512 00101 – 576 00110 – 768 (default) 00111 – 1024 01000 – 1152 01001 – 1408 01010 – 1536 01011 – 2112 01100 – 2304 Other – reserved 10000 – 125 10001 – 136 10010 – 250 10011 – 272 10100 – 375 10101 – 500 10110 – 544 10111 – 750 11000 – 1000 11001 – 1088 11010 – 1496 11011 – 1500

REGISTER 14 – ADC CONTROL 6, DEFAULT 0010 0000

Bit Name	Bit	Description

ADC_invL	7	0 – normal (default) 1 – left channel polarity inverted	
ADC_HPF_L	5	0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)	
MAXGAIN[1:0]	3:2	ALC MAXGAIN[1:0] for PGA max gain	
		00000 – -6.5dB 00001 – -5 dB 00010 – -3.5dB 00011 – -2dB 00100 – -0.5dB 00101 – +1dB 00100 – +2.5dB 00111 – +4dB 01000 – +5.5dB 01001 – +7dB 01010 – +8.5dB 01011 – +10dB 01100 – +11.5dB 01101 – +13dB 01110 – +14.5dB	01111– +16dB 10000 – +17.5dB 10001 – +19dB 10010 – +20.5dB 10011 – +22dB 10100 – +23.5dB 10101 – +25dB 10110 – +26.5dB 10111 – +28dB 11000 – +29.5dB 11001 – +31dB 11010 – +32.5dB 11011 – +34dB others – +35.5dB
MINGAIN[1:0]	1:0	ALC MINGAIN[1:0] for PGA min gain	
		00000 – -12dB 00001 – -10.5 dB 00010 – -9dB 00011 – -7.5dB 00100 – -6dB 00101 – -4.5dB 00100 – -3dB 00111 – -1.5dB 01000 – 0dB 01001 – +1.5dB 01010 – +3dB 01011 – +4.5dB 01100 – +6dB 01101 – +7.5dB 01110 – +9dB	01111– +10.5dB 10000 – +12dB 10001 – +13.5dB 10010 – +15dB 10011 – +16.5dB 10100 – +18dB 10101 – +19.5dB 10110 – +21dB 10111 – +22.5dB 11000 – +24dB 11001 – +25.5dB 11010 – +27dB 11011 – +28.5dB others – +30dB

REGISTER 15 – ADC CONTROL 7, DEFAULT 0010 0000

Bit Name	Bit	Description
ADCRampRate	7:6	00 – 0.5 dB per 4 LRCK digital volume control ramp rate (default) 01 – 0.5 dB per 8 LRCK digital volume control ramp rate 10 – 0.5 dB per 16 LRCK digital volume control ramp rate 11 – 0.5 dB per 32 LRCK digital volume control ramp rate
ADCSoftRamp	5	0 – disabled digital volume control soft ramp 1 – enabled digital volume control soft ramp (default)
ADCMute	2	0 – normal (default) 1 – mute ADC digital output

REGISTER 16 – ADC CONTROL 8, DEFAULT 1100 0000

Bit Name	Bit	Description
LADCVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB.

		00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

REGISTER 18 – ADC CONTROL 10, DEFAULT 0011 1000

Bit Name	Bit	Description	
ALCSEL	7:6	00 – ALC off other – ALC on	
MAXGAIN[4:2]	5:3	Set maximum gain of PGA	
		000 – -6.5 dB 001 – -0.5 dB 010 – 5.5 dB 011 – 11.5 dB	100 – 17.5 dB 101 – 23.5 dB 110 – 29.5 dB 111 – 35.5 dB
MINGAIN[4:2]	2:0	Set minimum gain of PGA	
		000 – -12 dB 001 – -6 dB 010 – 0 dB 011 – +6 dB	100 – +12 dB 101 – +18 dB 110 – +24 dB 111 – +30 dB

REGISTER 19 – ADC CONTROL 11, DEFAULT 1011 0000

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 – -16.5 dB 0001 – -15 dB 0010 – -13.5 dB …… 0111 – -6 dB 1000 – -4.5 dB 1001 – -3 dB 1010-1111 – -1.5 dB
ALCHLD	3:0	ALC hold time before gain is increased 0000 – 0ms 0001 – 2.67ms 0010 – 5.33ms …… (time doubles with every step) 1001 – 0.68s 1010 or higher – 1.36s

REGISTER 20 – ADC CONTROL 12, DEFAULT 0011 0010

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time, ALC mode/limiter mode: 0000 – 410 us/90.8 us 0001 – 820 us/182us 0010 – 1.64 ms/363us …… (time doubles with every step) 1001 – 210 ms/46.5 ms 1010 or higher – 420 ms/93 ms
ALCATK	3:0	ALC attack (gain ramp down) time, ALC mode/limiter mode: 0000 – 104 us/22.7 us

		0001 – 208 us/45.4 us 0010 – 416 us/90.8 us …… (time doubles with very step) 1001 – 53.2 ms/11.6 ms 1010 or higher – 106 ms/23.2 ms

REGISTER 21 – ADC CONTROL 13, DEFAULT 0000 0110

Bit Name	Bit	Description
ALCMODE	7	Determines the ALC mode of operation: 0 – ALC mode (Normal Operation) 1 – Limiter mode.
ALCZC	6	ALC uses zero cross detection circuit. 0 – disable (recommended) 1 – enable
TIME_OUT	5	Zero Cross time out 0 – disable (default) 1 – enable
WIN_SIZE	4:0	Windows size for peak detector， set the window size to N*16 samples 00110 – 96 samples (default) 00111 – 102 samples ….. 11111 – 496 samples

REGISTER 22 – ADC CONTROL 14, DEFAULT 0000 0000

Bit Name	Bit	Description
NGTH	7:3	Noise gate threshold 00000 – -76.5 dBFS 00001 – -75 dBFS …… 11110 – -31.5 dBFS 11111 – -30 dBFS
NGG	2:1	Noise gate type x0 – PGA gain held constant 01 – mute ADC output 11 – reserved
NGAT	0	Noise gate function enable 0 – disable 1 – enable

REGISTER 23 – DAC CONTROL 1, DEFAULT 0000 0000

Bit Name	Bit	Description
DACLRSWAP	7	0 – normal 1 – left and right channel data swap
DACLRP	6	I2S or left justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edgeLRCK Polarity
DACWL	5:3	000 – 24-bit serial audio data word length

		001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
DACFORMAT	2:1	00 – I2S serial audio data format 01 – left justify serial audio data format 10 – reserved 11 – DSP/PCM mode serial audio data format

REGISTER 24 – DAC CONTROL 2, DEFAULT 0000 0110

Bit Name	Bit	Description
MODE_NOTCH	7	Notch mode, there is 2Fs OSR for input data 0 – notch mode disable (default) 1 – notch mode enable
dac_ratio_sel	6	DAC ratio selection for slave mode 0 – DAC ratio auto detect (default) 1 – DAC ratio use DACFsRatio
DACFsMode	5	0 – single speed mode (default) 1 – double speed mode
DACFsRatio	4:0	Master mode DAC MCLK to sampling frequency ratio 00000 — 128; 00001 — 192; 00010 — 256; 00011 — 384; 00100 — 512; 00101 — 576; 00110 — 768; (default) 00111 — 1024; 01000 — 1152; 01001 — 1408; 01010 — 1536; 01011 — 2112; 01100 — 2304; Other — Reserved. 10000 — 125; 10001 — 136; 10010 — 250; 10011 — 272; 10100 — 375; 10101 — 500; 10110 — 544; 10111 — 750; 11000 — 1000; 11001 — 1088; 11010 — 1496; 11011 — 1500;

REGISTER 25 – DAC CONTROL 3, DEFAULT 0010 0010

Bit Name	Bit	Description
DACRampRate	7:6	00 – 0.5 dB per 4 LRCK digital volume control ramp rate (default) 01 – 0.5 dB per 32 LRCK digital volume control ramp rate 10 – 0.5 dB per 64 LRCK digital volume control ramp rate 11 – 0.5 dB per 128 LRCK digital volume control ramp rate
DACSoftRamp	5	0 – disabled digital volume control soft ramp 1 – enabled digital volume control soft ramp (default)
DACLeR	3	0 – normal (default) 1 – both channel gain control is set by DAC left gain control register
DACMute	2	0 – normal (default) 1 – mute analog outputs for both channels

REGISTER 26 – DAC CONTROL 4, DEFAULT 1100 0000

Bit Name	Bit	Description

LDACVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

REGISTER 27 – DAC CONTROL 5, DEFAULT 1100 0000

Bit Name	Bit	Description
RDACVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

REGISTER 28 – DAC CONTROL 6, DEFAULT 0000 1000

Bit Name	Bit	Description
DeemphasisMode (DEEMP)	7:6	00 – de-emphasis frequency disabled (default) 01 – 32 KHz de-emphasis frequency in single speed mode 10 – 44.1 KHz de-emphasis frequency in single speed mode 11 – 48 KHz de-emphasis frequency in single speed mode
DAC_invL	5	0 – normal DAC left channel analog output no phase inversion (default) 1 – normal DAC left channel analog output 180 degree phase inversion
DAC_invR	4	0 – normal DAC right channel analog output no phase inversion (default) 1 – normal DAC right analog output 180 degree phase inversion
ClickFree	3	0 – disable digital click free power up and down 1 – enable digital click free power up and down (default)

REGISTER 29 – DAC CONTROL 7, DEFAULT 0000 0000

Bit Name	Bit	Description
ZeroL	7	0 – normal (default) 1 – set left channel DAC output all zero
ZeroR	6	0 – normal (default) 1 – set right channel DAC output all zero
Mono	5	0 – stereo (default) 1– mono (L+R)/2 into DACL and DACR
SE	4:2	SE strength 000 – 0 (default) …… 111 – 7
Vpp_scale	1:0	00 – Vpp set at 3.5V (0.7 modulation index) (default) 01 – Vpp set at 4.0V 10 – Vpp set at 3.0V 11 – Vpp set at 2.5V

REGISTER 30 – DAC CONTROL 8, DEFAULT 0001 1111

Bit Name	Bit	Description
Shelving_a[29:24]	5:0	30-bit a coefficient for shelving filter

		Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 31 – DAC CONTROL 9, DEFAULT 1111 0111

Bit Name	Bit	Description
Shelving_a[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 32 – DAC CONTROL 10, DEFAULT 1111 1101

Bit Name	Bit	Description
Shelving_a[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 33 – DAC CONTROL 11, DEFAULT 1111 1111

Bit Name	Bit	Description
Shelving_a[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 34 – DAC CONTROL 12, DEFAULT 0001 1111

Bit Name	Bit	Description
Shelving_b[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 35 – DAC CONTROL 13, DEFAULT 1111 0111

Bit Name	Bit	Description
Shelving_b[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 36 – DAC CONTROL 14, DEFAULT 1111 1101

Bit Name	Bit	Description
Shelving_b[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 37 – DAC CONTROL 15, DEFAULT 1111 1111

Bit Name	Bit	Description
Shelving_b[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 38 – DAC CONTROL 16, DEFAULT 0000 0000

Bit Name	Bit	Description
LMIXSEL	5:3	Left input select for output mix 000 – reserved (default) 001 – LIN1 010 – DF2SE out 011 – ADC input (after mic amplifier) others – reserved
RMIXSEL	2:0	Right input select for output mix 000 – reserved (default) 001 – RIN1 010 – DF2SE out

		011 – ADC input (after mic amplifier) others – reserved

REGISTER 39 – DAC CONTROL 17, DEFAULT 0011 1000

Bit Name	Bit	Description
LD2LO	7	0 – left DAC to left mixer disable (default) 1 – left DAC to left mixer enable
LI2LO	6	0 – LIN signal to left mixer disable (default) 1 – LIN signal to left mixer enable
LI2LOVOL	5:3	LIN signal to left mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)
MIXBOTH	2	0 – normal (default) 1 – RI2ROVOL use LI2LOVOL

REGISTER 42 – DAC CONTROL 20, DEFAULT 0011 1000

Bit Name	Bit	Description
RD2RO	7	0 – right DAC to right mixer disable (default) 1 – right DAC to right mixer enable
RI2RO	6	0 – RIN signal to right mixer disable (default) 1 – RIN signal to right mixer enable
RI2ROVOL	5:3	RIN signal to right mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)

REGISTER 43 – DAC CONTROL 21, DEFAULT 0001 0000

Bit Name	Bit	Description
slrck	7	0 – DACLRC and ADCLRC separate (default) 1 – DACLRC and ADCLRC same
lrck_sel	6	Master mode, if slrck = 1 then 0 – use DAC LRCK (default) 1 – use ADC LRCK
offset_dis	5	0 – disable offset (default) 1 – enable offset
mclk_dis	4	0 – normal 1 – disable MCLK input from PAD (default)
pdn_adc_anaclk	3	0 – normal (default) 1 – power down ADC anaclk
pdn_dac_anaclk	2	0 – normal (default)

		1 – power down DAC anaclk

REGISTER 44 – DAC CONTROL 22, DEFAULT 0000 0000

Bit Name	Bit	Description
offset	7:0	DC offset

REGISTER 45 – DAC CONTROL 23, DEFAULT 0000 0000

Bit Name	Bit	Description
VROI	4	0 – 1.5k VREF to analog output resistance (default) 1 – 40k VREF to analog output resistance

REGISTER 48 – DAC CONTROL 26, DEFAULT 0000 0000

Bit Name	Bit	Description
LRBOTH	6	0 – normal (default) 1 – ROUTVOL use LOUTVOL
LOUTVOL	5:0	LOUT volume 000000 – -45dB (default) 000001 – -43.5dB 000010 – -42dB … 011110 – 0dB 011111 – 1.5dB … 100001 – 4.5dB

REGISTER 49 – DAC CONTROL 27, DEFAULT 0000 0000

Bit Name	Bit	Description
ROUTVOL	5:0	ROUT volume 000000 – -45dB (default) 000001 – -43.5dB 000010 – -42dB … 011110 – 0dB 011111 – 1.5dB … 100001 – 4.5dB

REGISTER 53 – TEST MODE, DEFAULT 0000 0000

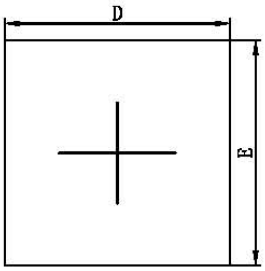
Bit Name	Bit	Description
TestModeEnable	7	Writing a0 to this register enables the test mode

REGISTER 56 – ADC TEST CONTROL 2, DEFAULT 0000 0000

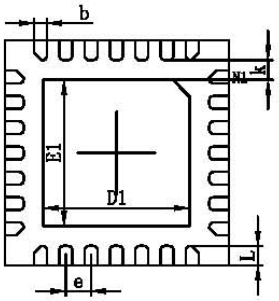
Bit Name	Bit	Description
DF2SE_10dB	1	DF2SE 10 dB enable 0 – disable (default) 1 – enable

10.PACKAGE

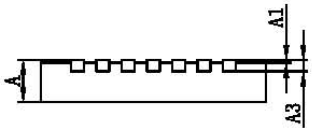
QFNWB4×4-28L-A(P0.45T0.75/0.85)PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
E1	2.500	2.700	0.098	0.106
D1	2.500	2.700	0.098	0.106
k	0.200MIN		0.008MIN	
b	0.180	0.280	0.007	0.011
e	0.450TYP.		0.018TYP.	
L	0.274	0.426	0.011	0.017

11.CORPORATE INFORMATION

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