

## Document Title

**1M x 16 bit Low Low Power 1T/1C Pseudo SRAM**

## Revision history

Revision No.	History	Draft Date	Remark
1.0	Initial	Dec. 3. '02	Preliminary
1.1	DC Spec. 변경	Apr. 21. '03	
1.2	Add to Lead Free Product	Mar. 09. '04	
1.3	Modification of Part Number [Lead Free Product] (HY64UD16162B-DFxxxP Series → HY64UD16162B-DFPxxx Series)	Jul. 22. '04	

## 1M x 16 bit Low Low Power 1T/1C SRAM

### DESCRIPTION

The HY64UD16162B-DF(P)xxx series is a 16Mbit 1T/1C SRAM featured by high-speed operation and super low power consumption. The HY64UD16162B series adopts one transistor memory cell and is organized as 1,048,576 words by 16bits. The HY64UD16162B series operates in the extended range of temperature and supports a wide operating voltage range. The HY64UD16162B series also supports the deep power down mode for a super low standby current. The HY64UD16162B series delivers the high-density low power SRAM capability to the high-speed low power system.

### FEATURES

- CMOS Process Technology
- 1M x 16 bit Organization
- TTL compatible and Tri-state outputs
- Deep Power Down : Memory cell data hold invalid
- Standard pin configuration : 48-FBGA(6mmX8mm)
- Data mask function by /LB, /UB
- Separated I/O Power Supply : Vddq

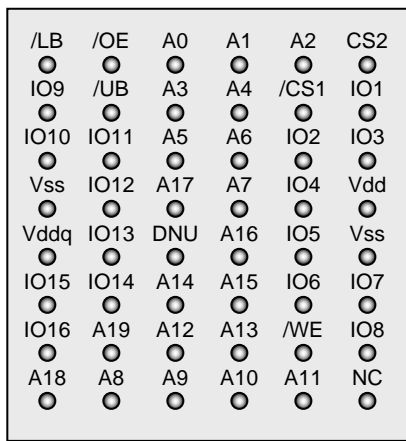
### PRODUCT FAMILY

Product No.	Voltage [V] Vdd/Vddq	Mode	Power Dissipation			Speed tRC[ns]	Temp. [°C]
			(ISB1,Max)	(IDPD,Max)	(Icc2,Max)		
HY64UD16162B-DF(P)60E	3.0/3.0	1CS with /UB,/LB:tCS <sup>1</sup>	TBD	10µA	25mA	TBD	-25~85
HY64UD16162B-DF(P)60I	3.0/3.0	1CS with /UB,/LB:tCS <sup>1</sup>	TBD	10µA	25mA	TBD	-40~85
HY64UD16162B-DF(P)70E	3.0/3.0	1CS with /UB,/LB:tCS <sup>1</sup>	85µA	10µA	25mA	70	-25~85
HY64UD16162B-DF(P)70I	3.0/3.0	1CS with /UB,/LB:tCS <sup>1</sup>	85µA	10µA	25mA	70	-40~85

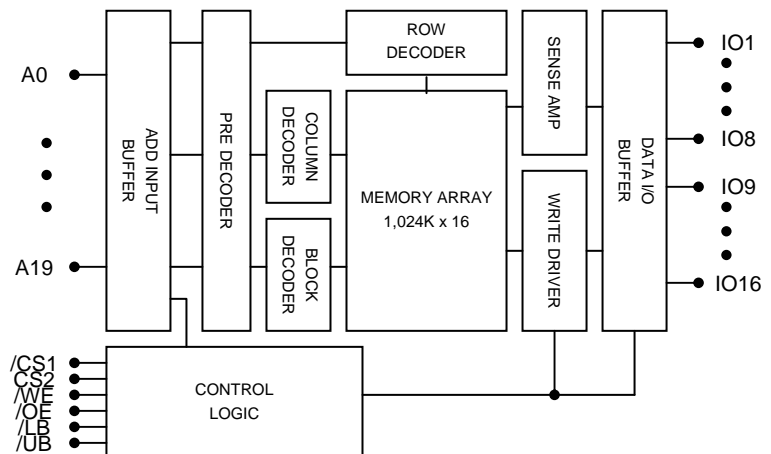
Note 1. tCS - /UB,/LB=High : Chip Deselect.

2. HY64UD16162B-DFxxx Series : Leaded FBGA
- HY64UD16162B-DFPxxx Series : Lead Free FBGA

### PIN CONNECTION (Top View)



### BLOCK DIAGRAM



### PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select	/OE	Output Enable
CS2	Deep Power Down	IO1~IO8	Lower Data Inputs/Outputs
/WE	Write Enable	IO9~IO16	Upper Data Inputs/Outputs
/LB	Lower Byte(I/O1~I/O8)	A0~A19	Address Inputs
/UB	Upper Byte(I/O9~I/O16)	Vdd	Power Supply for Internal Circuit
DNU	Do Not Use	Vddq	Power Supply for I/O
NC	No Connection	Vss	Ground

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**ORDERING INFORMATION**

Part Number	Speed	Power	Temperature	FBGA
HY64UD16162B-DFxxE	60 / 70	LL-Part	E <sup>1</sup>	Lead
HY64UD16162B-DFxxI	60 / 70	LL-Part	I <sup>2*</sup>	Lead
HY64UD16162B-DFPxxE	60 / 70	LL-Part	E <sup>1</sup>	Lead Free
HY64UD16162B-DFPxxI	60 / 70	LL-Part	I <sup>2*</sup>	Lead Free

Note

1. E : Extended Temp. (-25°C ~ 85°C)
2. I : Industrial Temp. (-40°C ~ 85°C)

**ABSOLUTE MAXIMUM RATINGS <sup>1</sup>**

Symbol	Parameter	Rating	Unit	Remark
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>dd</sub> +0.3	V	
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>ddq</sub> +0.3	V	
V <sub>dd</sub>	Core Power Supply	-0.3 to 3.6	V	
V <sub>ddq</sub>	I/O Power Supply	-0.3 to 3.6	V	
T <sub>A</sub>	Ambient Temperature	-25 to 85	°C	HY64UD16162B-DF(P)xxE
		-40 to 85	°C	HY64UD16162B-DF(P)xxI
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C	
P <sub>D</sub>	Power Dissipation	1.0	W	
T <sub>SOLDER</sub>	Ball Soldering Temperature & Time	260•10	°C•sec	

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**TRUTH TABLE**

/CS1	CS2	/WE	/OE	/LB	/UB	Mode	I/O Pin		Power
							I/O1~I/O8	I/O9~I/O16	
H	H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	L	X	X	X	X	Deselected	High-Z	High-Z	Deep Power Down
X	H	X	X	H	H	Deselected	High-Z	High-Z	Standby
L	H	L	X	L	H	Write	DIN	High-Z	Active
L	H	H	L	L	H	Read	DOUT	High-Z	Active
L	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
L	H	L	X	H	L	Write	High-Z	DIN	Active
L	H	H	L	H	L	Read	High-Z	DOUT	Active
L	H	H	H	H	L	Output Disabled	High-Z	High-Z	Active
L	H	L	X	L	L	Write	DIN	DIN	Active
L	H	H	L	L	L	Read	DOUT	DOUT	Active
L	H	H	H	L	L	Output Disabled	High-Z	High-Z	Active

Note

1. H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care(V<sub>IL</sub> or V<sub>IH</sub>)
2. /UB, /LB(Upper, Lower Byte enable)  
 These active LOW inputs allow individual bytes to be written or read.  
 When /LB is LOW, data is written or read to the lower byte, I/O1 - I/O8.  
 When /UB is LOW, data is written or read to the upper byte, I/O9 - I/O16.

**RECOMMENDED DC OPERATING CONDITION**

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vdd	Core Supply Voltage	2.7	3.0	3.3	V
Vddq	I/O Supply Voltage	2.7	3.0	3.3	V
Vss	Ground	0	-	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	Vdd+0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>1</sup>	-	0.6	V

Note 1. V<sub>IL</sub> = -1.5V for pulse width less than 10ns  
 Undershoot is sampled, not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**

Vdd=2.7V~3.3V, Vddq=2.7V~3.3V, T<sub>A</sub>= -25°C to 85°C(E) / -40°C to 85°C(I)

Sym.	Parameter	Test Condition	Min.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> , /CS1=V <sub>IH</sub> , CS2=V <sub>IH</sub> , /OE=V <sub>IH</sub> or /WE=V <sub>IL</sub>	-1	1	μA	
I <sub>CC</sub>	Operating Power Supply Current	/CS1=V <sub>IL</sub> , CS2=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> =0mA	-	3	mA	
I <sub>CC1</sub>	Average Operating Current	/CS1 ≤ 0.2V, CS2 ≥ V <sub>DD</sub> -0.2V, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V, Cycle Time=1μs. 100% Duty, I <sub>I/O</sub> =0mA	-	5	mA	
I <sub>CC2</sub>		/CS1=V <sub>IL</sub> , CS2=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Cycle Time=Min. 100% Duty, I <sub>I/O</sub> =0mA	60ns 70ns	-	25 25	mA mA
I <sub>SB</sub>	TTL Standby Current	/CS1, CS2=V <sub>IH</sub> or /UB, /LB= V <sub>IH</sub>	-	0.5	mA	
I <sub>SB1</sub>	Standby Current(CMOS Input)	/CS1, CS2 ≥ V <sub>DD</sub> -0.2V, /UB, /LB ≤ 0.2V or /UB, /LB ≥ V <sub>DD</sub> -0.2V, otherwise CS2, /UB, /LB ≥ V <sub>DD</sub> -0.2V, /CS1 ≤ 0.2V or /CS1 ≥ V <sub>DD</sub> -0.2V	60ns	-	TBD	μA
			70ns	-	85	μA
I <sub>DPD</sub>	Deep Power Down	CS2 ≤ V <sub>SS</sub> +0.2V	-	10	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-1.0mA	2.4	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	0.4	V	

**CAPACITANCE**

(Temp = 25°C, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance(ADD, /CS1, CS2, /WE, /OE, /UB, /LB)	V <sub>IN</sub> =0V	8	pF
C <sub>OUT</sub>	Output Capacitance(I/O)	V <sub>I/O</sub> =0V	10	pF

Note : These parameters are sampled and not 100% tested

## AC CHARACTERISTICS

V<sub>dd</sub>=2.7V~3.3V, V<sub>ddq</sub>=2.7V~3.3V, T<sub>A</sub> = -25°C to 85°C(E) / -40°C to 85°C(I), unless otherwise specified

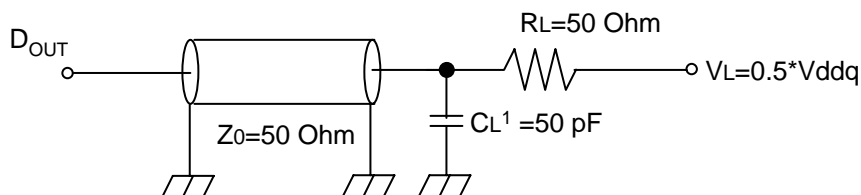
#	Symbol	Parameter	-60		-70		Unit
			Min.	Max.	Min.	Max.	
<b>Read Cycle</b>							
1	t <sub>RC</sub>	Read Cycle Time	60	-	70	-	ns
2	t <sub>AA</sub>	Address Access Time	-	60	-	70	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	60	-	70	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	20	-	20	ns
5	t <sub>BA</sub>	/LB, /UB Access Time	-	60	-	70	ns
6	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	ns
7	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	ns
8	t <sub>BLZ</sub>	/LB, /UB Enable to Output in Low Z	10	-	10	-	ns
9	t <sub>CHZ</sub>	Chip Disable to Output in High Z	0	10	0	10	ns
10	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	10	0	10	ns
11	t <sub>BHZ</sub>	/LB, /UB Disable to Output in High Z	0	10	0	10	ns
12	t <sub>OH</sub>	Output Hold from Address Change	5	-	5	-	ns
<b>Write Cycle</b>							
13	t <sub>WC</sub>	Write Cycle Time	60	-	70	-	ns
14	t <sub>CW</sub>	Chip Selection to End of Write	55	-	60	-	ns
15	t <sub>AW</sub>	Address Valid to End of Write	55	-	60	-	ns
16	t <sub>BW</sub>	/LB, /UB Valid to End of Write	55	-	60	-	ns
17	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	ns
18	t <sub>WP</sub>	Write Pulse Width	50	-	50	-	ns
19	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
20	t <sub>WHZ</sub>	Write to Output in High Z	0	15	0	20	ns
21	t <sub>DW</sub>	Data to Write Time Overlap	25	-	30	-	ns
22	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	ns
23	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	ns

## AC TEST CONDITIONS

T<sub>A</sub> = -25°C to 85°C(E) / -40°C to 85°C(I), unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rising and Fall Time	5ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	0.5*V <sub>ddq</sub>
Output Load	See Below

## AC TEST LOADS



Note

1. Including jig and scope capacitance.

## Power-Up Sequence

1. Supply power with CS2 high.
2. Maintain stable power for longer than 200 $\mu$ s.

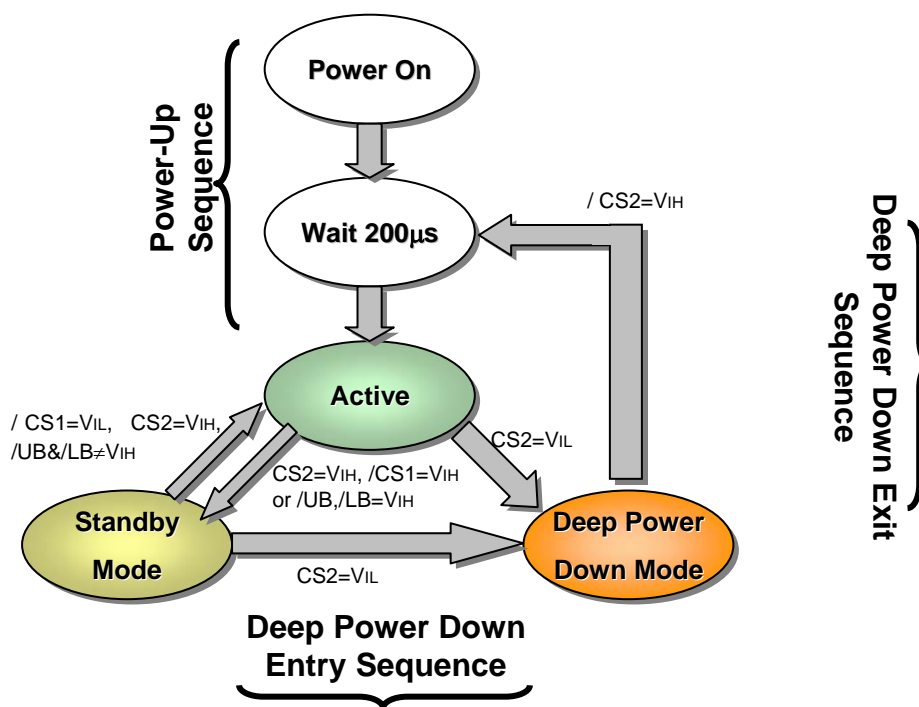
## Deep Power Down Entry Sequence

1. Keep CS2 low state.  
Deep power down mode is maintained while CS2 is low state.

## Deep Power Down Exit Sequence

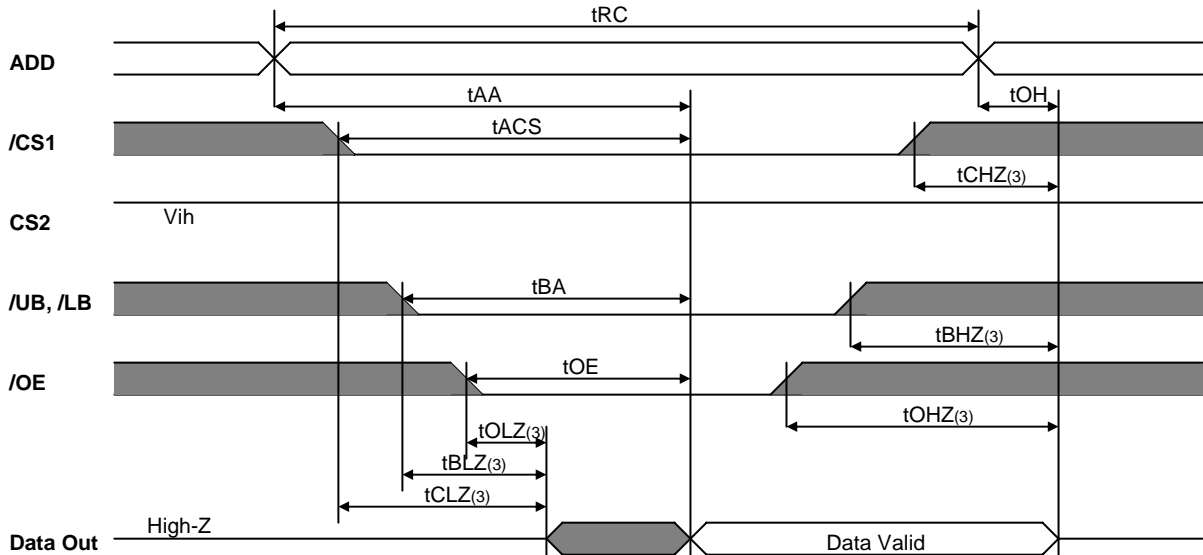
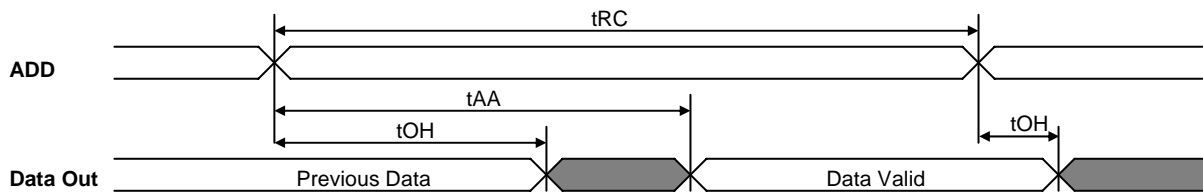
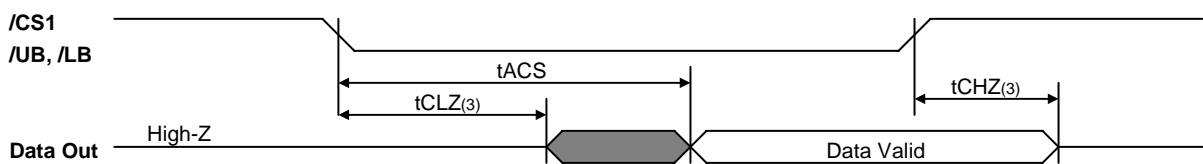
1. Keep CS2 high state.
2. Maintain stable power for longer than 200 $\mu$ s.

## STATE DIAGRAM

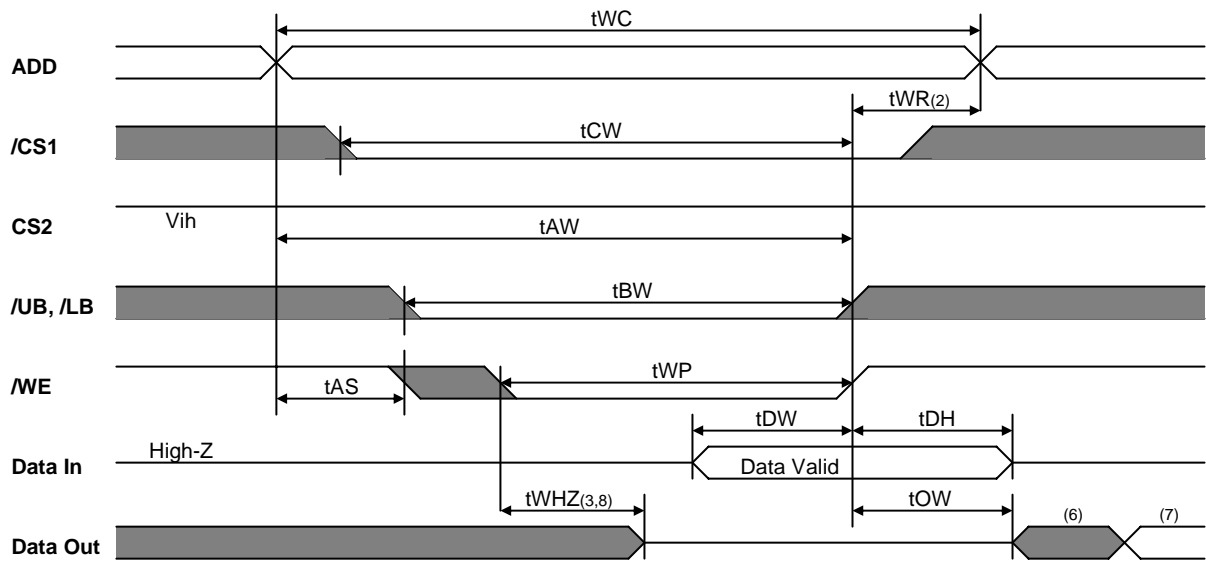
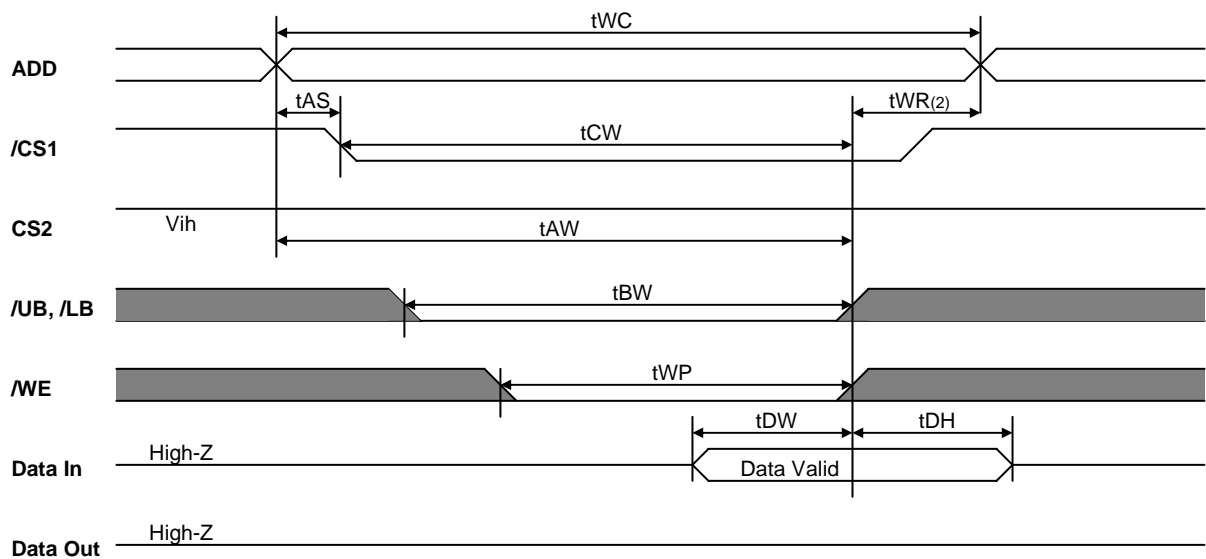


## STANDBY MODE CHARACTERISTICS

Mode	Memory Cell Data	Standby Current[ $\mu$ A]	Wait Time[ $\mu$ s]
Standby	Valid	TBD / 60ns	0
		85 / 70ns	
Deep Power Down	Invalid	2	200

**TIMING DIAGRAM**
**READ CYCLE 1 ( Note 1, 4 )**

**READ CYCLE 2 ( Note 1, 2, 4 ) ( CS2=Vih )**

**READ CYCLE 3 ( Note 1, 2, 4 ) ( CS2=Vih )**

**Notes :**

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB and/or /LB and /CS1 and CS2 are in active status.
2. /OE = V<sub>IL</sub>
3. tCHZ, tBHZ and tOHZ are defined as the time at which the outputs achieve the high impedance state and tOLZ, tBLZ and tCLZ are defined as the time at which the outputs achieve the low impedance state. These are not referenced to output voltage levels.
4. /CS1 in high for the standby, low for active.  
/UB and /LB in high for the standby, low for active.

**WRITE CYCLE 1 ( Note 1, 4, 5, 9, 10 ) ( /WE Controlled )**

**WRITE CYCLE 2 ( Note 1, 4, 5, 9, 10 ) ( /CS1 Controlled )**

**Notes :**

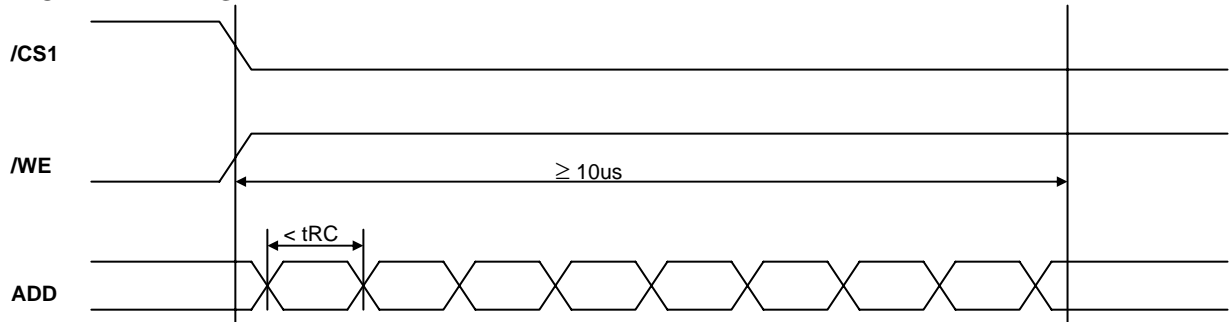
1. A write occurs during the overlap of low /CS1, low /WE and low /UB and/or /LB.
2.  $t_{WR}$  is measured from the earlier of /CS1, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low ( $OE=V_{IL}$ )
6. Q(data out) is the invalid data.
7. Q(data out) is the read data of the next address.
8.  $t_{WHZ}$  is defined as the time at which the outputs achieve the high impedance state. It is not referenced to output voltage levels.
9. /CS1 in high for the standby, low for active. /UB and /LB in high for the standby, low for active.
10. Do not input data to the I/O pins while they are in the output state.



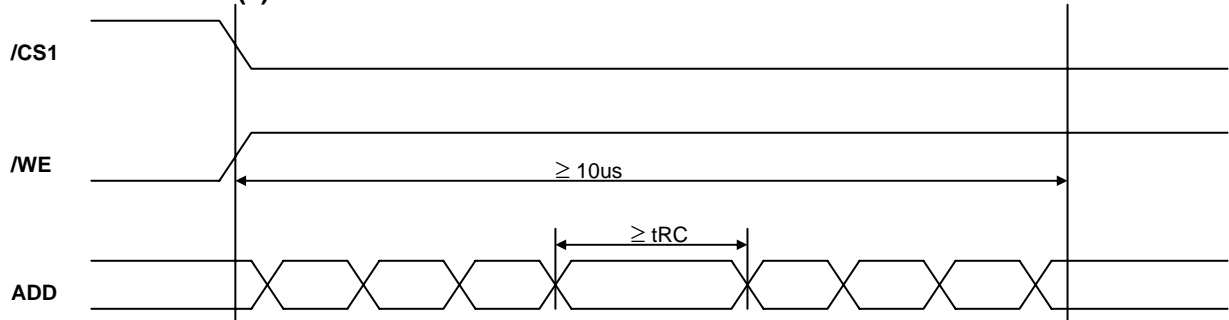
## AVOID TIMING

Hynix 1T/1C SRAM has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than  $t_{RC}$  during over 10us at read operation which showed in abnormal timing, Hynix 1T/1C SRAM needs a normal read timing at least during 10us which showed in avoidable timing(1) or toggle the  $/CS1$  to high( $\geq t_{RC}$ ) one time at least which showed in avoidable timing(2)

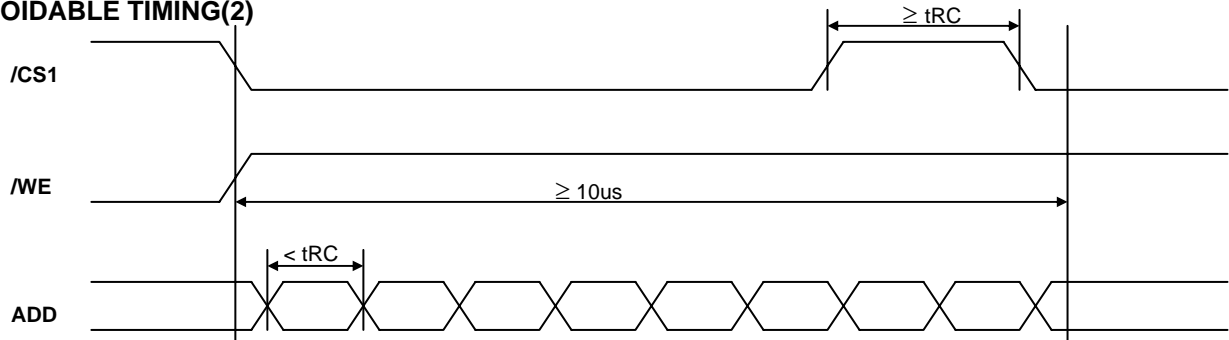
### ABNORMAL TIMING



### AVOIDABLE TIMING(1)

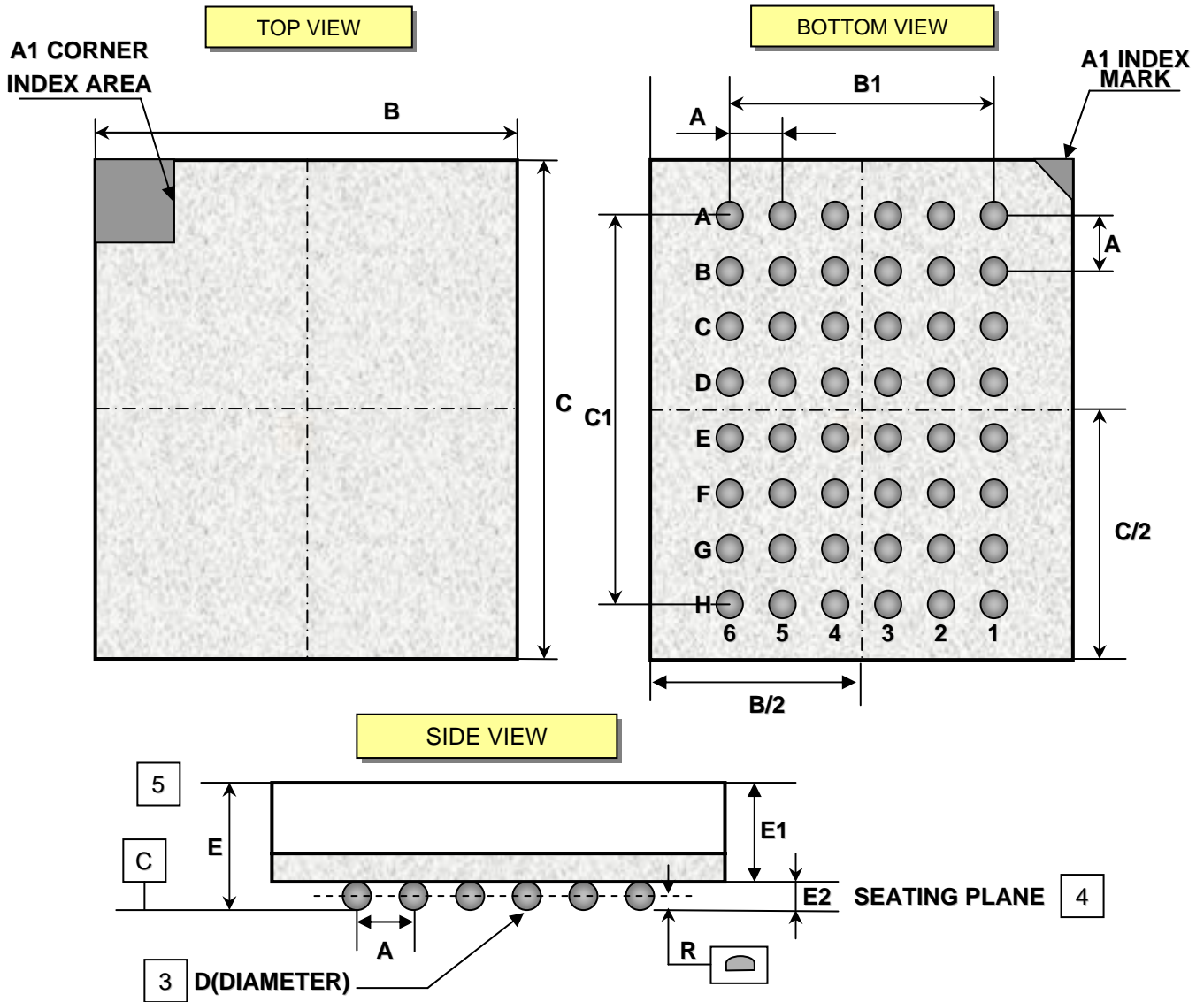


### AVOIDABLE TIMING(2)



## PACKAGE DIMENSION

48ball Fine Pitch Ball Grid Array Package(F)



unit : mm

Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
R	-	-	0.08

### NOTE.

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

**MARKING INFORMATION**

Package	Marking Example
FBGA	

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<ul style="list-style-type: none"> <li>• <b>HYUD16162B</b> : Part Name</li> <li><b>HY</b> : HYNIX</li> <li><b>U</b> : Power Supply : Vdd=2.7V~3.3V/Vddq=2.7V~3.3V</li> <li><b>D</b> : Tech. + Classification : 1T+1C</li> <li><b>16</b> : Bit Organization : x16</li> <li><b>16</b> : Density : 16M</li> <li><b>2</b> : Mode : 1CS with /UB,/LB;tCS</li> <li><b>B</b> : Version : 3rd Generation</li> </ul>	
<ul style="list-style-type: none"> <li>• <b>c</b> : Power Consumption : D – Low Low Power</li> <li>• <b>ss</b> : Speed : 60 – 60ns 70 – 70ns</li> <li>• <b>t</b> : Temperature : E – Extended(-25 ~ 85°C) I – Industrial(-40 ~ 85°C)</li> <li>• <b>yy</b> : Year ( ex : 02 = year 2002, 03= year 2003)</li> <li>• <b>ww</b> : Work Week ( ex : 12 = work week 12 )</li> <li>• <b>p</b> : P – Process Code : A – Current Product : <b>P – Lead Free Package</b></li> </ul>	
<ul style="list-style-type: none"> <li>• <b>xxxxx</b> : Lot No.</li> <li>• <b>KOR</b> : Origin Country</li> </ul>	
<p><b>Note</b></p> <ul style="list-style-type: none"> <li>- Capital Letter : Fixed Item</li> <li>- Small Letter : Non-fixed Item</li> </ul>	