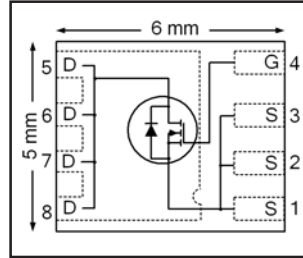


**Applications**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

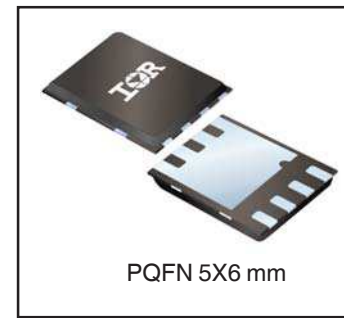
HEXFET® Power MOSFET



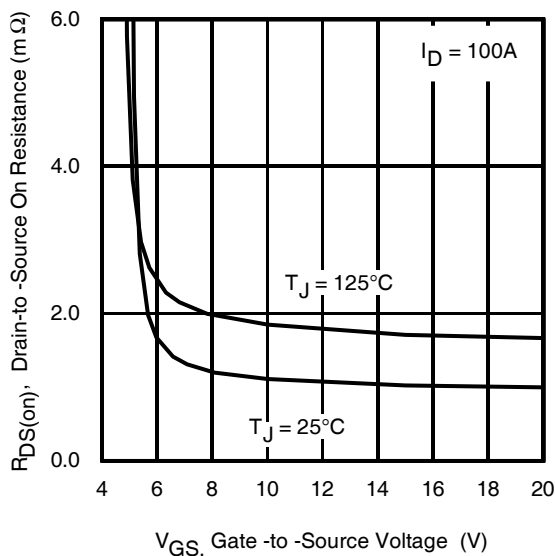
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ. max.</b>	<b>1.1mΩ</b>
	<b>1.4mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>259A①</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>100A</b>

**Benefits**

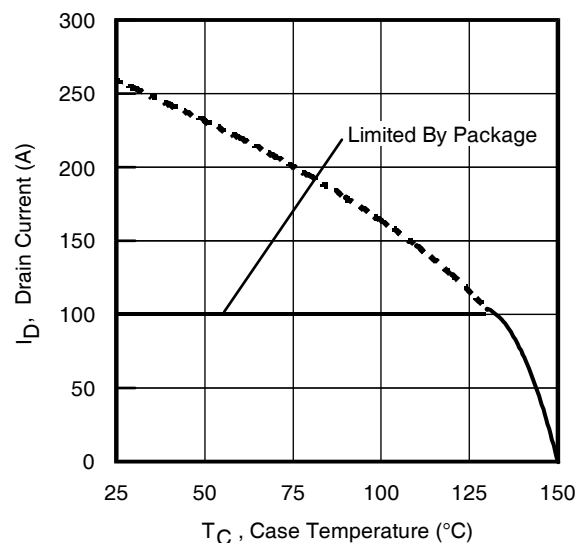
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- RoHS Compliant containing no Lead, no Bromide, and no Halogen



Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7004PBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7004TRPBF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	259 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	164 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	100	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1247	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	156	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	191	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	479	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case <sup>⑤</sup>	0.5	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case <sup>⑤</sup>	—	15	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑤</sup>	—	34	
$R_{\theta JA} (<10\text{s})$	Junction-to-Ambient <sup>⑤</sup>	—	21	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.033	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$ <sup>②</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.1	1.4	m $\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 100\text{A}$ <sup>⑤</sup>
		—	1.7	—	m $\Omega$	$V_{GS} = 6.0\text{V}$ , $I_D = 50\text{A}$ <sup>⑤</sup>
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}$ , $I_D = 150\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	2.4	—	$\Omega$	

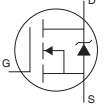
**Notes:**

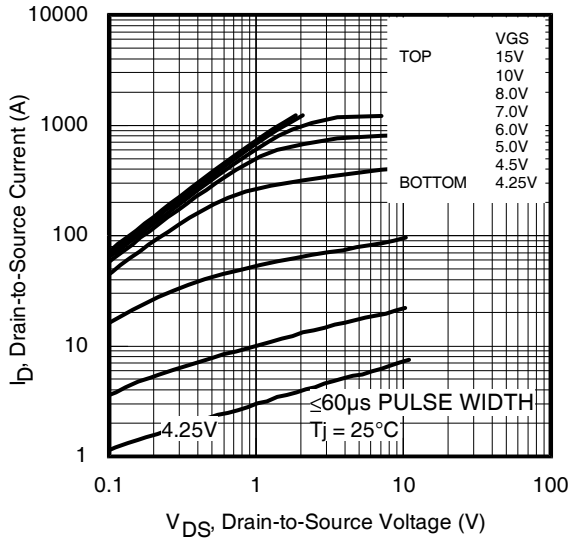
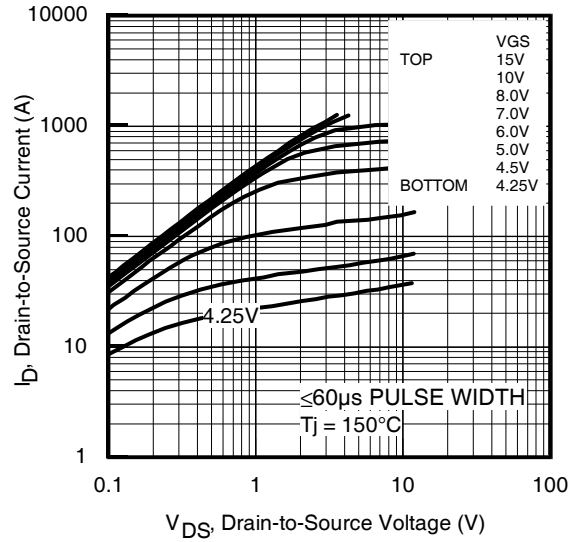
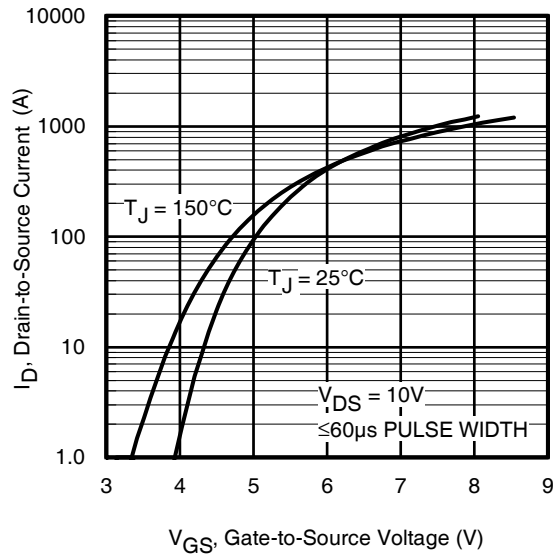
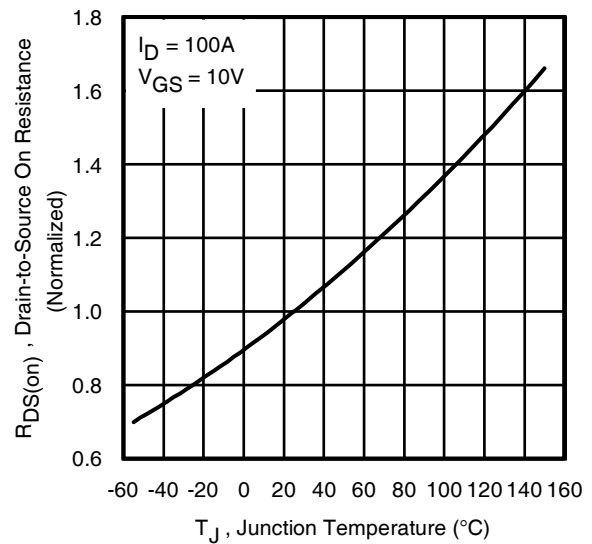
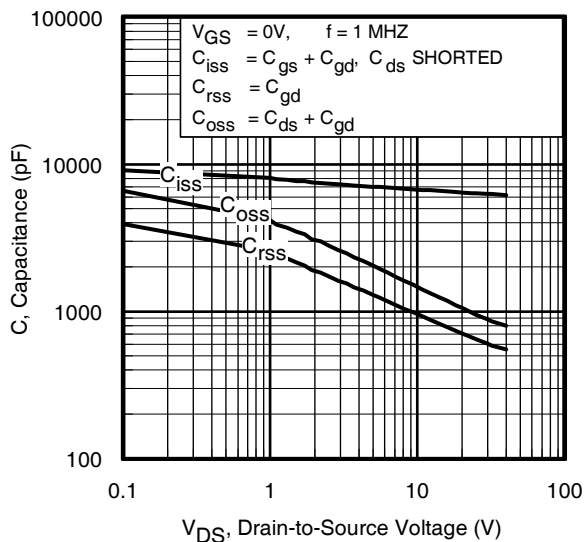
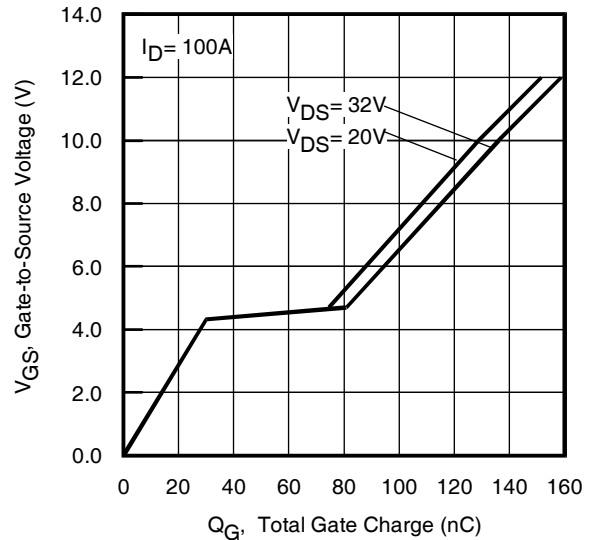
- ① Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.038\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 1366\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1 inch square 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 31\text{A}$ ,  $V_{GS} = 10\text{V}$ .

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	117	—	—	S	$V_{DS} = 10\text{V}, I_D = 100\text{A}$
$Q_g$	Total Gate Charge	—	129	194	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V}$ ⑤
$Q_{gs}$	Gate-to-Source Charge	—	34	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	40	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	169	—		
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
$t_r$	Rise Time	—	51	—		
$t_{d(off)}$	Turn-Off Delay Time	—	73	—		
$t_f$	Fall Time	—	49	—		
$C_{iss}$	Input Capacitance	—	6419	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$ ⑦ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$ ⑧
$C_{oss}$	Output Capacitance	—	952	—		
$C_{rss}$	Reverse Transfer Capacitance	—	656	—		
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1161	—		
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	1305	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	100①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	1247	A	
$V_{SD}$	Diode Forward Voltage	—	0.95	1.3	V	$T_J = 25^\circ\text{C}, I_S = 100\text{A}, V_{GS} = 0\text{V}$ ③
$dv/dt$	Peak Diode Recovery ④	—	2.5	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 100\text{A}, V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	35	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 34\text{V},$ $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	26	—		
		—	27	—		$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤
$I_{RRM}$	Reverse Recovery Current	—	1.5	—	A	$T_J = 25^\circ\text{C}$


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**

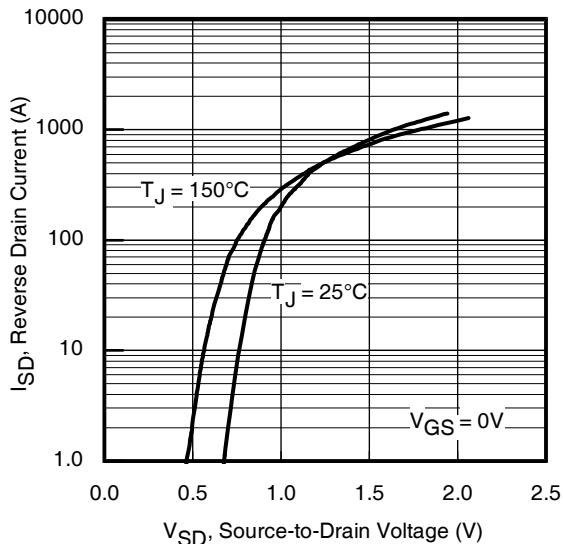


Fig 9. Typical Source-Drain Diode Forward Voltage

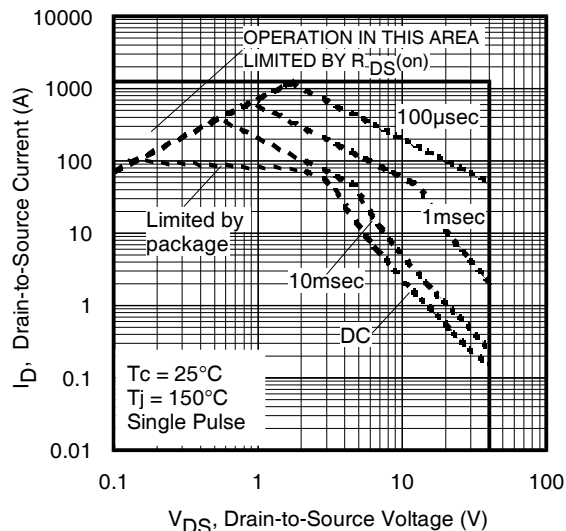


Fig 10. Maximum Safe Operating Area

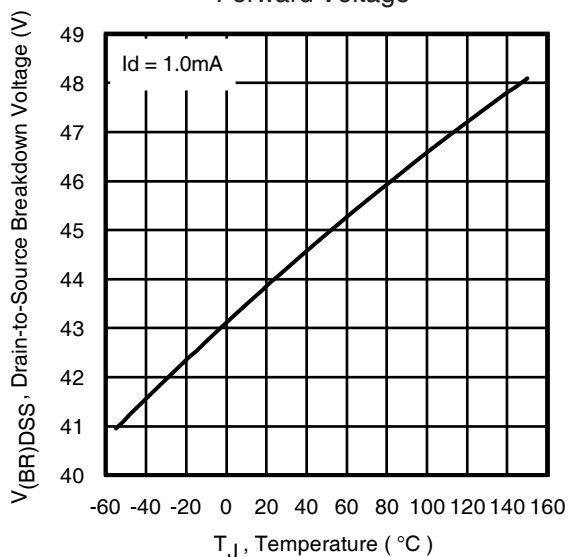


Fig 11. Drain-to-Source Breakdown Voltage

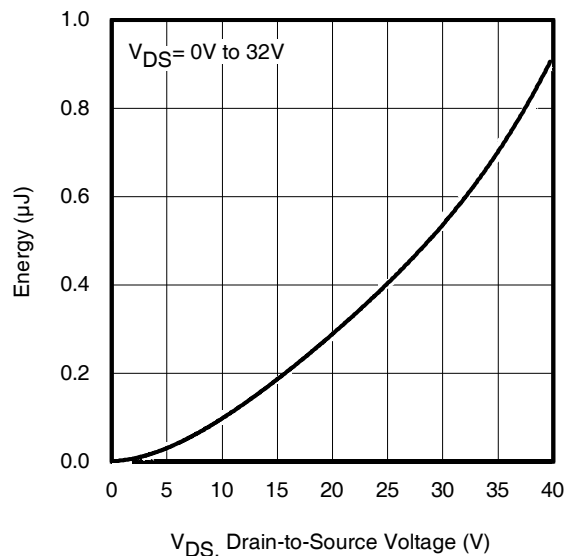


Fig 12. Typical  $C_{OSS}$  Stored Energy

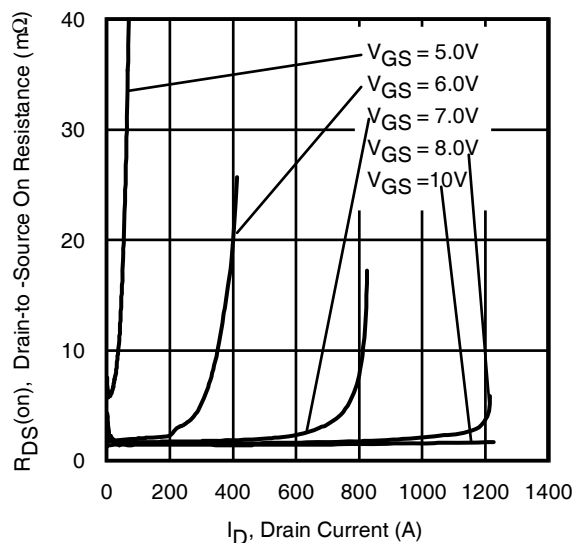
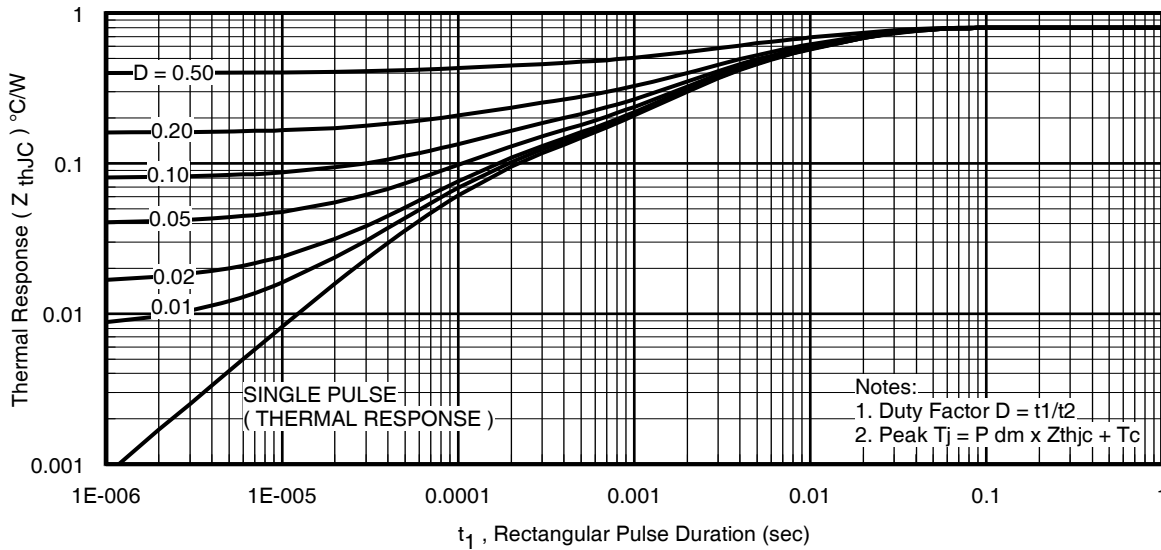
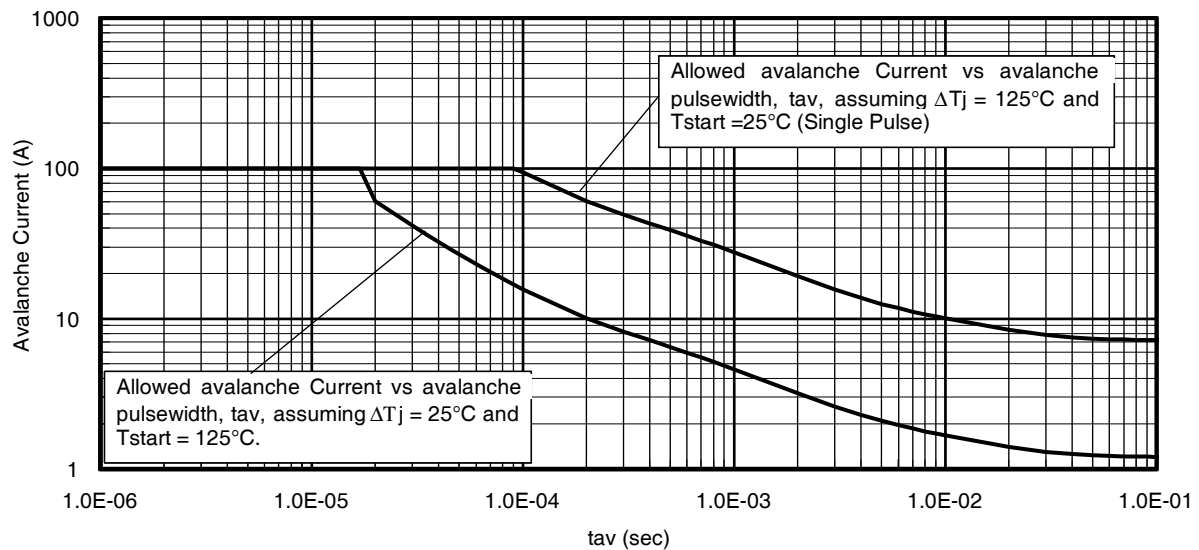
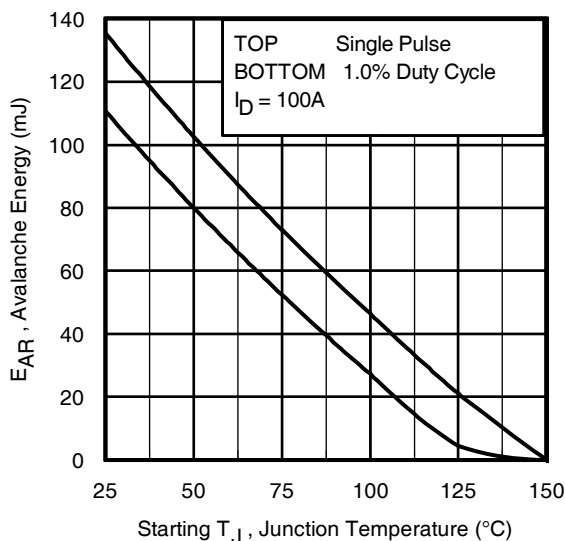


Fig 13. Typical On-Resistance vs. Drain Current

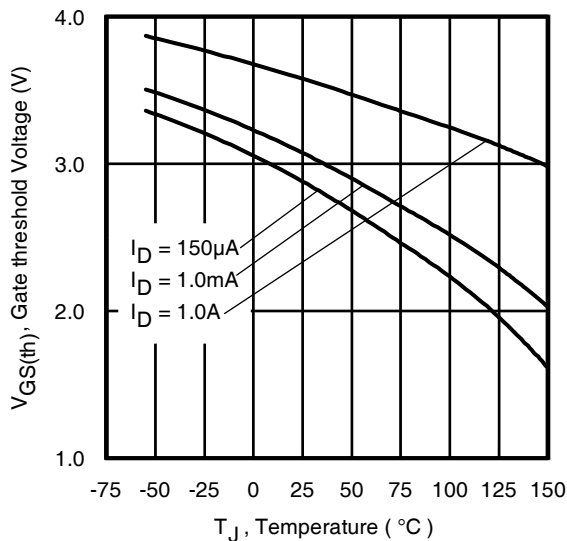
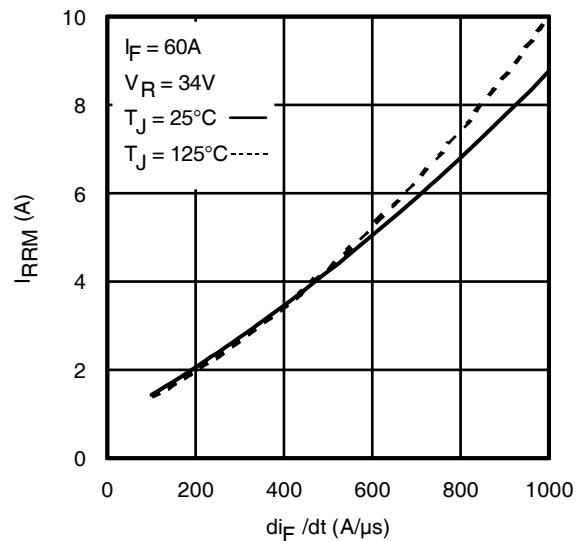
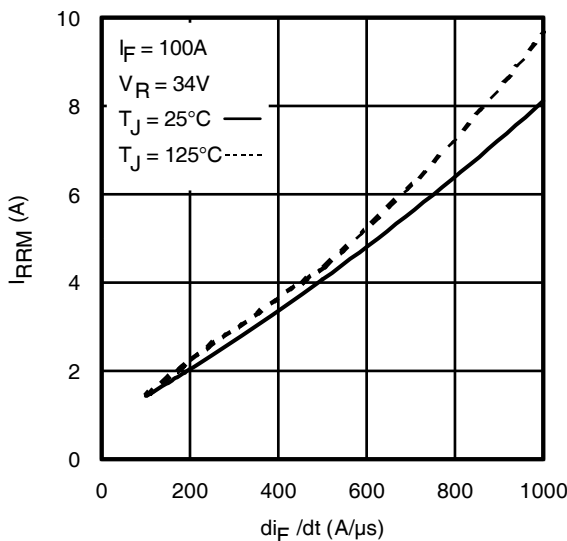
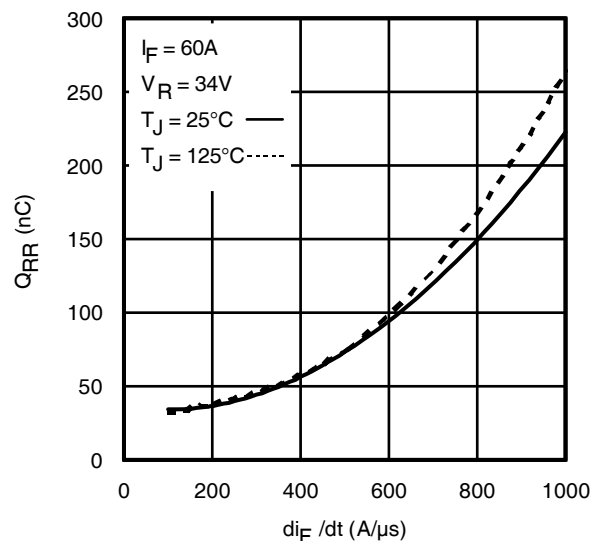
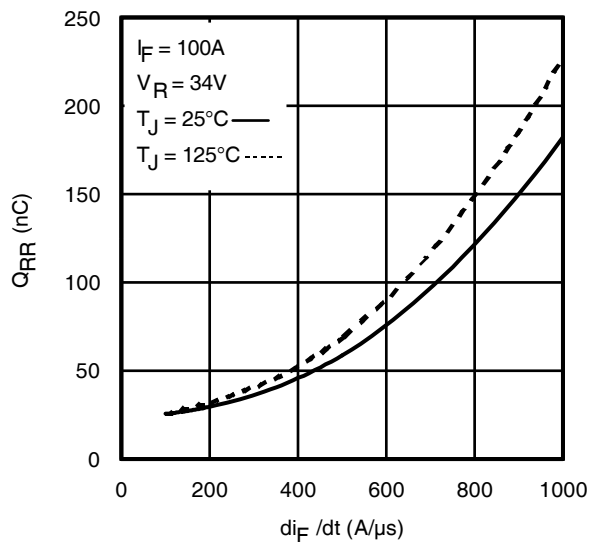

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Typical Avalanche Current vs. Pulsewidth**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

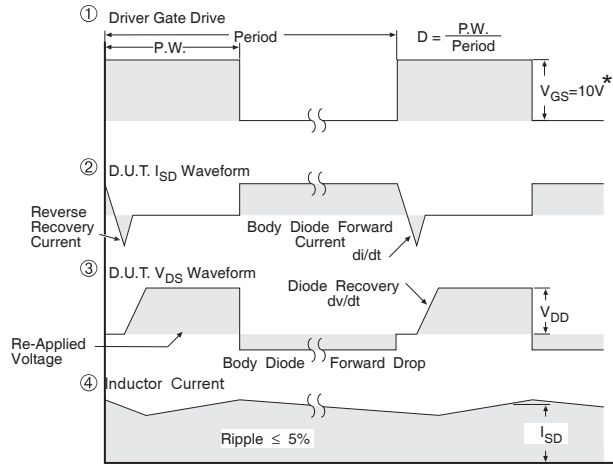
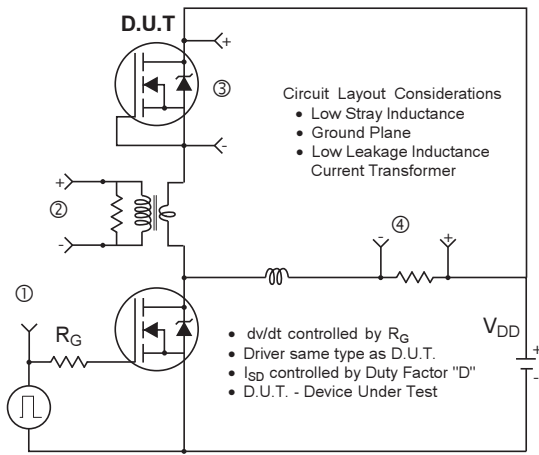
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

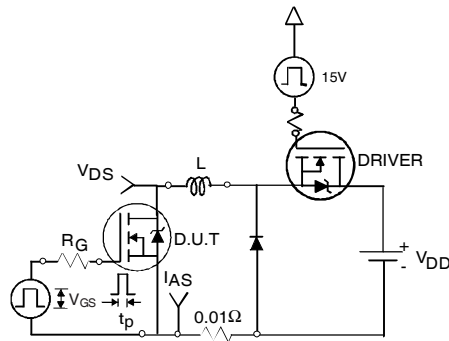
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig. 18 -** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 19 -** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_f/dt$ 

**Fig. 21 -** Typical Stored Charge vs.  $di_f/dt$

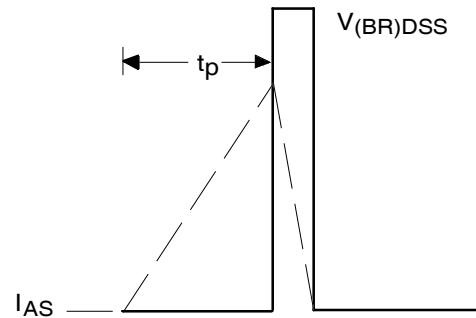


\*  $V_{GS} = 5V$  for Logic Level Devices

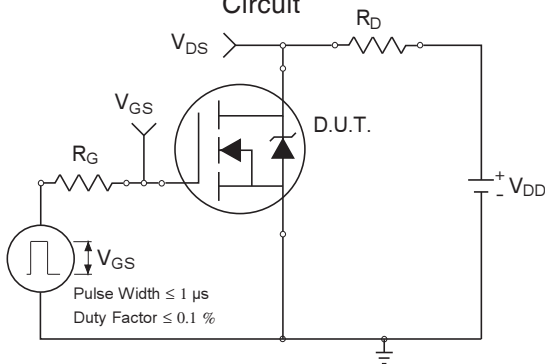
**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



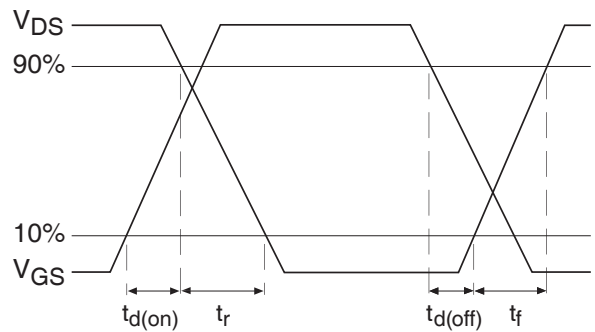
**Fig 22a. Unclamped Inductive Test Circuit**



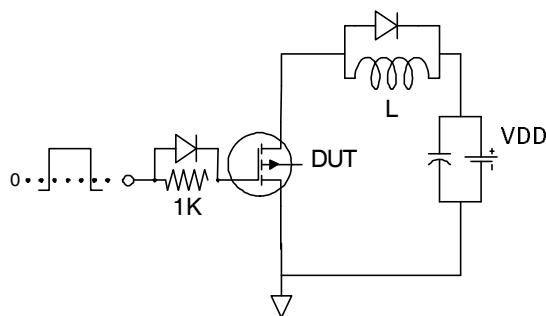
**Fig 22b. Unclamped Inductive Waveforms**



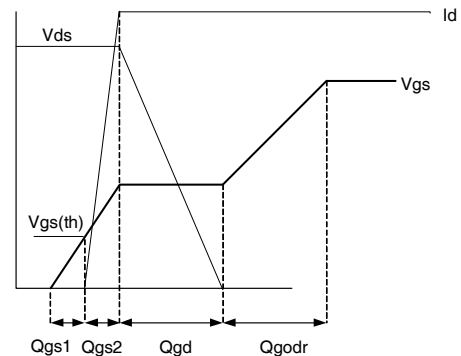
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



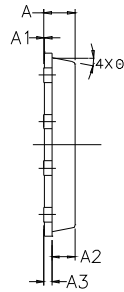
**Fig 24a. Gate Charge Test Circuit**



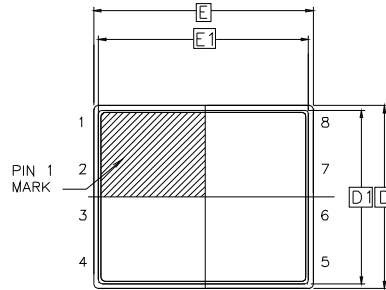
**Fig 24b. Gate Charge Waveform**



# PQFN 5x6 Outline "B" Package Details

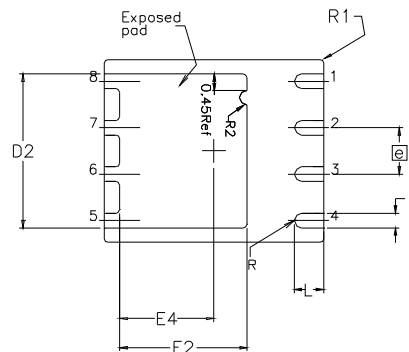


SIDE VIEW



TOP VIEW

DIM	MIN	NOM	MAX
SYMBOL			
A	0.800	0.830	1.05
A1	0.000	0.020	0.050
A2	0.580	0.630	0.680
A3		0.254 REF	
Ø	0"	10"	12"
b	0.350	0.400	0.470
D	4.850	5.000	5.150
D1	4.675	4.750	5.000
D2	3.700	4.210	4.300
e		1.270 BSC	
E	5.850	6.000	6.150
E1	5.675	5.750	6.000
E2	3.380	3.480	3.760
E4	2.480	2.580	2.680
L	0.550	0.800	0.900
R		0.200 REF	
R1		0.100 REF	
R2	0.150	0.200	0.250



BOTTOM VIEW

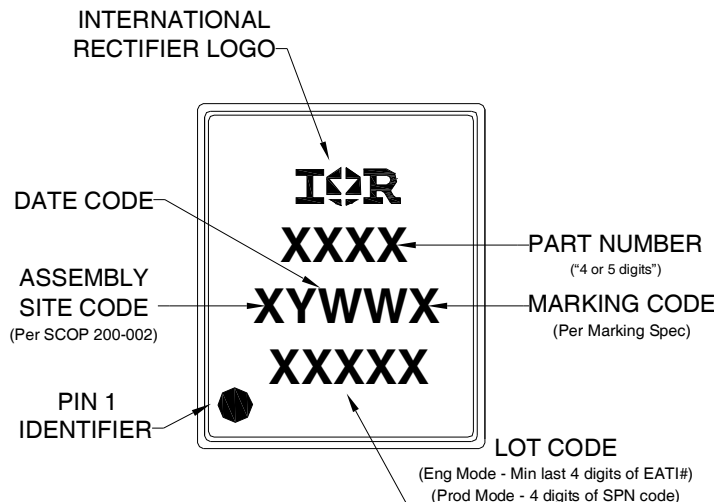
For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

<http://www.irf.com/technical-info/appnotes/an-1154.pdf>

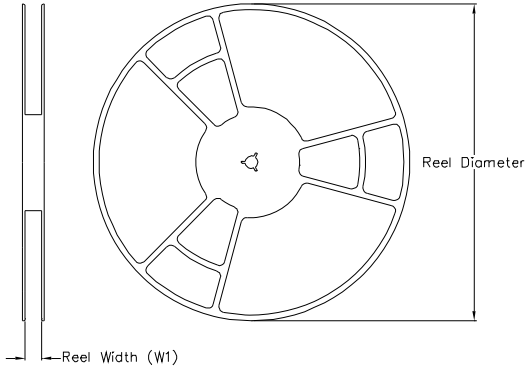
## PQFN 5x6 Outline "B" Part Marking



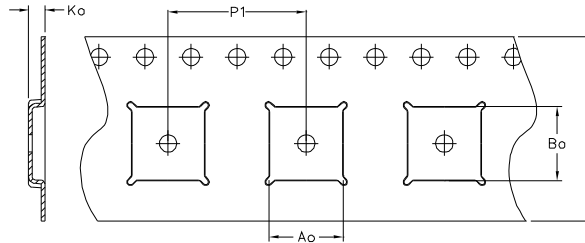
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# PQFN 5x6 Outline "B" Tape and Reel

## REEL DIMENSIONS

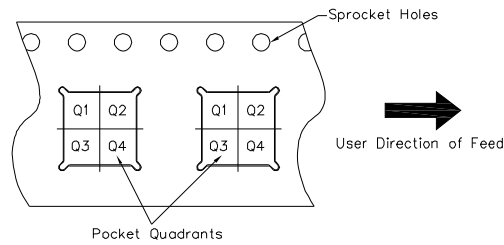


## TAPE DIMENSIONS



CODE	DESCRIPTION
$A_o$	Dimension design to accommodate the component width
$B_o$	Dimension design to accommodate the component length
$K_o$	Dimension design to accommodate the component thickness
$W$	Overall width of the carrier tape
$P1$	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	$A_o$ (mm)	$B_o$ (mm)	$K_o$ (mm)	$P1$ (mm)	$W$ (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial (per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
2/19/2015	<ul style="list-style-type: none"> <li>• Updated <math>E_{AS(L=1mH)} = 479mJ</math> on page 2</li> <li>• Updated note 10 "Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 31A</math>, <math>V_{GS} = 10V</math>". on page 2</li> </ul>