19-0784; Rev 1; 7/07

EVALUATION KIT AVAILABLE

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

General Description

The MAX8667/MAX8668 dual step-down converters with dual low-dropout (LDO) linear regulators are intended to power low-voltage microprocessors or DSPs in portable devices. They feature high efficiency with small external component size. The step-down converters are adjustable from 0.6V to 3.3V (MAX8668) or factory preset (MAX8667) with guaranteed output current of 600mA for OUT1 and 1200mA for OUT2. The 1.5MHz hysteretic-PWM control scheme allows for tiny external components and reduces no-load operating current to 100µA with all outputs enabled. Dual low-quiescent-current, low-noise LDOs operate down to 1.7V supply voltage. The MAX8667/MAX8668 have individual enables for each output, maximizing flexibility.

The MAX8667/MAX8668 are available in the space-saving, 3mm x 3mm, 16-pin thin QFN package.

Applications

Cell Phones/Smartphones

PDA and Palmtop Computers

Portable MP3 and DVD Players

Digital Cameras, Camcorders

PCMCIA Cards

Handheld Instruments

Features

- **Tiny, Thin QFN 3mm x 3mm Package**
- **Individual Enables**
- **Step-Down Converters**
  - **600mA Guaranteed Output Current on OUT1**
  - **1200mA Guaranteed Output Current on OUT2**
  - **Tiny Size 2.2µH Chip Inductor (0805)**
  - **Output Voltage from 0.6V to 3.3V (MAX8668)**
  - **Ultra-Fast Line and Load Transients**
  - **Low 25µA Supply Current Each**
- **LDOs**
  - **300mA Guaranteed**
  - **Low 1.7V Minimum Supply Voltage**
  - **Low Output Noise**

Ordering Information

PART	PKG CODE	TOP MARK
MAX8667ETEAA+	T1633-4	AEQ
MAX8667ETEAB+	T1633-4	AFI
MAX8667ETEAC+	T1633-4	AFM
MAX8667ETECQ+	T1633-4	AFN

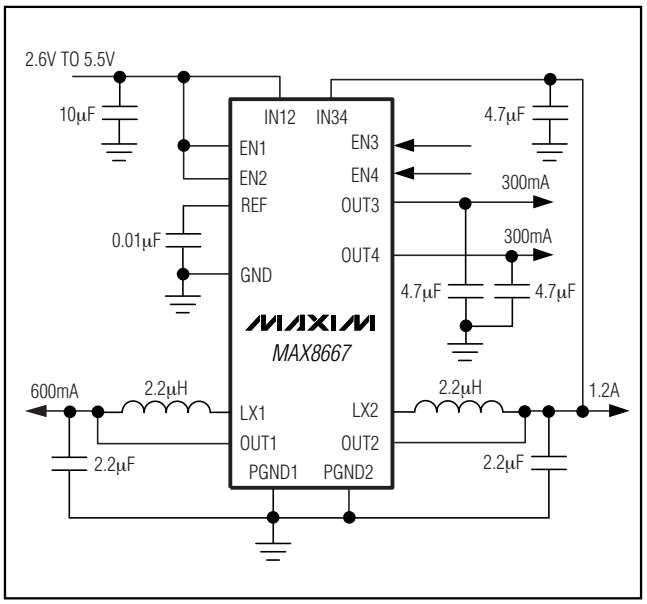
Note: *All MAX8667/MAX8668 parts are in a 16-pin, thin QFN, 3mm x 3mm package and operate in the -40°C to +85°C extended temperature range.*

+Denotes a lead-free package.

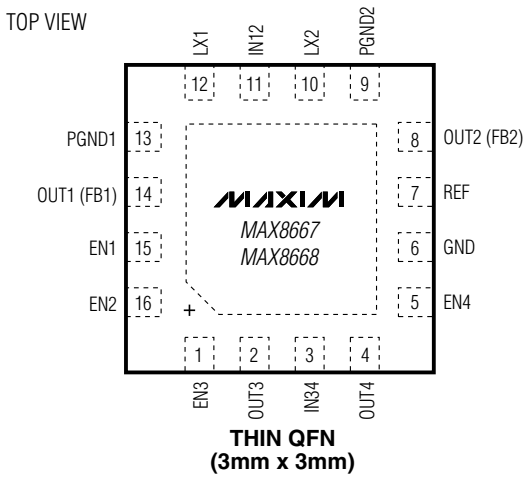
Ordering Information continued at the end of data sheet.

Selector Guide appears at the end of data sheet.

Typical Operating Circuit



Pin Configuration



THIN QFN (3mm x 3mm)

( ) ARE FOR THE MAX8668

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

ABSOLUTE MAXIMUM RATINGS

IN12, IN34, FB1, FB2, EN1, EN2, EN3, EN4, OUT1, OUT2, REF to GND.....-0.3V to +6.0V
OUT3, OUT4 to GND.....-0.3V to the lesser of + 6V or (V_{IN34} + 0.3V)
PGND1, PGND2 to GND .....-0.3V to +0.3V
LX1, LX2 Current .....1.5A RMS
LX1, LX2 to GND (Note 1).....-0.3V to (V_{IN12} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin, 3mm x 3mm Thin QFN
(derate 20.8mW/°C above +70°C).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX_ has internal clamp diodes to GND and IN12. Applications that forward bias these diodes should take care not to exceed the IC's package-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN34} = V_{IN12} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN34 Supply Range	$V_{IN12} \geq V_{IN34}$		1.7		5.5	V
IN12 Supply Range	MAX8668, $V_{IN12} \geq V_{IN34}$		2.6		5.5	V
IN12 Suppy Range	MAX8667, $V_{IN12} \geq V_{IN34}$		2.8		5.5	V
Shutdown Supply Current, I_{IN12} + I_{IN34}	V_{IN12} = V_{IN34} = 4.2V $V_{EN\_}$ = 0V	T_A = +25°C			1	µA
		T_A = +85°C		0.05		µA
No Load Supply Current, I_{IN12} + I_{IN34}	MAX8667ETEJS+, all regulators enabled			100	150	µA
UNDERVOLTAGE LOCKOUT						
IN12 UVLO	V_{IN12} rising		2.4	2.5	2.6	V
	V_{IN12} hysteresis			0.1		V
IN34 UVLO	V_{IN34} rising		1.5	1.6	1.7	V
	V_{IN34} hysteresis			0.1		V
THERMAL SHUTDOWN						
Threshold	T_A rising			+160		°C
Hysteresis				15		°C
REFERENCE						
Reference Bypass Output Voltage			0.591	0.600	0.609	V
REF Supply Rejection	2.6V ≤ (V_{IN12} = V_{IN34}) ≤ 5.5V			0.15		mV/V
LOGIC AND CONTROL INPUTS						
EN_ Input Low Level	1.7V ≤ V_{IN34} ≤ 5.5V 2.6V ≤ V_{IN12} ≤ 5.5V				0.4	V
EN_ Input High Level	1.7V ≤ V_{IN34} ≤ 5.5V 2.6V ≤ V_{IN12} ≤ 5.5V		1.44			V
EN_ Input Leakage Current	V_{IN12} = V_{IN34} = 5.5V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.001		
STEP-DOWN CONVERTERS						
Minimum Adjustable Output Voltage	MAX8668			0.6		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN34} = V_{IN12} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Adjustable Output Voltage	MAX8668			3.3		V
FB1, FB2 Regulation Voltage	MAX8668, no load, $V_{FB\_}$ falling	T_A = +25°C	0.588	0.600	0.612	V
		T_A = -40°C to +85°C	0.582	0.600	0.618	
OUT1, OUT2 Regulation Voltage	MAX8667ETEJS+, no load, $V_{OUT\_}$ falling	T_A = +25°C	1.274	1.300	1.326	V
		T_A = -40°C to +85°C	1.261	1.300	1.339	
FB1, FB2 Line Regulation	MAX8668, V_{IN12} = 2.6V to 5.5V			0.01		%/V
OUT1, OUT2 Line Regulation	MAX8667, V_{IN12} = 2.8V to 5.5V			0.05		%/V
FB1, FB2 Bias Current	MAX8668, shutdown mode			0.1		µA
	MAX8668, V_{FB1} = 0.5V			0.01		
OUT1 Current Limit	pMOSFET switch (I_{LIMP1})		700	900	1100	mA
	nMOSFET rectifier (valley current)		500	750	1000	
OUT2 Current Limit	pMOSFET switch (I_{LIMP2})		1333	1667	2000	mA
	nMOSFET rectifier (valley current)		1200	1500	1800	
OUT1 On-Resistance	pMOSFET switch, I_{LX1} = -400mA			0.3	0.6	Ω
	nMOSFET rectifier, I_{LX1} = 400mA			0.3	0.6	
OUT2 On-Resistance	pMOSFET switch, I_{LX2} = -400mA			0.12	0.27	Ω
	nMOSFET rectifier, I_{LX2} = 400mA			0.12	0.27	
Rectifier-Off Current Threshold (I_{LXOFF})				60	120	mA
LX Leakage Current	LX_ = 5.5V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.1		
Minimum On-Time				100		ns
Minimum Off-Time				50		ns
LDO REGULATORS						
Supply Current	Each LDO			20		µA
Output-Voltage Accuracy	1mA load, T_A = +25°C		-1.5		+1.5	%
	1mA to 300mA load		-3.0		+3.0	
Line Regulation	V_{IN34} = 3.6V to 5.5V, 1mA load			0.003		%/V
Dropout Voltage	V_{IN34} = 1.8V, 300mA load			130	250	mV
Current Limit	V_{OUT3}, V_{OUT4} 90% of nominal value		375	420	465	mA
Soft-Start Ramp Time	To 90% of final value			0.1		ms
Output Noise	100Hz to 100kHz, 30mA load, V_{OUT3} and V_{OUT4} = 2.8V			75		$µV_{RMS}$
Power-Supply Rejection Ratio	f < 1kHz, 30mA load			57		dB
Shutdown Output Resistance				1		kΩ
TIMING (See Figure 2)						
Power-On Time (t_{PWRON})	OUT1, OUT2			25		µs
	OUT3, OUT4			45		
Enable Time (t_{EN})	OUT1, OUT2			15		µs
	OUT3, OUT4			35		

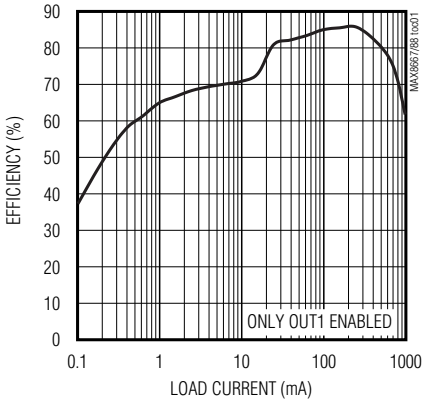
Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

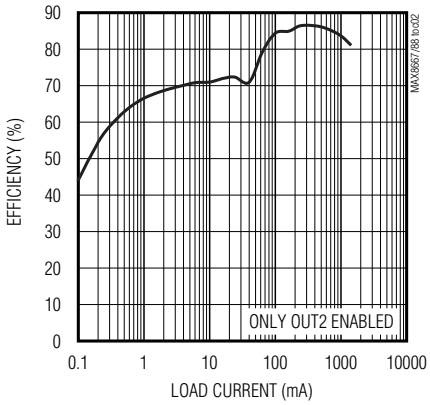
Typical Operating Characteristics

(V_{IN12} = V_{IN34} = 3.6V, circuit of Figure 4, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} = 2.8V, T_A = +25°C, unless otherwise noted.)

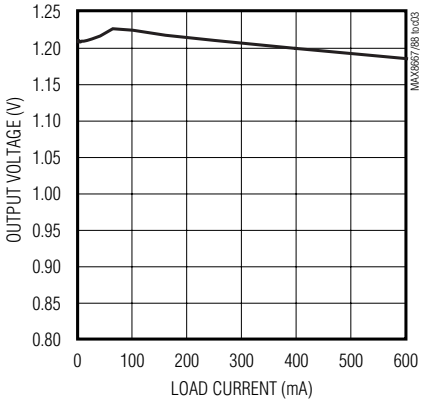
OUT1 EFFICIENCY vs. LOAD CURRENT (V_{OUT1} = 1.2V)



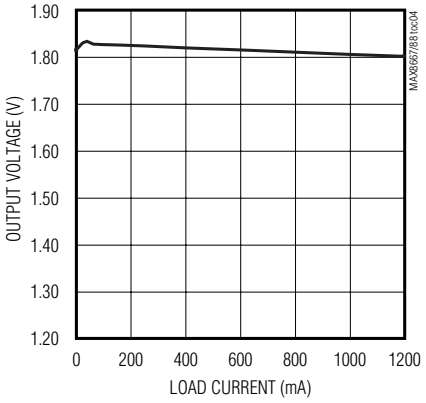
OUT2 EFFICIENCY vs. LOAD CURRENT (V_{OUT2} = 1.8V)



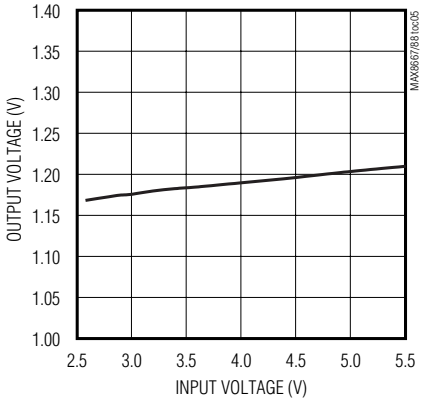
OUT1 LOAD REGULATION



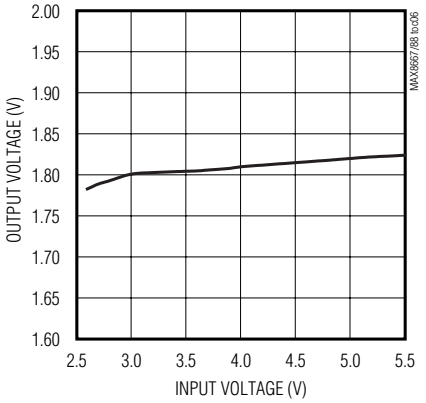
OUT2 LOAD REGULATION



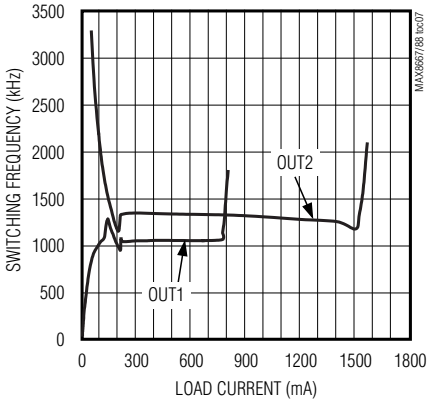
OUT1 OUTPUT VOLTAGE vs. INPUT VOLTAGE (600mA LOAD)



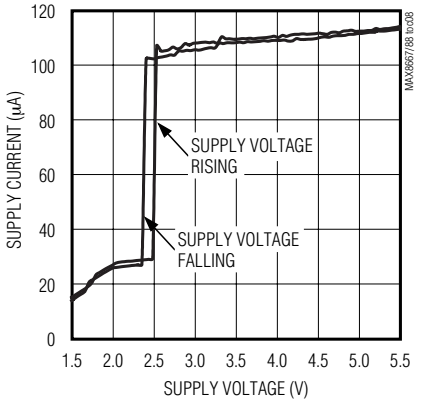
OUT2 OUTPUT VOLTAGE vs. INPUT VOLTAGE (1200mA LOAD)



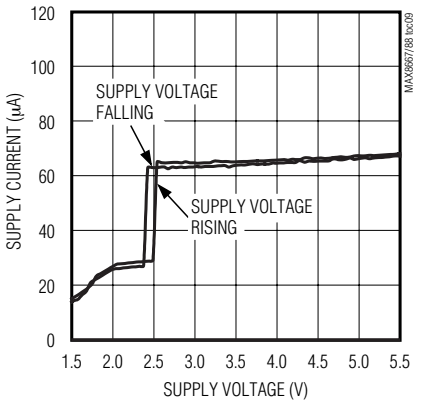
SWITCHING FREQUENCY vs. LOAD CURRENT



NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE ALL REGULATOR ENABLED



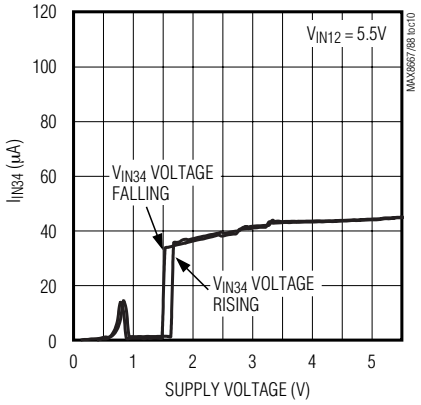
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE OUT1 AND OUT2 ONLY



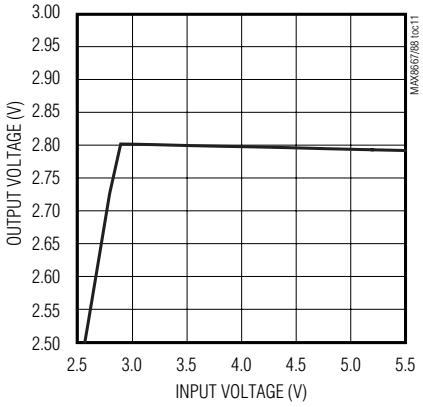
Typical Operating Characteristics (continued)

(V_{IN12} = V_{IN34} = 3.6V, circuit of Figure 4, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} = 2.8V, T_A = +25°C, unless otherwise noted.)

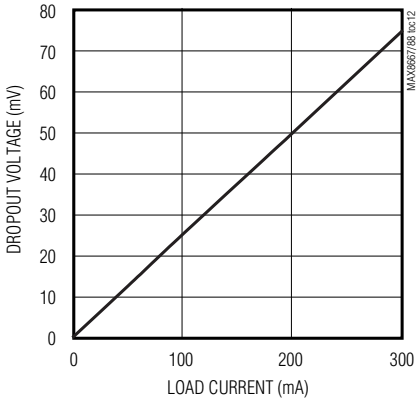
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE OUT3 AND OUT4 ONLY



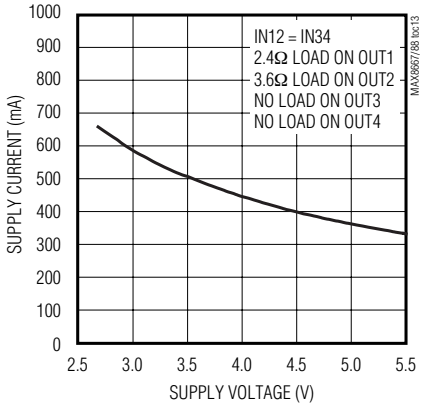
OUT3 OUTPUT VOLTAGE vs. INPUT VOLTAGE (300mA LOAD)



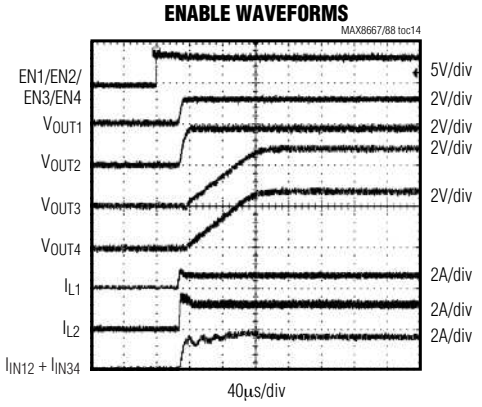
OUT3 DROPOUT VOLTAGE vs. LOAD CURRENT



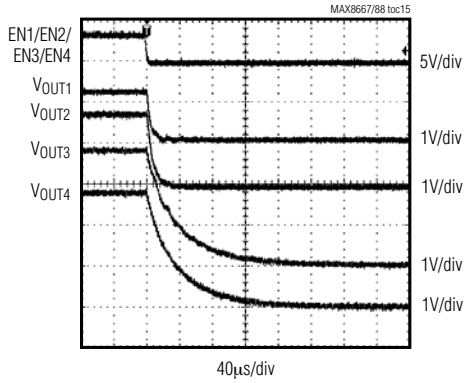
SUPPLY CURRENT vs. SUPPLY VOLTAGE



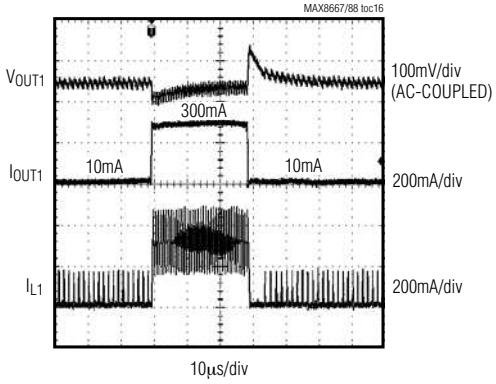
ENABLE WAVEFORMS



SHUTDOWN WAVEFORMS



OUT1 LOAD TRANSIENT

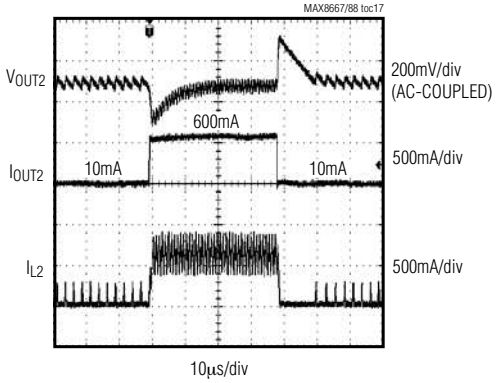


1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

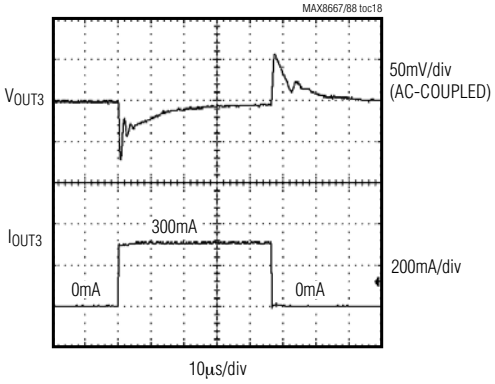
Typical Operating Characteristics (continued)

(V_{IN12} = V_{IN34} = 3.6V, circuit of Figure 4, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} = 2.8V, T_A = +25°C, unless otherwise noted.)

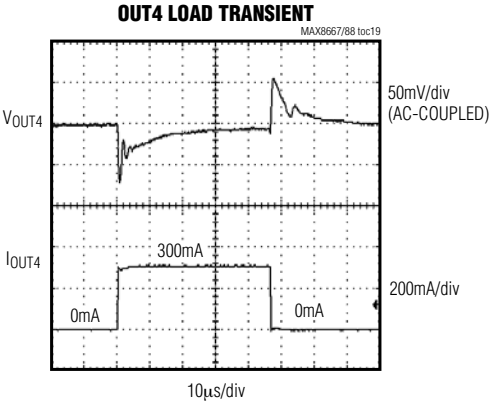
OUT2 LOAD TRANSIENT



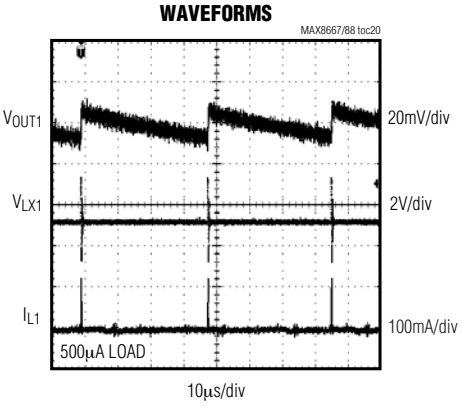
OUT3 LOAD TRANSIENT



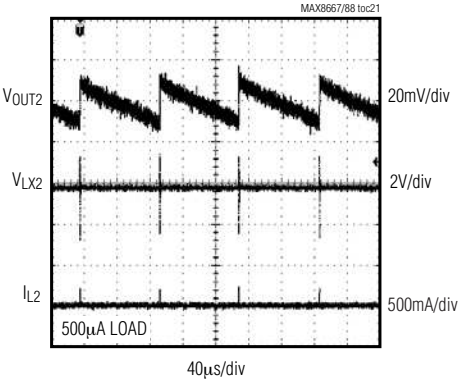
OUT4 LOAD TRANSIENT



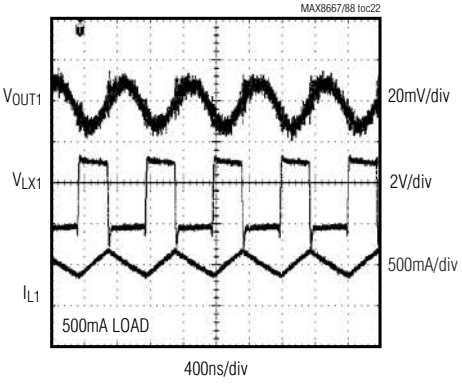
OUT1 LIGHT-LOAD SWITCHING WAVEFORMS



OUT2 LIGHT-LOAD SWITCHING WAVEFORMS



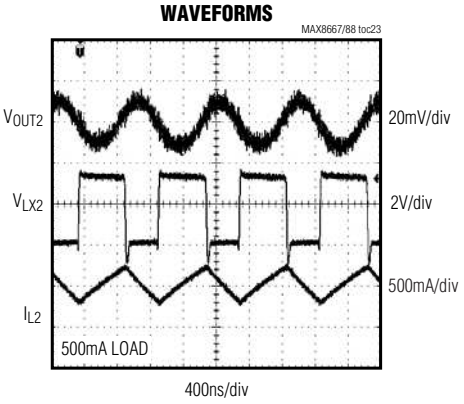
OUT1 HEAVY-LOAD SWITCHING WAVEFORMS



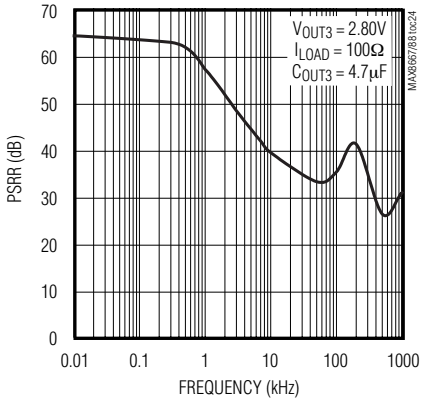
Typical Operating Characteristics (continued)

(V_{IN12} = V_{IN34} = 3.6V, circuit of Figure 4, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} = 2.8V, T_A = +25°C, unless otherwise noted.)

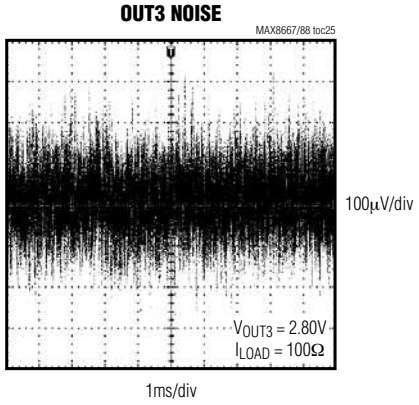
OUT2 HEAVY-LOAD SWITCHING WAVEFORMS



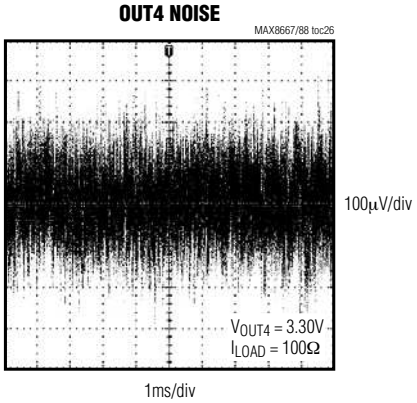
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OUT3 NOISE



OUT4 NOISE



1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

Pin Description

PIN	NAME		FUNCTION
	MAX8667	MAX8668	
1	EN3	EN3	Enable Input for Regulator 3. Drive EN3 high or connect to IN34 to turn on regulator 3. Drive low to turn off regulator 3 and reduce input quiescent current.
2	OUT3	OUT3	Output of Regulator 3. Bypass OUT3 with a 4.7µF ceramic capacitor to GND. OUT3 is discharged to GND through an internal 1kΩ in shutdown.
3	IN34	IN34	Input Voltage for LDO Regulators 3 and 4. Supply voltage range is from 1.7V to 5.5V. This supply voltage must not exceed V_{IN12}. Connect a 4.7µF or larger ceramic capacitor from IN34 to ground.
4	OUT4	OUT4	Output of Regulator 4. Bypass OUT4 with a 4.7µF ceramic capacitor to GND. OUT4 is discharged to GND through an internal 1kΩ in shutdown.
5	EN4	EN4	Enable Input for Regulator 4. Drive EN4 high or connect to IN34 to turn on regulator 4. Drive low to turn off regulator 4 and reduce input quiescent current.
6	GND	GND	Ground
7	REF	REF	Reference Output. Bypass REF with a 0.01µF ceramic capacitor to GND.
8	OUT2	—	Feedback Input for Regulator 2. Connect OUT2 directly to the output of step-down regulator 2.
	—	FB2	Feedback Input for Regulator 2. Connect FB2 to the center of a resistor feedback divider between the output of regulator 2 and ground to set the output voltage. See the *Setting the Output Voltages and Voltage Positioning* section.
9	PGND2	PGND2	Power Ground for Step-Down Regulator 2
10	LX2	LX2	Inductor Connection for Regulator 2
11	IN12	IN12	Input Voltage for Step-Down Regulators 1 and 2. Supply voltage range is from 2.6V to 5.5V. This supply voltage must not be less than V_{IN34}. Connect a 10µF or larger ceramic capacitor from IN12 to ground.
12	LX1	LX1	Inductor Connection for Regulator 1
13	PGND1	PGND1	Power Ground for Step-Down Regulator 1
14	OUT1	—	Feedback Input for Regulator 1. Connect OUT1 directly to the output of step-down regulator 1.
	—	FB1	Feedback Input for Regulator 1. Connect FB1 to the center of a resistor feedback divider between the output of regulator 1 and ground to set the output voltage. See the *Setting the Output Voltages and Voltage Positioning* section.
15	EN1	EN1	Enable Input for Regulator 1. Drive EN1 high or connect to IN12 to turn on step-down regulator 1. Drive low to turn off the regulator and reduce input quiescent current.
16	EN2	EN2	Enable Input for Regulator 2. Drive EN2 high or connect to IN12 to turn on step-down regulator 2. Drive low to turn off the regulator and reduce input quiescent current.
—	EP	EP	Exposed Paddle. Connect to GND, PGND1, PGND2, and circuit ground.

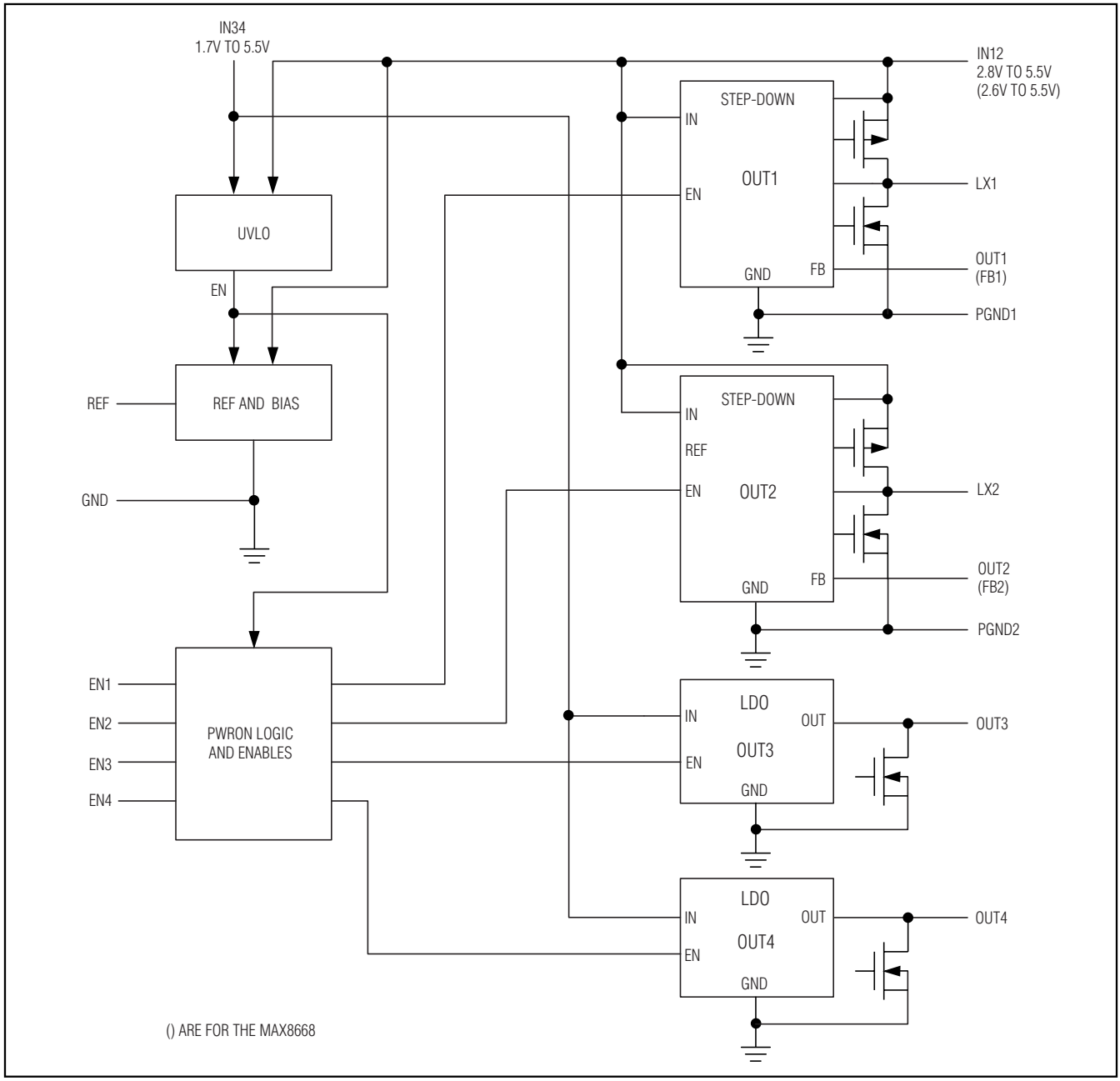


Figure 1. Functional Diagram

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

Detailed Description

The MAX8667/MAX8668 dual step-down converters with dual low-dropout (LDO) linear regulators are intended to power low-voltage microprocessors or DSPs in portable devices. They feature high efficiency with small external component size. The step-down outputs are adjustable from 0.6V to 3.3V (MAX8668) or factory preset (MAX8667) with guaranteed output current of 600mA for OUT1 and 1200mA for OUT2. The 1.5MHz hysteretic-PWM control scheme allows for tiny external components and reduces no-load operating current to 100µA (typ) with all regulators enabled. Dual, low-quiescent-current, low-noise LDOs operate down to 1.7V supply voltage. The MAX8667/MAX8668 have individual enable inputs for each output to facilitate any supply sequencing.

Step-Down DC-DC Regulators (OUT1, OUT2)

Step-Down Regulator Architecture

The MAX8667/MAX8668 step-down regulators are optimized for high-efficiency voltage conversion over a wide load range, while maintaining excellent transient response, minimizing external component size, and minimizing output voltage ripple. The DC-DC converters (OUT1, OUT2) also feature an optimized on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency. The MAX8667/MAX8668 utilize a proprietary hysteretic-PWM control scheme that switches with nearly fixed frequency at up to 1.5MHz allowing for ultra-small external components. The step-down converter output current is guaranteed up to 600mA for OUT1 and 1200mA for OUT2.

When the step-down converter output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning the high-side p-channel MOSFET switch on. This switch remains on until the minimum on-time (t_{ON}) expires and the output voltage is in regulation or the current-limit threshold ($I_{LIMP\_}$) is exceeded. Once off, the high-side switch remains off until the minimum off-time (t_{OFF}) expires and the output voltage again falls below the regulation threshold. During this off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on or the inductor current reduces to the rectifier-off current threshold (I_{LXOFF} = 60mA typ). The internal synchronous rectifier eliminates the need for an external Schottky diode.

Input Supply and Undervoltage Lockout

The input voltage range of step-down regulators OUT1 and OUT2 is 2.6V to 5.5V. This supply voltage must be greater than or equal to the LDO supply voltage (V_{IN34}).

A UVLO circuit prevents step-down regulators OUT1 and OUT2 from switching when the supply voltage is too low to guarantee proper operation. When V_{IN12} falls below 2.4V (typ), OUT1 and OUT2 are shut down. OUT1 and OUT2 turn on and begin soft-start when V_{IN12} rises above 2.5V (typ).

Soft-Start

When initially powered up, or enabled with EN_, the step-down regulators soft-start by gradually ramping up the output voltage. This reduces inrush current during startup. See the startup waveforms in the *Typical Operating Characteristics* section.

Current Limit

The MAX8667/MAX8668 limit the peak inductor current of the p-channel MOSFET ($I_{LIMP\_}$). A valley current limit is used to protect the step-down regulators during severe overload and output short-circuit conditions. When the peak current limit is reached, the internal p-channel MOSFET turns off and remains off until the output drops below regulation, the inductor current falls below the valley current-limit threshold, and the minimum off-time has expired.

Voltage Positioning

The OUT1 and OUT2 output voltages and voltage positioning of the MAX8668 are set by a resistor network connected to FB_. With this configuration, a portion of the feedback signal is sensed on the switched side of the inductor, and the output voltage droops slightly as the load current is increased due to the DC resistance of the inductor. This output voltage droop is known as voltage positioning. Voltage positioning allows the load regulation to be set to match the voltage droop during a load transient, reducing the peak-to-peak output voltage deviation during a load transient, and reducing the output capacitance requirements.

Dropout

As the input voltage approaches the output voltage, the duty cycle of the p-channel MOSFET reaches 100%. In this state, the p-channel MOSFET is turned on constantly (not switching), and the dropout voltage is the voltage drop due to the output current across the on-resistance of the internal p-channel MOSFET (R_{PCH}) and the inductor's DC resistance (R_L):

$$V_{DO} = I_{LOAD}(R_{PCH} + R_L)$$

LDO Linear Regulators (OUT3, OUT4)

The MAX8667/MAX8668 contain two low-dropout linear regulators (LDOs), OUT3 and OUT4. The LDO output voltages are factory preset, and each LDO supplies

loads up to 300mA. The LDOs include an internal reference, error amplifier, p-channel pass transistor, and internal voltage-dividers. Each error amplifier compares the reference voltage to the output voltage (divided by the internal voltage-divider) and amplifies the difference. If the divided feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the outputs and increasing the output voltage. If the divided feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

Input Supply and Undervoltage Lockout

The input voltage range of LDO regulators OUT3 and OUT4 is 1.7V to 5.5V. This supply voltage must be less than or equal to the voltage applied to IN12 ($V_{IN34} \leq V_{IN12}$).

An undervoltage lockout circuit turns off the LDO regulators when the input supply voltage is too low to guarantee proper operation. When V_{IN34} falls below 1.5V (typ), OUT3 and OUT4 are shut down. OUT3 and OUT4 turn on and begin soft-start when V_{IN34} rises above 1.6V (typ).

Soft-Start

When initially powered up, or enabled with EN_, the LDOs soft-start by gradually ramping up the output voltage. This reduces inrush current during startup. The soft-start ramp time is typically 100µs from the start of the soft-start ramp to the output reaching its nominal regulation voltage.

Current Limit

The OUT3 and OUT4 output current is limited to 375mA (min). If the output current exceeds the current limit, the corresponding LDO output voltage drops.

Dropout

The maximum dropout voltage for the linear regulators is 250mV at 300mA load. To avoid dropout, make sure the IN34 supply voltage is at least 250mV higher than the highest LDO output voltage.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the MAX8667/MAX8668. Thermal-protection circuits monitor the die temperature. If the die temperature exceeds +160°C, the IC is shut down, allowing the IC to cool. Once the IC has cooled by 15°C, the IC is enabled again. This results in a pulsed output during continuous thermal-overload conditions. The thermal-overload protection protects the MAX8667/MAX8668 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See the *Thermal Considerations* section for more information.

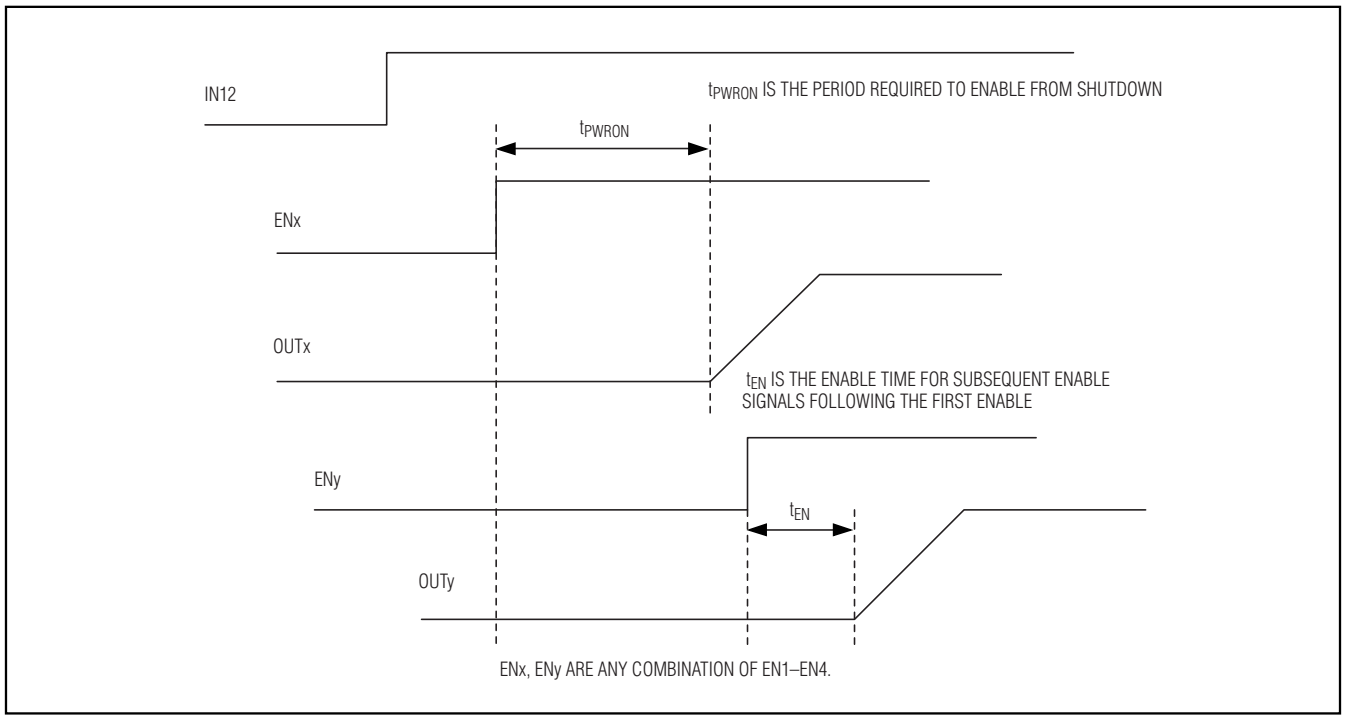


Figure 2. Timing Diagram

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

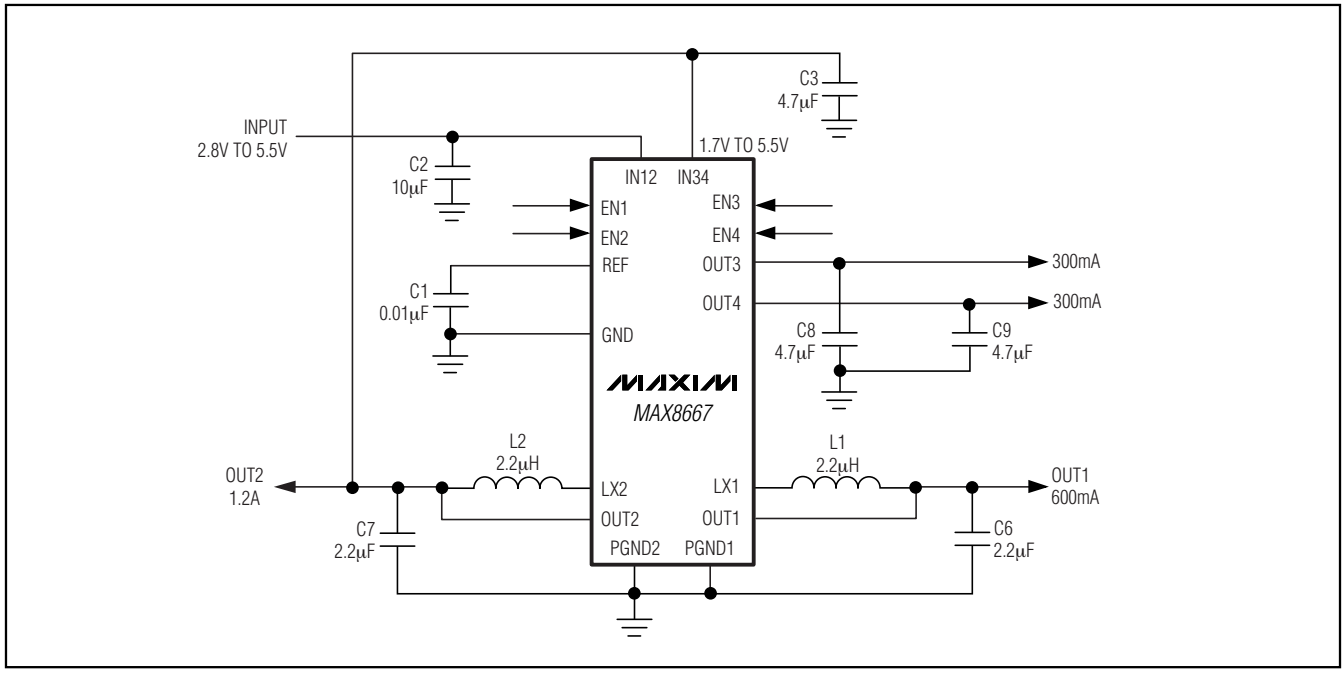


Figure 3. MAX8667 Typical Application Circuit

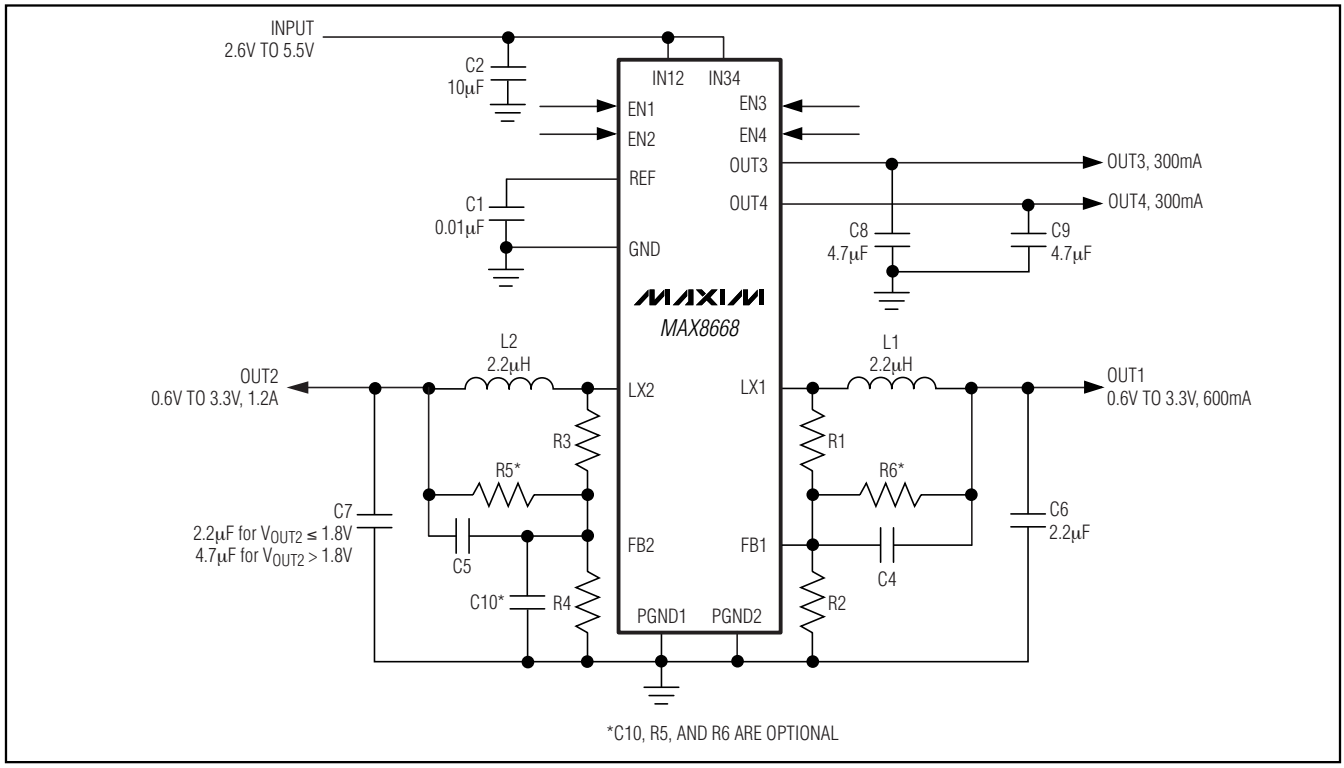


Figure 4. MAX8668 Typical Application Circuit

Applications Information

Setting the Output Voltages and Voltage Positioning

The LDO output voltages of the MAX8667/MAX8668, and the step-down outputs of the MAX8667 are factory preset. See the *Selector Guide* to find the part number corresponding to the desired output voltages.

The OUT1 and OUT2 output voltages of the MAX8668 are set by a resistor network connected to FB_ as shown in Figure 5. With this configuration, a portion of the feedback signal is sensed on the switched side of the inductor (LX), and the output voltage droops slightly as the load current is increased due to the DC resistance of the inductor (DCR). This allows the load regulation to be set to match the voltage droop during a load transient (voltage positioning), reducing the peak-to-peak output-voltage deviation during a load transient, and reducing the output capacitance requirements.

For the simplest method of setting the output voltage, R6 is not installed. Choose the value of R2 (a good starting value is 100kΩ), and then calculate the value of R1 as follows:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} is the feedback regulation voltage (0.6V).

With the voltage set in this manner, the voltage positioning depends only on the DCR, and the maximum output voltage droop is:

$$\Delta V_{OUT(MAX)} = DCR \times I_{OUT(MAX)}$$

Setting the Output Voltages with Reduced Voltage Positioning

To obtain less voltage positioning than described in the previous section, use the following procedure for setting the output voltages. The OUT1 and OUT2 output voltages and voltage positioning of the MAX8668 are set by a resistor network connected to FB_ as shown in Figure 5.

To set the output voltage (V_{OUT}), first select a value for R2 (a good starting value is 100kΩ). Then calculate the value of R_{EQ} (the equivalent parallel resistance of R1 and R6) as follows:

$$R_{EQ} = \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \times R2$$

where V_{FB} is the feedback-regulation voltage (0.6V).

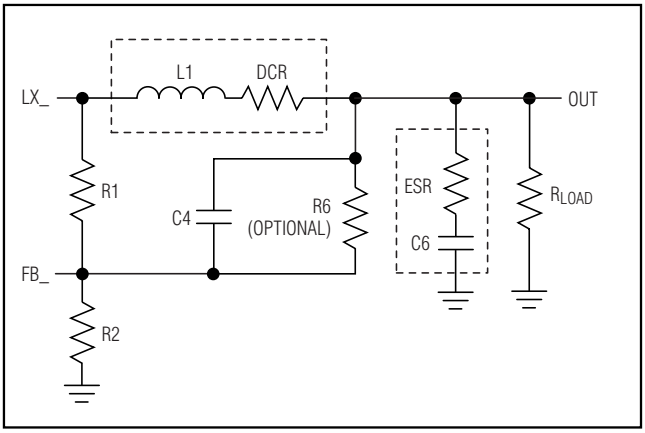


Figure 5. MAX8668 Feedback Network

Calculate the factor m based on the desired load-regulation improvement:

$$m = \frac{I_{OUT(MAX)} \times DCR}{\Delta V_{OUT(DESIRED)}}$$

where $I_{OUT(MAX)}$ is the maximum output current, DCR is the inductor series resistance, and $\Delta V_{OUT(DESIRED)}$ is the maximum allowable droop in the output voltage at full load. The calculated value for m must be between 1.1 and 2; m = 2 results in a 2x improvement in load regulation.

Now calculate the values of R1 and R6 as follows:

$$R1 = R_{EQ} \times m$$

$$R6 = R_{EQ} \times \frac{m}{m-1}$$

The value of R1 should always be lower than the value of R6.

Power-Supply Sequencing

The MAX8667/MAX8668 have individual enable inputs for each regulator to allow complete control over the power sequencing. When all EN_ inputs are low, the IC is in low-power shutdown mode, reducing the supply current to less than 1µA. After one of the EN_ inputs asserts high, the corresponding regulator begins soft-start after a delay of t_{EN} (see Figure 2). The first output enabled from shutdown mode or initially powering up the IC has a longer delay (t_{PWRON}) as the IC exits the low-power shutdown mode.

Inductor Selection

The MAX8667/MAX8668 step-down converters operate with inductors between 2.2µH and 4.7µH. Low inductance values are physically smaller, but require faster switching, resulting in some efficiency loss. The inductor's DC current rating must be high enough to account

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

Table 1. Recommended Inductors

MANUFACTURER	INDUCTOR	L (µH)	R_L (mΩ)	CURRENT RATING (A)	L x W x H (mm)
FDK	MIPF2016	2.2	110	1.1	2.0 x 1.6 x 1.0
FDK	MIPF2520D	2.2	80	1.3	2.5 x 2.0 x 1.0
Murata	LQH32CN2R2M5	2.2	97	0.79	3.2 x 2.5 x 1.55
	LQM31P	2.2	220	0.9	3.2 x 1.6 x 0.95
Sumida	CDRH2D09	2.2	120	0.44	3.2 x 3.2 x 1.0
TDK	GLF251812T	2.2	200	0.6	2.5 x 1.8 x 1.35
TOKO	D2812C	2.2	140	0.77	2.8 x 2.8 x 1.2
TOKO	MDT2520-CR	2.2	80	0.7	2.5 x 2.0 x 1.0
Wurth	TPC Series	2.2	55	1.8	4.0 x 4.0 x 1.1
	TPC Series	4.7	124	1.35	4.0 x 4.0 x 1.1
Taiyo Yuden	CB2518T	2.2	90	0.51	2.5 x 1.8 x 2.0

for peak ripple current and load transients. The step-down converter's unique architecture has minimal current overshoot during startup and load transients and in most cases, an inductor capable of 1.3x the maximum load current is acceptable.

For output voltages above 2V, when light-load efficiency is important, the minimum recommended inductor is 2.2µH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA) and minimal load regulation, keep the inductor resistance as small as possible. For light-load applications (up to 200mA), higher resistance is acceptable with very little impact on performance.

Capacitor Selection

Input Capacitors

The input capacitor for the step-down converters (C2 in Figures 3 and 4) reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C2 at the switching frequency should be very low. Surface-mount ceramic capacitors are a good choice due to their small size and low ESR. Make sure the capacitor maintains its capacitance over temperature and DC bias. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well. A 10µF ceramic capacitor is recommended.

A 4.7µF ceramic capacitor is recommended for the LDO input capacitor (C3 in Figure 3).

Step-Down Output Capacitors

The step-down output capacitors (C6 and C7 in Figures 3 and 4) are required to keep the output-voltage ripple small and to ensure regulation loop stability. These capacitors must have low impedance at the switching frequency. Surface-mount ceramic capacitors are a good choice due to their small size and low ESR. Make sure the capacitor maintains its capacitance over temperature and DC bias. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well. The output capacitance can be very low. For most applications, a 2.2µF ceramic capacitor is sufficient. For C7 of the MAX8668, a 2.2µF ($V_{OUT2} \le 1.8V$) or a 4.7µF ($V_{OUT2} > 1.8V$) ceramic capacitor is recommended. For optimum load-transient performance and very low output ripple, the output capacitor value in µF should be equal to or greater than the inductor value in µH.

Feed-Forward Capacitor

The feed-forward capacitors on the MAX8668 (C4 and C5 in Figure 4) set the feedback loop response, control the switching frequency, and are critical in obtaining the best efficiency possible. Small X7R and C0G ceramic capacitors are recommended.

For OUT1, calculate the value of C4 as follows:

$$C4 = 1.2 \times 10^{-5}(s/V) \times (V_{OUT} / R1)$$

For OUT2, calculate the value of C5 and C10 as follows:

$$C_{ff} = 1.2 \times 10^{-5}(s/V) \times (V_{OUT} / R3)$$

$$C_{ff} = C5 + (C10 / 2)$$

$$(C10 / C5) + 1 = (V_{OUT} / V_{FB}), \text{ where } V_{FB} \text{ is } 0.6V.$$

Rearranging the formulas:

$$C10 = 2 \times C_{ff} \times (V_{OUT} - V_{FB})/(V_{OUT} + V_{FB})$$

$$C5 = C_{ff} - (C10 / 2)$$

C10 is needed if V_{OUT} > 1.5V or V_{IN12} can be less than V_{OUT} / 0.65.

LDO Output Capacitor and Stability

Connect a 4.7µF ceramic capacitor between OUT3 and GND, and a second 4.7µF ceramic capacitor from OUT4 to GND. For a constant loading above 10mA, the output capacitors can be reduced to 2.2µF. The equivalent series resistance (ESR) of the LDO output capacitors affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stable operation and optimum transient response. Surface-mount ceramic capacitors have very low ESR and are commonly available. Connect these capacitors as close as possible to the IC's pins to minimize PCB trace inductance.

Thermal Considerations

The maximum package power dissipation of the MAX8667/MAX8668 is 1667mW. Make sure the power dissipated by the MAX8667/MAX8668 does not exceed this rating. The total IC power dissipation is the sum of the power dissipation of the four regulators:

$$P_D = P_{D1} + P_{D2} + P_{D3} + P_{D4}$$

Estimate the OUT1 and OUT2 power dissipations as follows:

$$P_{D1} = I_{OUT1} \times V_{OUT1} \times \frac{1-\eta}{\eta}$$

$$P_{D2} = I_{OUT2} \times V_{OUT2} \times \frac{1-\eta}{\eta}$$

where R_L is the inductor's DC resistance, and η is the efficiency (see the *Typical Operating Characteristics* section).

Calculate the OUT3 and OUT4 power dissipations as follows:

$$P_{D3} = I_{OUT3} \times (V_{IN34} - V_{OUT3})$$

$$P_{D4} = I_{OUT4} \times (V_{IN34} - V_{OUT4})$$

The maximum junction temperature of the MAX8667/MAX8668 is +150°C. The junction-to-case thermal resistance (θ_{JC}) of the MAX8667/MAX8668 is 6.9°C/W. When mounted on a single-layer PCB, the junction to ambient thermal resistance (θ_{JA}) is about 64°C/W. Mounted on a multilayer PCB, θ_{JA} is about 48°C/W. Calculate the junction temperature of the MAX8667/MAX8668 as follows:

$$T_J = T_A + P_D \times \theta_{JA}$$

where T_A is the maximum ambient temperature. Make sure the calculated value of T_J does not exceed the +150°C maximum.

PCB Layout

High switching frequencies and relatively large peak currents make PCB layout a very important aspect of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the input capacitors as close as possible to the IN_ and PGND_ pins. Connect the inductor and output capacitors as close as possible to the IC and keep the traces short, direct, and wide.

The feedback network traces are sensitive to inductor magnetic field interference. Route these traces away from the inductors and noisy traces such as LX. Keep the feedback components close to the FB_ pin.

Connect GND and PGND_ to the ground plane. Connect the exposed paddle to the ground plane with one or more vias to help conduct heat away from the IC.

Refer to the MAX8668 evaluation kit for a PCB layout example.

1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

Ordering Information (continued)

PART	PKG CODE	TOP MARK
MAX8667ETEHR+	T1633-4	AFJ
MAX8667ETEJS+	T1633-4	AFQ
MAX8668ETEA+	T1633-4	AER
MAX8668ETEP+	T1633-4	AFK
MAX8668ETEQ+	T1633-4	AFR
MAX8668ETET+	T1633-4	AFS
MAX8668ETEU+	T1633-4	AFL
MAX8668ETEV+	T1633-4	AFT
MAX8668ETEW+	T1633-4	AFU
MAX8668ETEX+	T1633-4	AFV

All MAX8667/MAX8668 parts are in a 16-pin, thin QFN, 3mm x 3mm package and operate in the -40°C to = +85°C extended temperature range.

+Denotes a lead-free package.

Selector Guide

PART	OUT1 (V)	OUT2 (V)	OUT3 (V)	OUT4 (V)
MAX8667ETEAA+	1.20	1.80	2.80	2.80
MAX8667ETEAB+	1.20	1.80	2.85	2.85
MAX8667ETEAC+	1.20	1.80	1.20	1.20
MAX8667ETECQ+	1.60	1.80	2.80	1.20
MAX8667ETEHR+	1.80	1.20	2.60	2.80
MAX8667ETEJS+	1.30	1.30	3.30	2.70
MAX8668ETEA+	ADJ	ADJ	2.80	2.80
MAX8668ETEP+	ADJ	ADJ	3.30	1.80
MAX8668ETEQ+	ADJ	ADJ	2.80	1.20
MAX8668ETET+	ADJ	ADJ	3.30	3.30
MAX8668ETEU+	ADJ	ADJ	3.30	2.80
MAX8668ETEV+	ADJ	ADJ	3.30	2.50
MAX8668ETEW+	ADJ	ADJ	3.30	3.00
MAX8668ETEX+	ADJ	ADJ	2.80	1.80

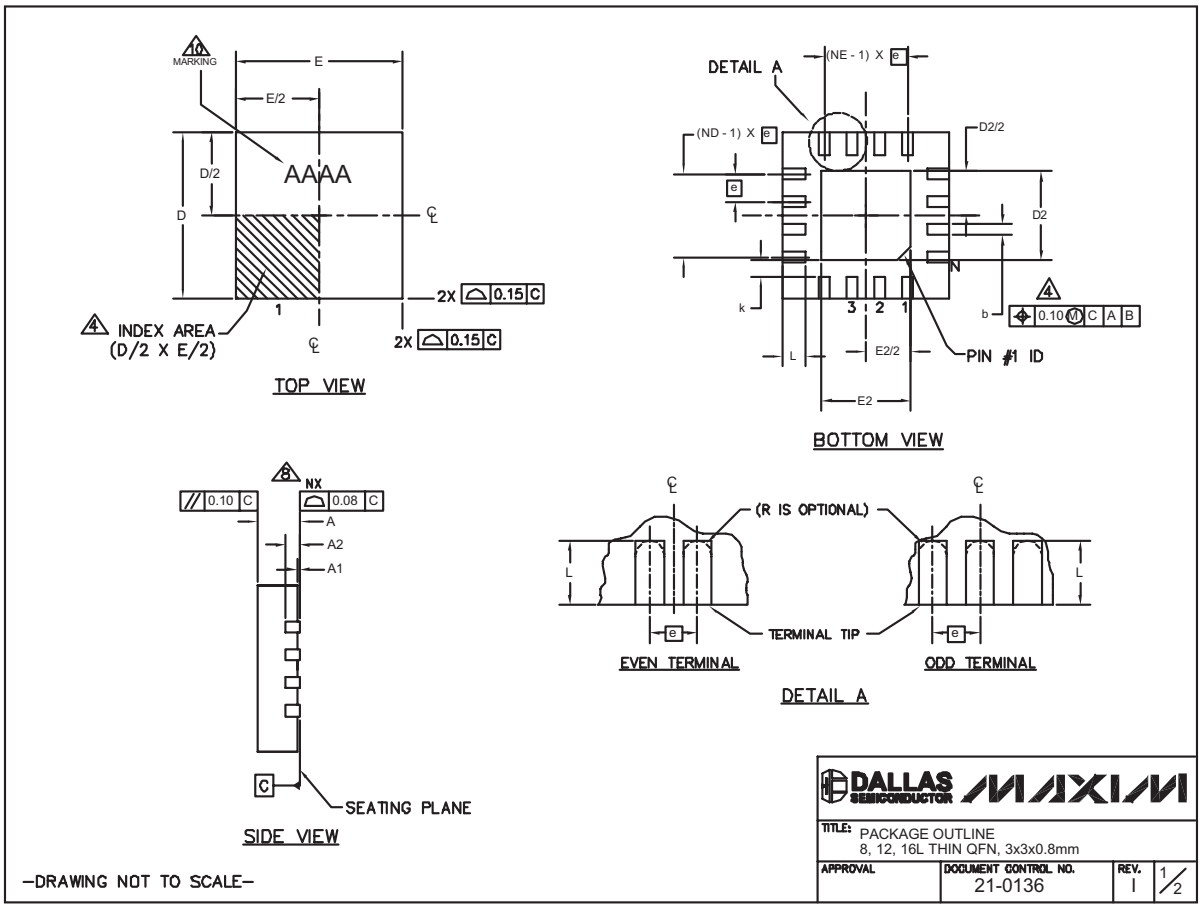
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



1.5MHz Dual Step-Down DC-DC Converters with Dual LDOs and Individual Enables

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	I	2/2

Revision History

Pages changed at Rev 1: 1, 12, 14, 18

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