Normally – OFF Silicon Carbide Junction Transistor

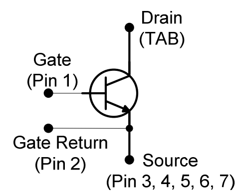
V_{DS}	=	1200 V
$R_{DS(ON)}$	=	1.5 Ω
$I_{D\ (@\ 25°C)}$	=	2 A
$h_{FE\ (@\ 25°C)}$	=	100

Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

7L D2PAK (TO-263-7L)



Please note: The Source and Gate Return pins are not exchangeable. Their exchange might lead to malfunction.

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 25°C	2	A	
Continuous Gate Current	I_G		0.1	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175°C, Clamped Inductive Load	$I_{D,max}$ = 2 @ $V_{DS} \leq V_{DSmax}$	A	Fig. 9
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175°C, I_G = 0.2 A, V_{DS} = 800 V, Non Repetitive	> 20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Storage Temperature	T_{stg}		-55 to 175	°C	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 1 A, T_j = 25 °C		1.5		Ω	
Gate – Source Saturation Voltage	$V_{GS,SAT}$	I_D = 1 A, I_D/I_G = 40, T_j = 25 °C I_D = 1 A, I_D/I_G = 30, T_j = 175 °C		3.45 3.22		V	Fig. 4
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 1 A, T_j = 25 °C		100		–	Fig. 2
B: Off State							
Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 25 °C		0.01		μA	Fig. 5
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	
C: Thermal							
Thermal resistance, junction - case	R_{thJC}			4.83		°C/W	Fig. 7

Section III: Figures

A: Static Characteristics

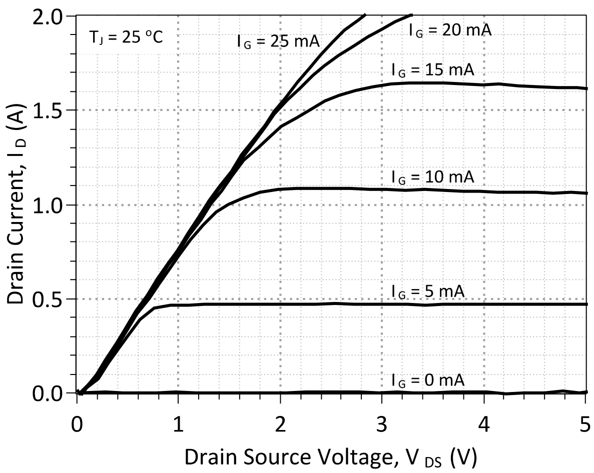


Figure 1: Typical Output Characteristics at 25 °C

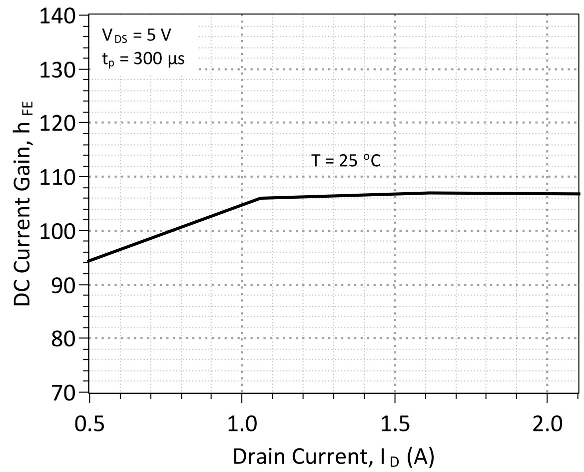


Figure 2: DC Current Gain vs. Drain Current

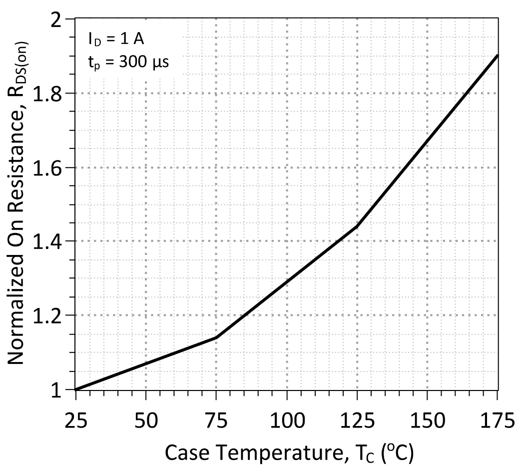


Figure 3: On-Resistance vs. Temperature

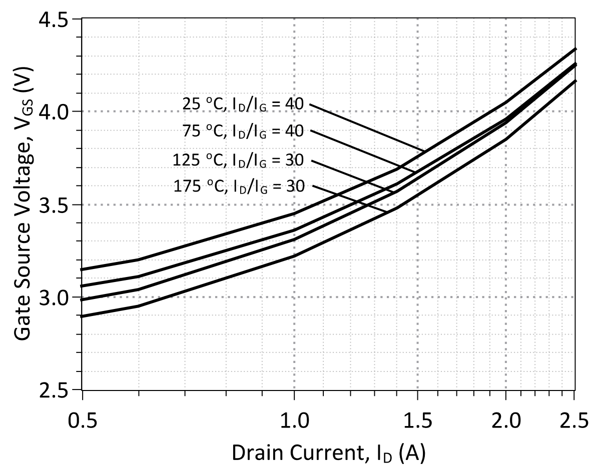


Figure 4: Typical Gate – Source Saturation Voltage

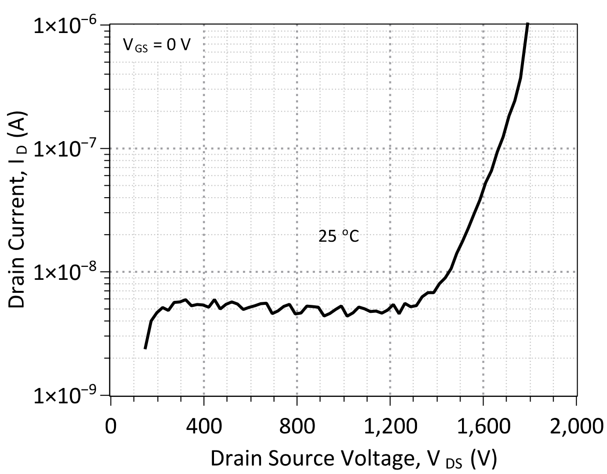


Figure 5: Typical Blocking Characteristics

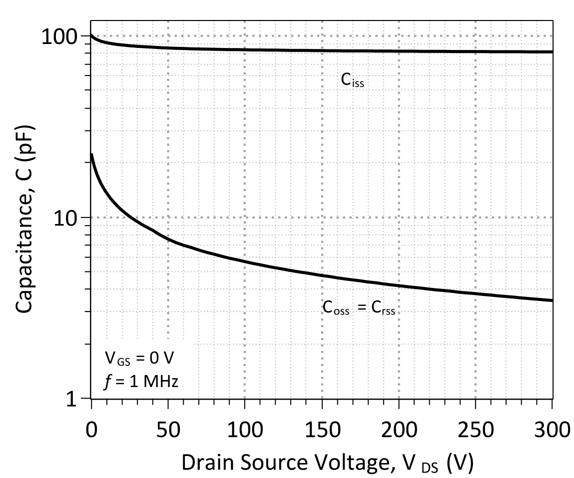


Figure 6: Input, Output, and Reverse Transfer Capacitance

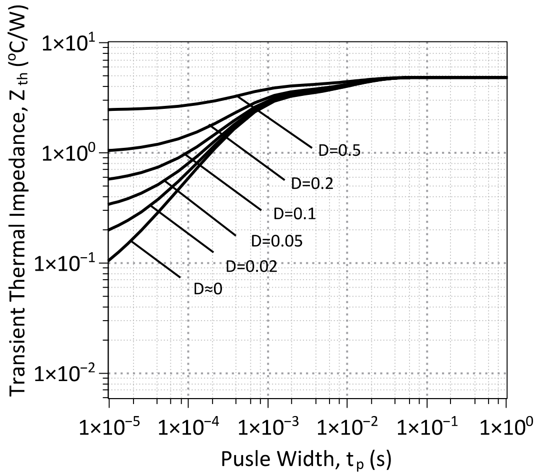


Figure 7: Transient Thermal Impedance

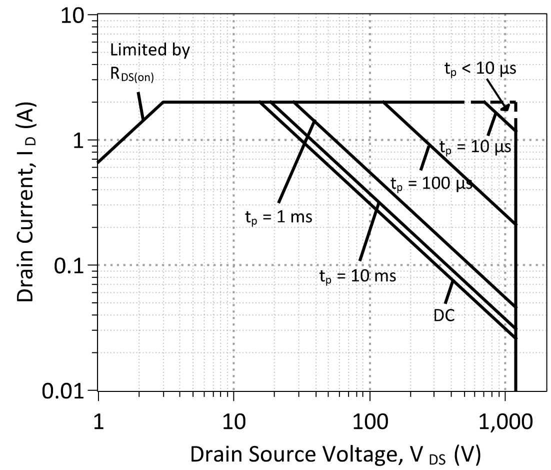


Figure 8: Forward Bias Safe Operating Area at T_c= 25°C

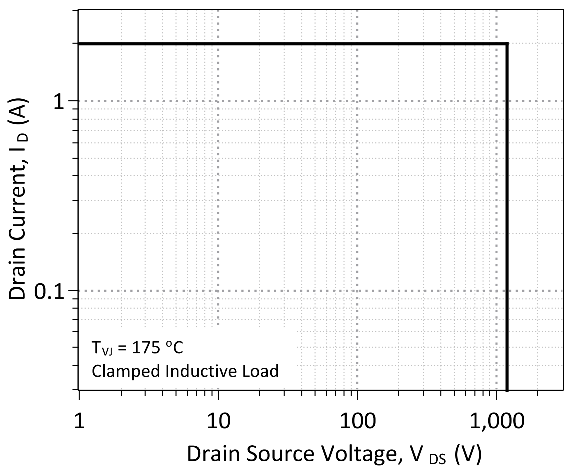


Figure 9: Turn-Off Safe Operating Area

Section IV: Driving the GR1500JT12-263

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis
TTL Logic	High	Low	Wide Temperature Range
Constant Current	Medium	Medium	Wide Temperature Range
High Speed – Boost Capacitor	Medium	High	Fast Switching
High Speed – Boost Inductor	Low	High	Ultra Fast Switching
Proportional	Lowest	High	Wide Drain Current Range
Pulsed Power	Medium	N/A	Pulse Power

Static TTL Logic Driving

The GR1500JT12-263 may be driven with direct (5 V) TTL logic and current amplification. The amplified current level of the supply must meet or exceed the steady state gate current ($I_{G,steady}$) required to operate the GR1500JT12-263. Minimum $I_{G,steady}$ is dependent on the anticipated drain current I_D through the SJT and the DC current gain h_{FE}, it may be calculated from the following equation. An accurate value of the h_{FE} may be read from Figure 2. An optional resistor R_G may be used in series with the gate pin to trim $I_{G,steady}$, also an optional capacitor C_G may be added in parallel with R_G to facilitate faster SJT switching if desired, further details on these options are given in the following section.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

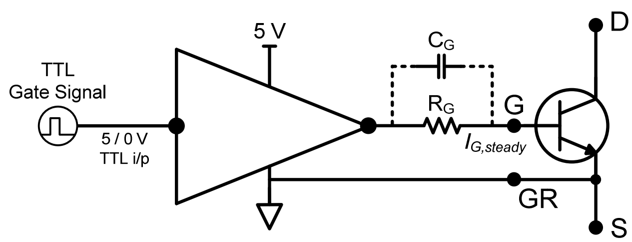


Figure 10: TTL Gate Drive Schematic

High Speed Driving

The SJT is a current controlled transistor which requires a positive gate current for turn-on and to remain in on-state. An idealized gate current waveform for ultra-fast switching of the SJT while maintaining low gate drive losses is shown in Figure 11, it features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current during on-state.

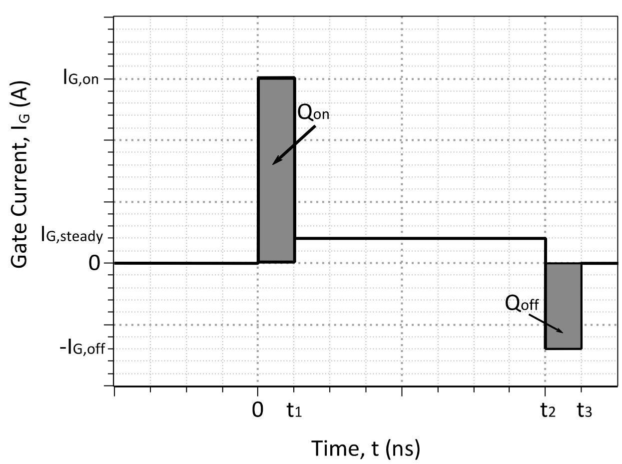


Figure 11: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the SJT gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally, $I_{G,on}$ should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the $V_{GS,sat}$ (see Figure 7) level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. Turn off can be achieved with V_{GS} = 0 V, however a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

A:1: High Speed, Low Loss Drive with Boost Capacitor

The GR1500JT12-263 may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. An example of this topology is shown in Figure 12.

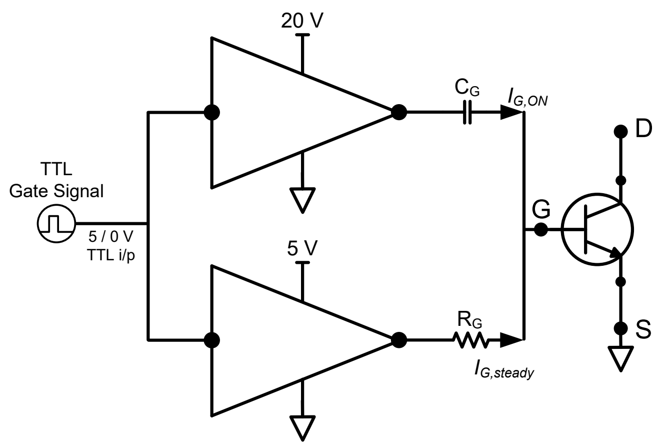


Figure 12: Simplified Boost Capacitor Drive Topology.

A:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GR1500JT12-263 at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SJT gate pin using logic control of S_1, S_2, S_3, and S_4, as shown in Figure 13. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G. Please refer to the article “A current-source concept for fast and efficient driving of silicon carbide transistors” by Dr. Jacek Rąbkowski for additional information on this driving topology.[3]

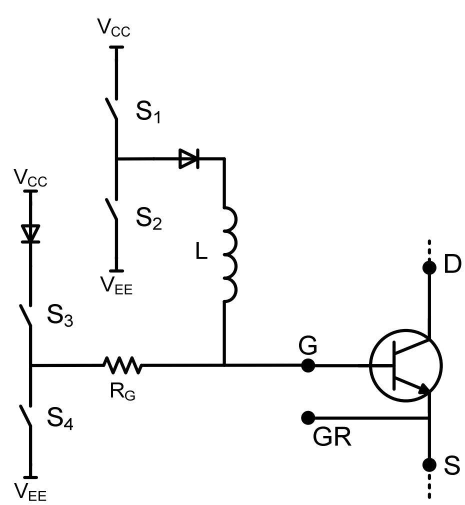


Figure 13: Simplified Inductive Pulsed Drive Topology

[3] – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/aee-2013-0026, June 2013

B: Proportional Gate Current Driving

For applications in which the GR1500JT12-263 will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the GR1500JT12-263

Voltage Controlled Proportional Driver

The voltage controlled proportional driver relies on a gate drive IC to detect the GR1500JT12-263 drain-source voltage V_{DS} during on-state to sense I_D. The gate drive IC will then increase or decrease $I_{G,steady}$ in response to I_D. This allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GR1500JT12-263 are in off-state. A simplified version of this topology is shown in Figure 14, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/

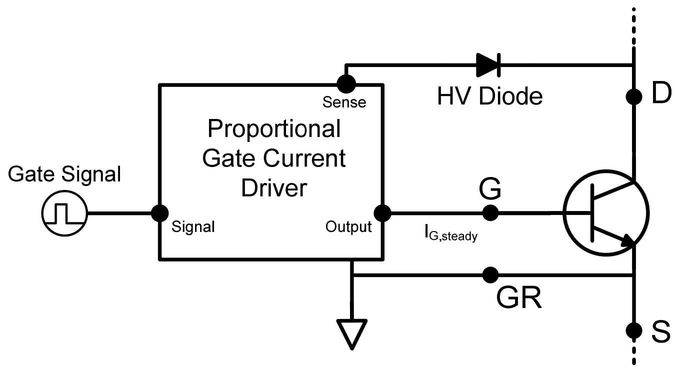


Figure 14: Simplified Voltage Controlled Proportional Driver

Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback I_D of the GR1500JT12-263 during on-state to supply $I_{G,steady}$ into the device gate. $I_{G,steady}$ will then increase or decrease in response to I_D at a fixed forced current gain which is set be the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. GR1500JT12-263 is initially turned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A simplified version of this topology is shown in Figure 15, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/.

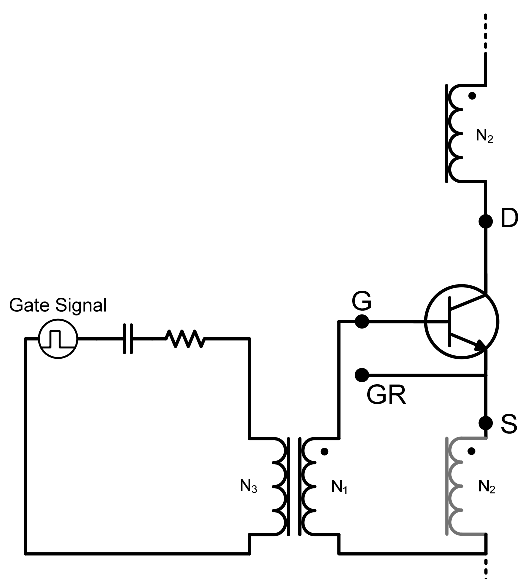
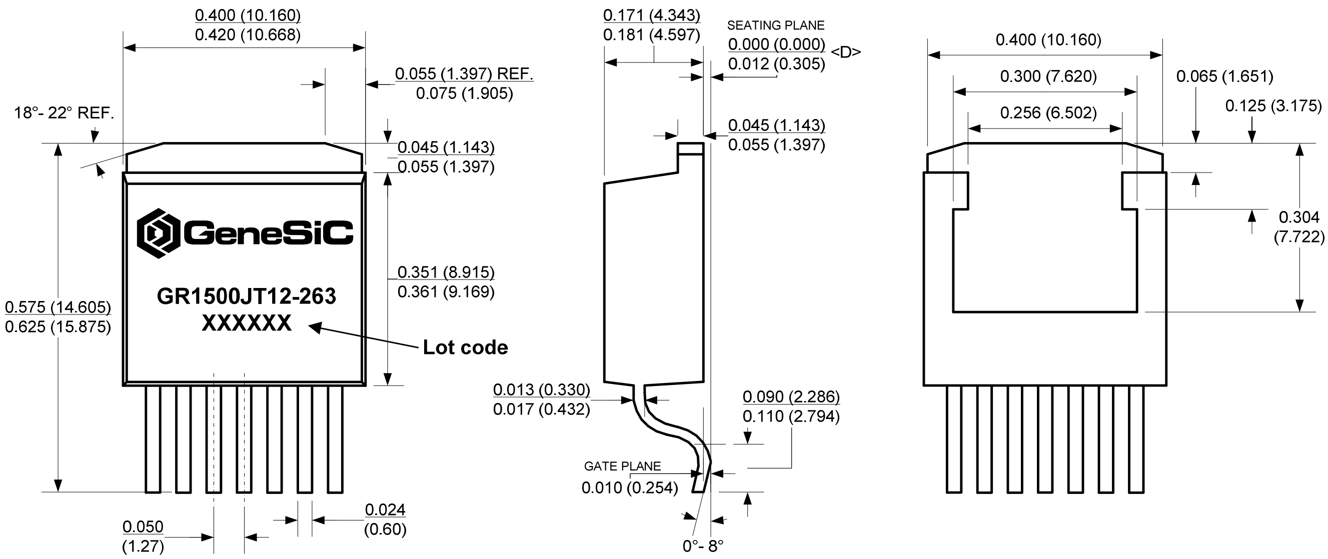


Figure 15: Simplified Current Controlled Proportional Driver

Section V: Package Dimensions

TO-263-7 **PACKAGE OUTLINE**



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2016/04/04	0	Initial release	

Published by
GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155
Dulles, VA 20166

Section VI: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/sjt/GR1500JT12-263_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GR1500JT12-263.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.0           $
*     $Date:   04-APR-2016       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2016 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GR1500JT12 NPN
+ IS       9.8338E-48
+ ISE      1.0733E-26
+ EG       3.23
+ BF       110
+ BR       0.55
+ IKF      5000
+ NF       1
+ NE       2
+ RB       20
+ IRB      0.002
+ RBM      0.6
+ RE       0.003
+ RC       1.5
+ CJC      25E-12
+ VJC      3
+ MJC      0.5
+ CJE      80E-12
+ VJE      3
+ MJE      0.5
+ XTI      3
+ XTB      -1.5
+ TRC1     6.5E-3
+ VCEO     1200
+ MFG      GeneSiC_Semiconductor
*
* End of GR1500JT12 SPICE Model
```